Low-Leakage Germanium-Seeded Laterally-Crystallized Single-Grain 100-nm TFT's for Vertical Integration Applications

Vivek Subramanian, *Member, IEEE,* Masato Toita, Nabeel R. Ibrahim, Shukri J. Souri, and Krishna C. Saraswat, *Fellow, IEEE*

***Abstract*—We report on 100-nm channel-length thin-film transistors (TFT's) that are fabricated using germanium-seeded lateral crystallization of amorphous silicon. Germanium-seeding allows the fabrication of devices with control over grain boundary location. Its effectiveness improves with reduced device geometry, allowing "single-grain" device fabrication. In the first application of this technology to deep submicron devices, we report on 100-nm devices having excellent performance compared to conventional TFT's, which have randomly located grains. Devices have on-off ratio $>10^6$ and subthreshold slope of 107 mV/decade, attesting to the suitability of germanium-seeding for the fabrication of high-performance TFT's, suitable for use in vertically integrated three-dimensional (3-D) circuits.**

I. Introduction

THIN-FILM TRANSISTORS (TFT's) have been considered for use in various three-dimensional (3-D) circuits, such as vertically integrated SRAM's [1] and DRAM's [2]. Submicron TFT's suffer from performance variations caused by statistical variations in the number of grains within the channel [3]. They also suffer from high leakage caused by trap-assisted carrier generation in defects in the drain depletion region [4]. Advances in lateral crystallization technology, such as nickel-induced [5] and germanium-induced lateral crystallization [6], allow control over grain location. The CMOS-compatibility of germanium seeding may allow the use of submicron TFT's in vertical integration applications. Seeding ensures the absence of grain-boundaries within the drain depletion region, resulting in TFT's having good off-state behavior. We have previously reported on the excellent scalability of germanium seeding to submicron dimensions [7]. Here, we report on the first 100-nm channel-length TFT's fabricated using germanium seeding. These devices have low leakage and good on-off ratios, demonstrating the advantages of germanium seeding.

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V. Subramanian, N. R. Ibrahim, S. J. Souri, and K. C. Saraswat are with the Department of Electrical Engineering, Stanford University, Stanford, CA 94305-4070 USA.

M. Toita is with Asahi Kasei Microsystems Company, Ltd., Tokyo 151-0053, Japan.

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II. Experimental Details

The devices detailed here were fabricated on oxidized silicon substrates to simulate their intended application in vertically integrated circuits, as shown in Fig. 1. The 100-nm amorphous silicon was deposited by LPCVD from silane at 550 °C/700 mtorr and patterned into active islands. The underlying oxide was also etched to a depth of 100 nm to allow the formation of a quasi-wraparound gate structure, to further reduce leakage current through improved gate control via three-dimensional coupling, as shown inset in Fig. 1. After active island patterning, 50-nm low-temperature oxide (LTO) was deposited at 450 °C from SiH_4 and O_2 and patterned and etched to expose seeding windows over the drain regions of the devices. Germanium was deposited selectively by LPCVD from GeH_4 at 450 °C/100 mtorr and the films were then crystallized at 550 °C. The selective deposition ensured that germanium was only deposited in the seed windows. During the crystallization, this germanium alloyed with the Si at the Si-Ge interface to form SiGe. This alloy crystallizes first and hence acted as a nucleation site for subsequent lateral crystallization [7]. After crystallization, the unreacted germanium was removed in H_2SO_4: H_2O_2 and the sacrificial oxide was removed in HF. Subsequent processing was similar to that of a conventional planar TFT process, except that the devices were fabricated such that the seeded grain extended into the channel, forming a "single grain" channel for small geometry devices. The peak processing temperature was 850 °C, used to form a 70-Å thermal gate oxide. The 200-nm LPCVD n+ *in situ* doped polysilicon was used as the gate electrode, and an 1100-Å LTO spacer was used. Titanium salicide was used to form low-resistance contacts, and dopant activation was performed at 800 °C/1 min. This was sufficient to activate the dopants without causing substantial diffusion via any grain boundaries and intra-grain defects. All submicron patterning was performed using electron beam lithography.

III. Results and Discussion

Electrical results for NMOS and PMOS devices are shown in Figs. 2 and 3, verifying the low leakage and good on-off ratio. These devices are unhydrogenated. Performance may be improved using plasma hydrogenation, shown in Fig. 4

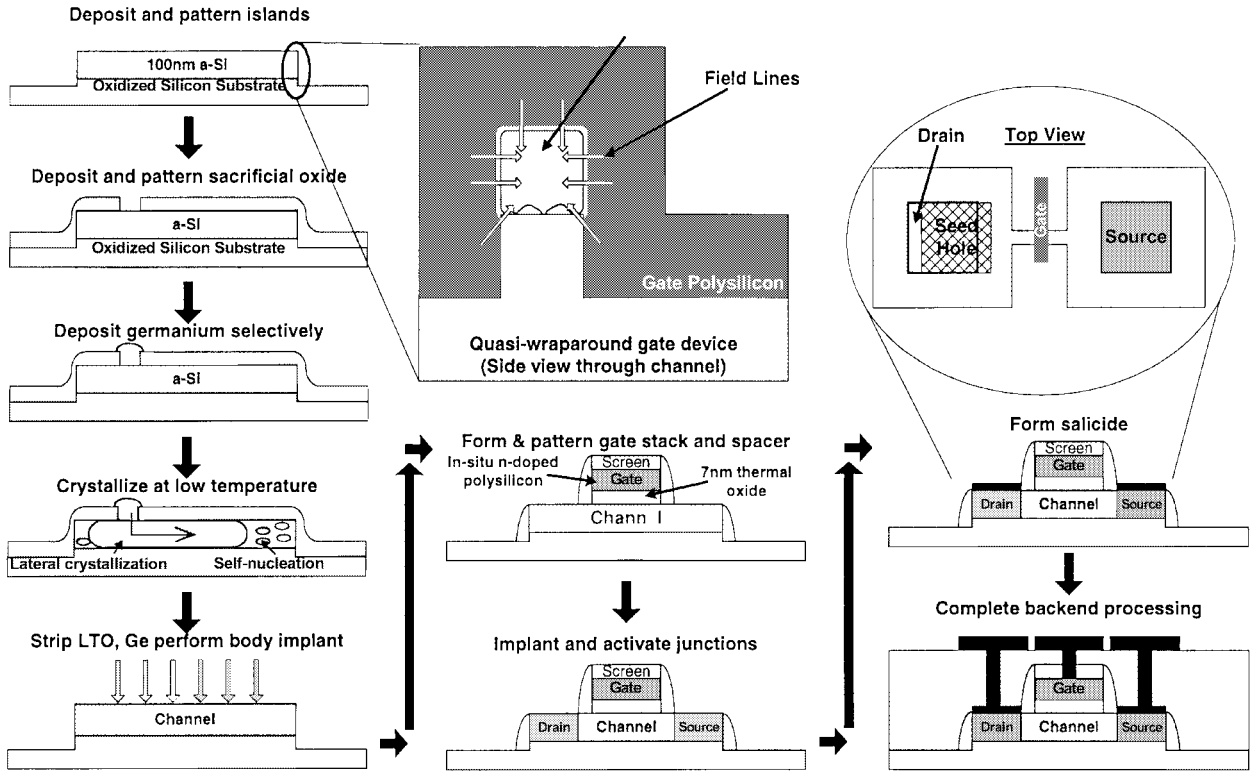
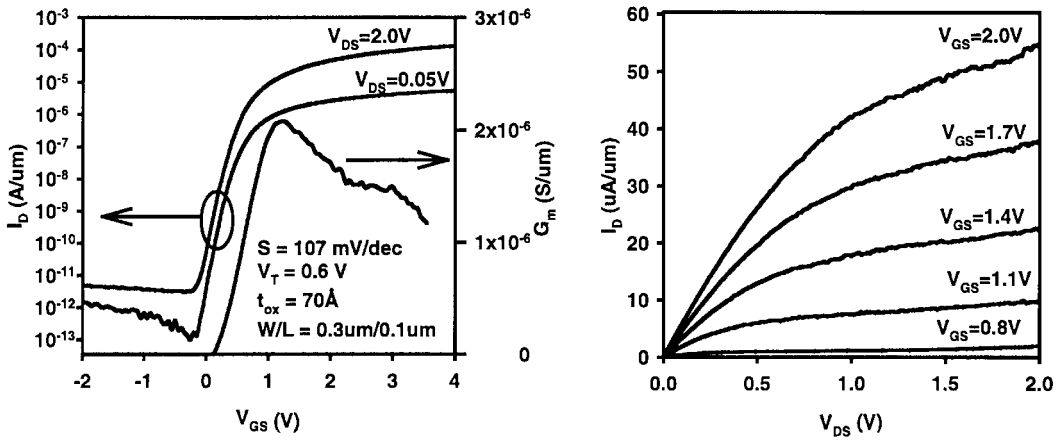


Fig. 1. Process flow for germanium-seeded 100-nm TFT's. A wraparound gatestructure (inset) is used to improve off-state behavior.

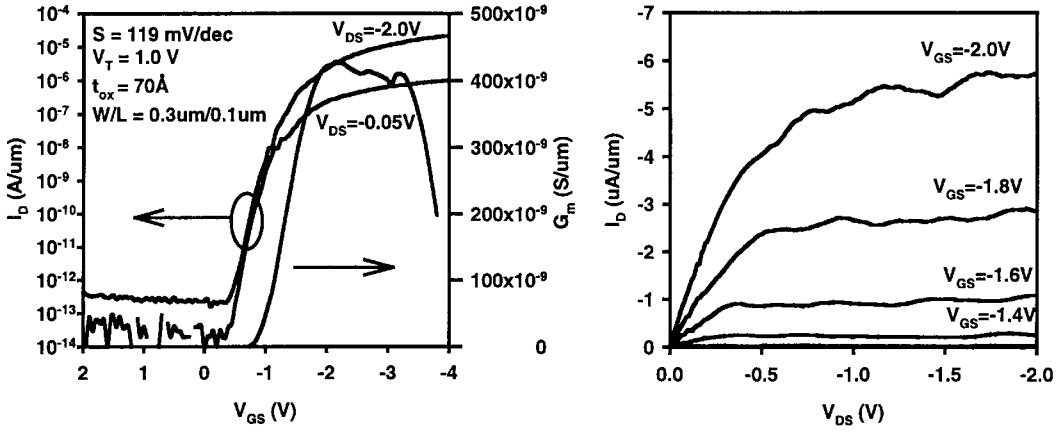


(a) (b)

Fig. 2. (a) Transfer and (b) output characteristics of NMOS TFT's.

for a sample nonoptimized device (with thicker spacer and gate oxide and no salicide). Both on- and off-state behavior improve.

The good characteristics of these devices are consequences of germanium-seeding. Since seeding is performed from the drain, grain growth occurs from the drain toward the source, and hence, the drain region is defect-free. The grain size of unseeded crystallized films is approximately 700 nm, and hence, for 100-nm devices, crystallization occurs through to the source, upon inclusion of the overlap tolerances, etc. Leakage current in TFT's is caused by trap-assisted carrier generation in the drain depletion region. Leakage may be reduced by using a drain-offset structure, as used in this work. However, this results in a decrease in on-current and hence, in poor on-off ratio. Combining a small drain offset with germanium-seeding results in both low leakage and high on-off ratio, as shown here. Since these devices have good crystalline quality near the drain, carrier generation is reduced, resulting in good off-state performance and good swing characteristics. To compare seeded and unseeded TFT's, performance of TFT's with varying numbers of grains within the channel are compared in Fig. 5. Clearly, the seeded TFT offers superior



(a) (b)

Fig. 3. (a) Transfer and (b) output characteristics of PMOS TFT's.

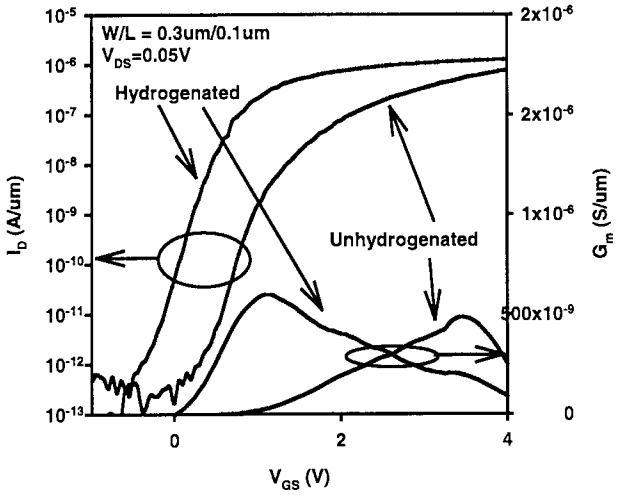


Fig. 4. Effect of hydrogenation on TFT performance.

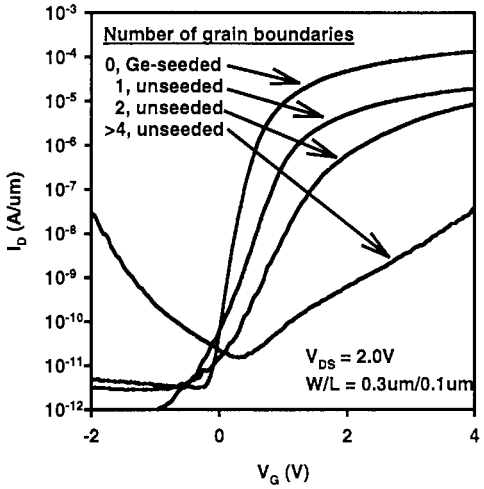


Fig. 5. Variation in electrical performance of TFT's with presence of grain-boundaries. Grain boundaries were detected using AFM on defect-etched reverse-engineered devices.

performance, making it attractive for applications requiring low leakage such as vertically integrated memory and mixed-signal applications. With these applications in mind, these devices have been optimized to ensure low leakage through control of doping profiles and through the use of the quasi-wraparound gate. Given the good on-off ratio of these devices, it should be possible to optimize these devices for high drive current for logic applications.

IV. Conclusion

The use of germanium-seeded lateral crystallization in the fabrication of 100-nm single-grain TFT's has been presented. Fabricated devices have excellent on-off ratio and off-state performance. This results from the use of germanium seeding to ensure good crystallinity in the drain depletion regions of the devices. Such low-leakage devices may have applications in vertically integrated memory and mixed-signal applications.

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