Optimization of Silicon-Germanium TFT's Through the Control of Amorphous Precursor Characteristics

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***Abstract*— Polycrystalline thin-film transistors (TFT's) are promising for use as high-performance pixel and integrated driver transistors for active matrix liquid crystal displays (AMLCD's). Silicon-germanium is a promising candidate for use as the channel material due to its low thermal budget requirements. The binary nature of the silicon-germanium system complicates the optimization of the channel deposition conditions. To date, little work has been done to perform this optimization, resulting in poor performance for SiGe TFT's. We report on optimization studies done on the low-pressure chemical vapor deposition of SiGe and its effect on TFT performance. We detail the results of a response surface characterization of SiGe deposition, and explain the obtained results in terms of atomistic models of deposition. Optimization strategies to enable the fabrication of high-performance SiGe TFT's are explained. Using these strategies, SiGe TFT's fabricated using solid phase crystallization and a 550 °C process are demonstrated, with mobility greater than 40 cm^2/V-s. Analysis is also performed on the effect of Ge-catalysis on the maximum optimization range. Results suggest that SiGe may offer enhanced optimization ranges over Si, as a result of this catalysis.**

***Index Terms*— Chemical vapor deposition, liquid crystal displays, optimization methods, silicon-germanium, thin-film transistors.**

I. Introduction

THIN-FILM TRANSISTORS (TFT's) find wide usage in active matrix liquid crystal displays (AMLCD's). Polycrystalline TFT's are promising for this application, as they may enable the integration of driver circuitry onto the glass substrate, reducing the overall manufacturing cost [1]. Silicon-germanium ($Si_{1-x}Ge_x$, hereafter referred to as SiGe) is a promising candidate for use as the TFT channel film, as it requires lower processing temperature than Si [2]. SiGe TFT's fabricated using low-temperature solid phase crystallization (LT-SPC) have been demonstrated [3]. For LT-SPC applications, SiGe is particularly advantageous, as it requires substantially shorter annealing cycles than required for the crystallization of Si. SiGe TFT's fabricated using scanned rapid thermal annealing (RTA) have also been demonstrated [4]. SiGe is advantageous for scanned RTA processes, as it requires lower crystallization temperatures, reducing glass warpage. To date, using conventional SPC processing with no pre-amorphization implant, SiGe TFT performance has generally been worse than poly-Si TFT performance [3]. SiGe TFT performance has been improved substantially through the use of n thin Si interlayer to improve the gate oxide interface [5]. However, little has been done to improve the intrinsic quality of the SiGe channel film itself; the binary nature of the SiGe system complicates optimization and modeling substantially. We have previously described preliminary optimization of SiGe TFT's through the use of multifactorial design of experiment techniques [6], [7]. In this paper, we describe the results of response surface characterization studies performed on the low-pressure chemical vapor deposition (LPCVD) of SiGe for the fabrication of SiGe TFT's. We detail TFT performance improvements achieved through the alteration of amorphous channel precursor deposition conditions, and describe a qualitative atomistic model of the deposition, explaining the variation in electrical results with the deposition conditions. We develop optimization strategies for the fabrication of high-performance SiGe TFT's, and discuss the limitations of such strategies.

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II. Background Information

A. Silicon-Germanium Deposition

Silicon-germanium is easily deposited by LPCVD from silane (SiH_4) and germane (GeH_4). To obtain amorphous films, deposition temperatures are usually lower than those required for the LPCVD of amorphous silicon [2]. This has been explained as a catalysis effect of germane [8]. Germanium species on the growing surface result in increased hydrogen desorption at any given temperature. Since this desorption is the rate limiting process in the deposition of silicon, this results in the observed increase in deposition rate.

The transition temperature for deposition in the amorphous phase to deposition in the polycrystalline phase is also lowered for SiGe. Therefore, SiGe depositions for the formation of TFT channel films are typically done at lower temperatures than those used for Si films. This ensures the formation of high-quality amorphous silicon germanium. Upon crystallization, these films form large grain poly-SiGe, suitable for the fabrication of polycrystalline TFT's.

Several factors affect the quality of the deposited amorphous SiGe. The deposition rate is a function of the temperature, pressure, and germanium fraction in the film. The germanium fraction in the film is itself a function of temperature and germane partial pressure relative to silane partial pressure. Therefore, the deposition of SiGe is a complex function of

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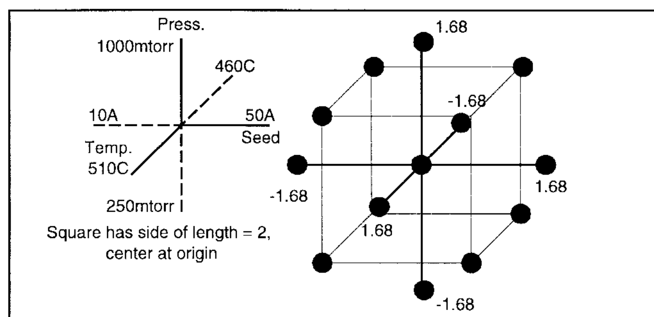


Fig. 1. Definition of experimental design space.

temperature, pressure and germane and silane partial pressures, and has been studied extensively [9]. The quality of the amorphous film is a function of the deposition parameters. Additionally, for the deposition of SiGe on SiO_2, it is necessary to deposit a thin seed layer of silicon on the oxide surface. This ensures the formation of a smooth channel film. Germanium deposition on oxide is not energetically favorable; therefore, failure to use a seed layer results in the deposition of rough films. This is caused by the initial clustering of germanium species on the growing surface. The use of a silicon seed layer solves this problem, but increases the complexity of analysis.

Given the numerous factors affecting the deposition and quality of amorphous silicon films, a systematic analysis of the same using standard factorial experimental design schemes is tedious and impractical; the problem is suitable for preliminary analysis using a multifactorial design of experiments

B. Design of Experiments

To enable the analysis of the deposition of SiGe, several process parameters of importance were identified using a Plackett-Burman screening experiment [10]. Based on the results of this experiment, detailed in [6], various parameters in need of further study were identified. These are the deposition pressure, temperature, and seed layer thickness. For reduced design complexity and size, germanium fraction was eliminated as a variable. All TFT's were fabricated with a 17% Ge fraction. This was chosen based on its high hall mobility [11], compatibility with conventional cleaning solutions, and ease of deposition. An experimental design space was selected for the various variables. Temperature ranges were chosen based on the ability to deposit amorphous films (defined the upper limit) and the ability to obtain reasonable deposition rates (defined the lower limit). Pressure ranges were selected based on the technological restrictions imposed by the deposition system. Seed layer thickness ranges were chosen based on the thickness ensuring full surface coverage (defined the lower limit). The upper limit of seed layer thickness was chosen to be small, based on the results of the screening experiment.

Upon definition of the experimental design space, a design was developed using standard design techniques. This design enables detection of first and second order trends. More sophisticated models could also be applied to the design results to enable detection of various nonlinear effects. The design space is shown schematically in Fig. 1.

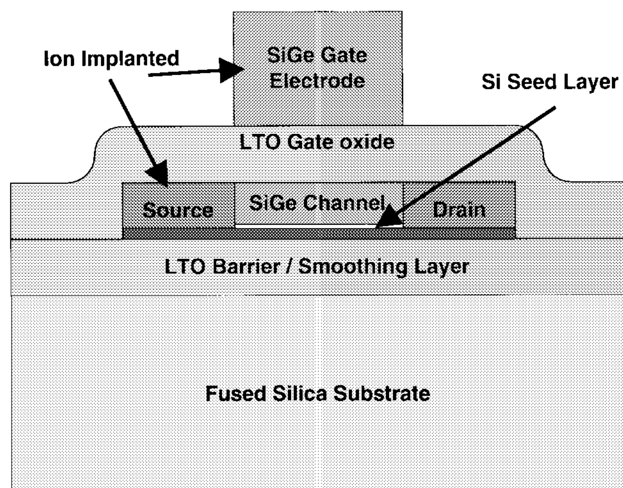


Fig. 2. Cross section of SiGe TFT.

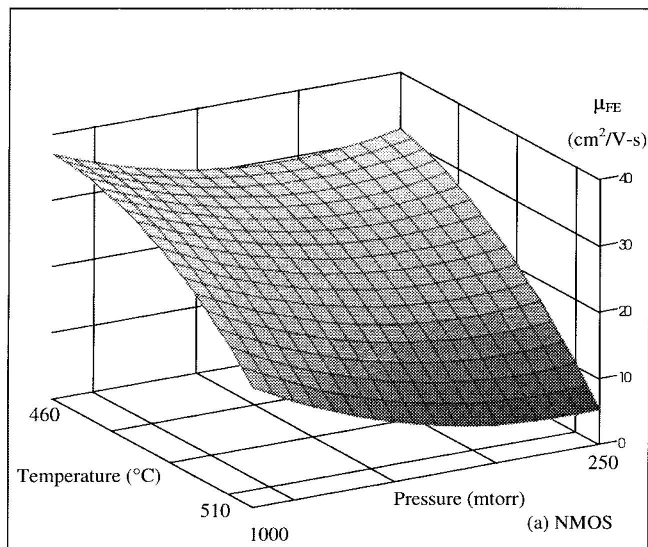
III. Experimental Details

All devices were fabricated on fused silica wafers. 100 nm LPCVD (LTO) SiO_2 was deposited on the substrates, for use as a barrier/smoothing layer. On this, amorphous channel films were deposited based on the conditions described in Fig. 1. The equipment used for deposition was a hot-wall tubular LPCVD system. The Si seed layer deposition was followed by the SiGe deposition without breaking vacuum. Subsequently, the films were crystallized in a furnace at 550 °C in an argon ambient. After crystallization, the active regions were patterned. 100-nm LPCVD SiO_2 was deposited as the gate dielectric and annealed in Ar at 550 °C for 6 h. This was followed by 250-nm $Si_{0.6}Ge_{0.4}$, which was used as the gate electrode. This film was chosen based on its high deposition rate at low temperatures (500 °C) and its ease of dopant activation (<2 h at 550 °C). Gates were defined, and doping was performed using ion-implantation. Dopants were activated at 550 °C. All dopants were activated within 4 h. After dopant activation, devices were passivated with LTO, contacts were formed, and metallization was performed using Al. The maximum process temperature was therefore 550 °C, ensuring compatibility with low-cost glass substrates. The wafers were plasma hydrogenated in a parallel plate system for 8 h, and electrical measurements were made. A cross section of the device structure is shown in Fig. 2. Plan-view TEM analysis was also performed on selected samples to determine the average grain size.

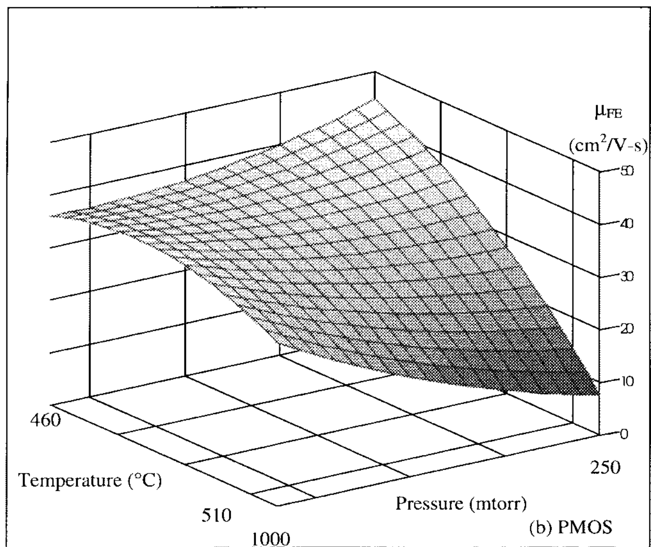
To test the accuracy of the model results, further devices were also fabricated as test devices. Deposition condition points were chosen away from the model vertices, near the edges of the experimental space, and near the center point. Results were compared to model predictions to determine model accuracy.

IV. Results and Discussion

Various electrical parameters were extracted from the measured current–voltage curves, including field-effect mobility, leakage current, subthreshold slope, and threshold voltage. Response surfaces were generated for the various parameters

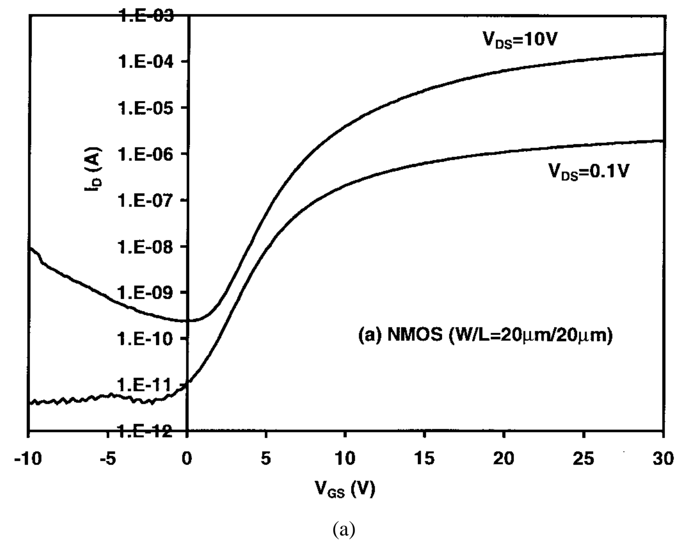


(a)

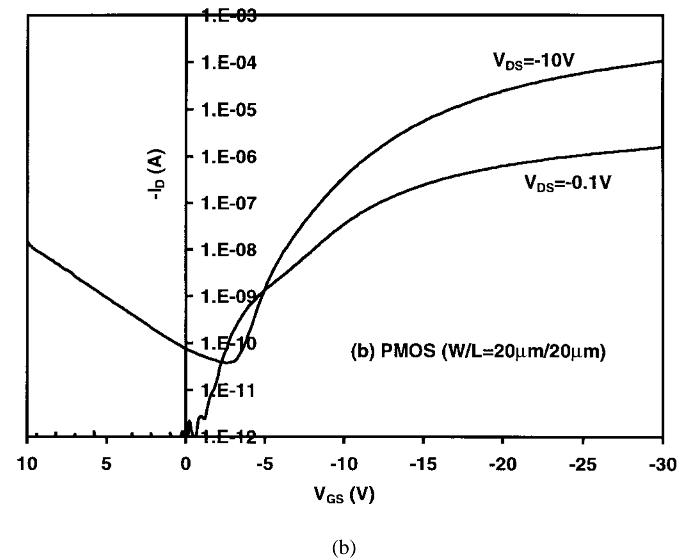


(b)

Fig. 3. Response surface of (a) NMOS and (b) PMOS mobility.



(a)



(b)

Fig. 4. Transfer characteristics of (a) NMOS and (b) PMOS TFT's.

using first and second order effects and interactions. Over the ranges of temperature, pressure and seed thickness used, it was expected that such models would provide good predictive ability. In general, it was found that all parameters demonstrated similar trends versus temperature and pressure, i.e., conditions that resulted in high mobility also resulted in steep subthreshold slope. It was also found that seed thickness generally has little effect on device performance over the ranges studied. Temperature and pressure, on the other hand, greatly affect device performance. The effect of temperature and pressure on device performance are shown in Fig. 3(a) and (b), which shows the variation in field-effect mobility with changes in deposition temperature and pressure.

From the response surfaces, it is apparent that performance improves with increasing pressure and decreasing temperature. At the lowest ranges of temperature and pressure, there is a saturation in improvement; indeed, some degradation is evident under some conditions. At intermediate temperatures and high pressures, performance is maximum, and importantly, performance improvement is not saturated, suggesting that further improvement can be achieved by increasing the ranges of pressure studied. Confirmation experiments verify these trends, suggesting that the predictive capabilities of the response surfaces are good. Within the ranges of temperature, pressure, and seed thickness used, SiGe TFT's having higher performance than previously achieved using a similar technology have been demonstrated. The transfer characteristics for sample NMOS and PMOS TFT's are shown in Fig. 4(a) and (b), respectively. Electrical parameters are summarized in Table I.

Based on confirmation experiments, the accuracy of the response surfaces has been found to be excellent over the ranges of temperature and pressure studied. Some deviation in actual and predicted values is evident near the boundaries of the experimental space; however, in all cases, the trend prediction has been found to be accurate, with only a slight quantitative discrepancy. Indeed, the trend prediction has been found to be satisfactory beyond the experimental space as well.

TABLE I
SUMMARY OF DEVICE CHARACTERISTICS

Parameter	Range of results			
	NMOS		PMOS	
	Worst	*Best*	*Worst*	*Best*
Field-effect mobility, μ_{FE} (cm^2/V-s)	5	38	6	44
Threshold Voltage, V_T (V)	12	5.5	-1.5	-8.5
Sub-threshold slope, sts (V/decade)	2.4	1.5	2.3	1.1
leakage current, I_{off} (pA/μm)	12	7	3	0.8

Field-effect mobility is defined as the maximum mobility achieved for V_{DS}=|0.1V|, V_{GS}<40V
Threshold Voltage is defined at I_D=100nA·(W/L), V_{DS}=|10V|
Sub-threshold slope and leakage current are defined at V_{DS}=10V

The trends determined experimentally are easily explained using conventional Si-based atomistic models of LPCVD [12]. With decreasing temperature, the surface diffusivity of physisorbed Si species is reduced. This reduces the amount of surface organization occurring before chemical bonding, thereby reducing the number of locally organized entities within the amorphous film. During crystallization, this corresponds to a reduction in nucleation sites present within the film, resulting in TFT's having larger average grain size, and hence, better performance. Deposition pressure results in an increased flux to the surface, and hence reduces the physisorbed lifetime on the surface prior to chemical bonding. This has a similar effect on the concentration of locally organized entities. The process is shown schematically in Fig. 5. At the lowest temperatures and highest pressures, however, the concentration of locally organized entities within the amorphous film is low enough that homogeneous nucleation within the amorphous matrix starts to dominate, resulting in the saturation and rebound observed in the electrical characteristics of the TFT's. This model is supported by a qualitative analysis of grain size obtained via TEM. In all cases, grains are typically elliptical in nature. Grain size was estimated by averaging the area of 100 grains and determining the diameter of a circle of equal area. Average grain size for the best channel films was found to be approximately 6500 Å, while the average grain size for the worst channel films was found to be somewhat lower, approximately 4000 Å. In general, while the largest grains in all films appear to be roughly the same size, the density of smaller grains is higher for the poor quality films, resulting in the decrease in average grain size. Additionally, all grains show evidence of intra-grain defects, seen by other authors for SPC films [13]; the concentration of these defects is visually higher in the poor quality films deposited at higher temperatures and lower pressures. Both these observations are expected results of the locally organized entity incorporation discussed above, since the presence of sub-critical organized entities in the amorphous film tend to increase nucleation and dendritic growth.

The atomistic model discussed above suggests a clear optimization strategy for SiGe TFT's, i.e., an increase in the deposition pressure and a decrease in the deposition temperature. However, clearly, such a strategy has practical limitations. In particular, at higher deposition pressures, gas-phase nucleation occurs, which results in extremely rough, defective, and poor

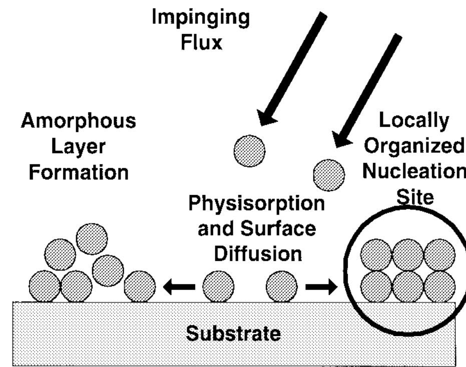


Fig. 5. Schematic view of atomistic deposition model.

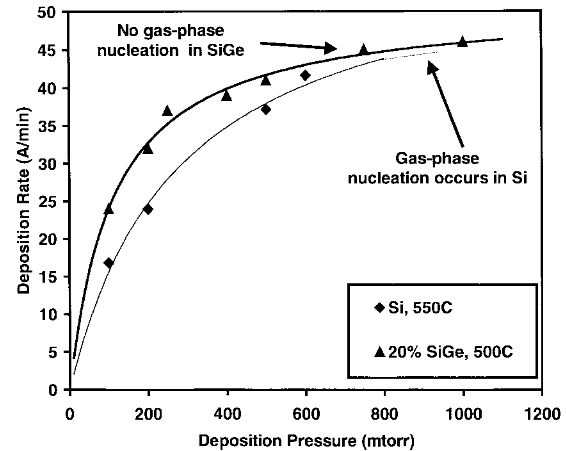


Fig. 6. Characterization of onset of gas-phase nucleation in Si and $Si_{0.8}Ge_{0.2}$.

quality films. In this regime, however, results suggest that SiGe may offer some advantages over Si. As mentioned above, Ge is a catalyst for the deposition of Si. It results in increased hydrogen desorption, increasing the deposition rate. This effect is therefore a surface effect. The effect of Ge on gas-phase reactions between Si atoms is not expected to be the same, since the process would require a greater germane partial pressure than present, resulting in decreased probability based on simple atomistic models.

For a given deposition rate at a low pressure of, for example, 100 mtorr, SiGe can be deposited at a lower temperature than Si. As the pressure is increased, the deposition rates of both SiGe and Si increase. However, at high pressures, the onset of gas-phase nucleation occurs in the Si deposition system. This point is offset to higher pressures in SiGe deposition, based on the lower deposition temperature, and hence gas-phase reactivity. This essentially amounts to an increase in the optimization space for SiGe deposition over that for Si deposition. Based on the response surfaces shown in Fig. 3, this corresponds to an increased maximum device performance. This is shown in Fig. 6, which shows the relative deposition rates and onset of gas-phase nucleation of Si and SiGe versus pressure for a similar deposition rate at low pressure. Shown in Fig. 7 is a schematic of the atomistic processes of catalysis. The differences in the shape of the deposition rate versus pressure curves shown in Fig. 6 are strongly indicative of the catalysis

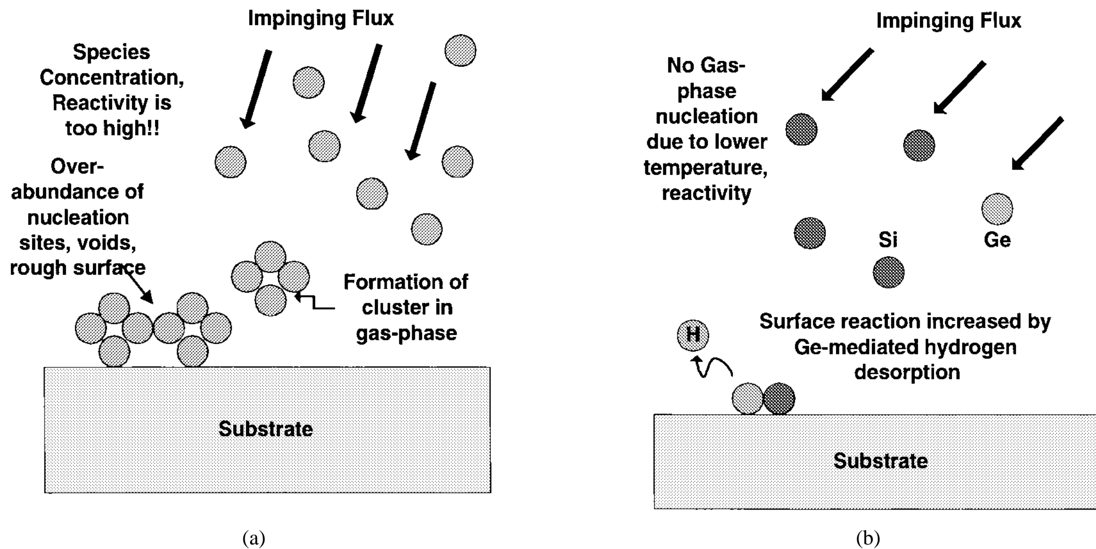


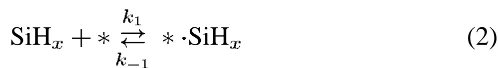
Fig. 7. Schematic view of (a) gas-phase nucleation and (b) the effect of Ge catalysis on the same.

process. The SiGe deposition curve shows a typical catalyzed reaction behavior [14]. The deposition is well described by a Michaelis–Menten catalyzed reaction equation

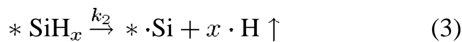
$$R = \frac{k_2 \cdot E_{\rm tot} \cdot P}{k_M + P} \tag{1}$$

where k_2 and k_M are constant, $E_{\rm tot}$ is the total amount of catalysis sites available, P is the deposition pressure, and R is the deposition rate.

Here, we make the simplifying assumption that the main rate-limiting reaction occurs in two stages



$$\mathrm{SiH}_x + * \underset{k_{-1}}{\overset{k_1}{\rightleftarrows}} * \cdot \mathrm{SiH}_x \tag{2}$$



$$* \, \mathrm{SiH}_x \overset{k_2}{\rightarrow} * \cdot \mathrm{Si} + x \cdot \mathrm{H} \uparrow \tag{3}$$

where $*$ is a bonding surface site, SiH_x is some silane species physisorbed to the surface, and k_1, k_{-1}, k_2 are rate constants.

Here, we assume that the first reaction includes the formation of the bonding site, *, within the rate constant k_1. For typical Si and SiGe reactions, this is hydrogen desorption limited. Assuming concentration-dependent reactions

$$k_M = \frac{k_{-1} + k_2}{k_1}. \tag{4}$$

For the case where hydrogen desorption is restricted, k_1 is small, and k_M becomes large. As k_M becomes larger, (1) results in more linear behavior with pressure. From Fig. 6, we note that this is indeed the case for Si.

The total number of Ge-catalysis sites available is a function of the equilibrium surface coverage by germanium, the H-desorption from these sites (assuming that H-desorption from these sites is much faster than desorption from Si-sites) and the total number of surface sites. Thus, at a constant germanium fraction, this number is essentially constant, resulting in the characteristic curve seen in Fig. 6. The Si deposition curve, on the other hand, exhibits a much more linear variation with pressure at the temperature used. Higher temperatures are required to deposit Si than those required to deposit SiGe at the same temperature and pressure. This results in increased gas-phase reactivity and hence an increased probability of gas-phase nucleation. Again, the catalyst effect of Ge is not evident in the gas-phase for low germane partial pressures, since the effect is a surface effect. For Ge to catalyze the gas-phase reaction, a substantially higher germane partial pressure would be required. At typical deposition temperatures, the gas-fraction of Ge-species is substantially less than the film-fraction of Ge. For example, to deposit $\mathrm{Si_{0.8}Ge_{0.2}}$ at 500 °C, a germane flow fraction of approximately 5% is required. Thus, there is a reduced probability of gas-phase nucleation for a given deposition rate and deposition pressure. The ability to sustain higher deposition rates in SiGe LPCVD without suffering from gas-phase nucleation suggests that it should be possible to extend the reaction window and improve TFT performance beyond the ranges of temperature and pressure available for the optimization of Si deposition.

From the experimental data summarized in Table I, it is evident that the field-effect mobility achieved within the range of optimization studied here is higher than achieved in previous works on glass-compatible SiGe TFT's. Additionally, the field-effect mobility falls within the range of results seen for standard silicon SPC processes. This has been achieved with a substantially lower thermal budget. Control silicon devices fabricated using the same process had typical mobilities in the range 35–40 $\mathrm{cm^2/V\text{-}s}$. Thus, on-state performance for SiGe devices is comparable to that of Si devices. Subthreshold slope, on the other hand, is quite high for SiGe devices (>1 V/decade) compared to that achieved for Si devices (NMOS $\sim$ 0.5 V/decade, PMOS $\sim$ 0.9 V/decade). This is probably related to the distribution of trap states within the band gap. The $\mathrm{SiO_2}$-SiGe interface is worse than the $\mathrm{SiO_2}$-Si interface [3]. Improving this interface through the use of a silicon interlayer has been found to affect the subthreshold performance of SiGe devices more that it affects the on-state performance [15]. This suggests that the interface traps are probably closer to the mid-gap. A solution to the poor off-state performance of SiGe TFT's is therefore to improve the gate dielectric

interface using a silicon interlayer. Coupling this with the channel optimization studied in this work should enable the fabrication of SiGe TFT's with good on-state and subthreshold performance at a reduced thermal budget when compared to Si TFT's.

V. Conclusions

Silicon germanium is a promising material for use as a channel in polycrystalline TFT's, due to its low temperature requirements when compared to polysilicon. Little has been done to characterize and optimize the deposition condition of the amorphous channel due to the complicated binary nature of the SiGe deposition system. The effect of channel deposition conditions on the performance of polycrystalline SiGe TFT's has been studied using a multifactorial design of experiments. It has been found that performance improves substantially with increasing temperature and decreasing pressure. This has been explained using an atomistic model of deposition. This model suggests simple optimization strategies for TFT performance enhancement through in increase in deposition pressure and a decrease in deposition temperature.

The effect of Ge catalysis on the atomistic behavior of the deposition system has been analyzed. Results suggest that gas-phase nucleation may be offset through the surface catalysis behavior of germanium. This will enable an extension of the optimization windows for SiGe TFT fabrication, and should enable the fabrication of high-performance SiGe TFT's for use in large-area glass-substrate active matrix technologies with integrated drivers.

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