

## Design and Characterization of SiGe TFT Devices and Process using Stanford's Test Chip Design Environment

M. V. Kumar, V. Subramanian, K. C. Saraswat, J. D. Plummer, and W. Lukaszek  
 Center for Integrated Systems, Stanford University, Stanford, CA 94305

**Abstract** – Stanford's test chip environment has been used to rapidly prototype a SiGe TFT process. The environment selected test structures tailored for the device/process. Then, with minimal effort and using parameterized test structures, the designer assembled a diagnostic test module. This module was used successfully in the development and optimization of the process, leading to the fabrication of high performance SiGe TFTs.

### INTRODUCTION

Thin film transistors (TFTs) find wide application in active matrix liquid crystal display (AMLCD) and static memory (SRAM) applications [1]. In recent years, there has been great interest in the possibility of developing a glass-compatible polycrystalline TFT process, which will enable the fabrication of low cost, high performance flat panel displays with integrated drivers. Silicon-Germanium (SiGe) is a material of great promise for achieving this goal, due to its lower processing temperature and thermal budget requirements [2]. The use of this binary alloy increases the number of process and device variables, and thus the optimization of this technology becomes correspondingly more difficult [3]. Therefore, the need exists for a set of test structures designed specifically for the SiGe TFT technology, to aid in process characterization and optimization. Given that the SiGe technology is still in its infancy and is constantly evolving, the ability to rapidly prototype test structures is extremely important. We describe the application of the Stanford Test Chip Design Environment [4] to this role, and describe its successful use in the optimization of a high-performance SiGe TFT process.

### BACKGROUND INFORMATION

Thin film transistor processes have several characteristics which make them different from standard single-crystal VLSI processes. For a glass-compatible technology, all processing is done at or below 600°C. This makes the use of thermally oxidized gate dielectrics impossible. Therefore deposited gate dielectrics are used. Active layers are also deposited, usually by LPCVD or PECVD. Given the number of deposition steps involved in the process, and the large area substrates used, cross-substrate uniformity becomes a critical parameter. Device performance is also a critical function of the characteristics of the deposited films. In particular, the deposition conditions of the active layer and the related process parameters greatly affect the device performance [5], as does the quality of the gate dielectric, which is typically inferior in quality to thermally oxidized dielectrics [6]. A characterization of the quality of these layers is therefore critical to enable optimization of the technology, and is critical to understanding and minimizing spatial non-uniformity.

Lithography is another critical step affecting large-area TFT processes. Given the large areas involved, spatial variations in exposure and linewidth are extremely important. Additionally, the use of transparent substrates greatly complicates exposure requirements, as the optical properties of the numerous thin films present result in large variations in absorbed dose during exposure. A proper spatial characterization of lithography parameters is therefore important.

Doping films on large area substrates is non-trivial. Ion-implantation techniques for large area substrates are under development, as are alternative techniques such as ion doping and gas immersion laser doping (GLD) [7]. Low-temperature activation of dopants is also difficult and inefficient. Degree of doping and dopant spatial uniformity is therefore another process parameter in need of characterization.

Given the large number of process parameters in need of characterization, a systematic test structure design is highly desirable. Additionally, rapid turnaround on test structure design is desirable to ensure quick iterations on process and device tests. The Stanford Test Chip Design Environment is admirably suited to achieve this.

Stanford's test chip design system contains a test structure advisor and a coupled, library-based layout and testing environment that dramatically increases productivity. The test structure advisor analyzes cross-sections of devices to recommend a comprehensive list of diagnostic and parametric test structures. These test structures can then be retrieved from the libraries of parameterized structures, customized, and placed in a design to rapidly generate customized test chips. Coupling of the layout and test environments enables the automatic generation of the vast majority of the parametric test software. This environment, shown in figure 1, manages the complexity of IC process testing related activities, ensures the efficient transfer of information between tasks, and provides users with an easy to use, intuitive interface. Thus, this environment expedites development activities and enables the rapid optimization of device and process technologies.

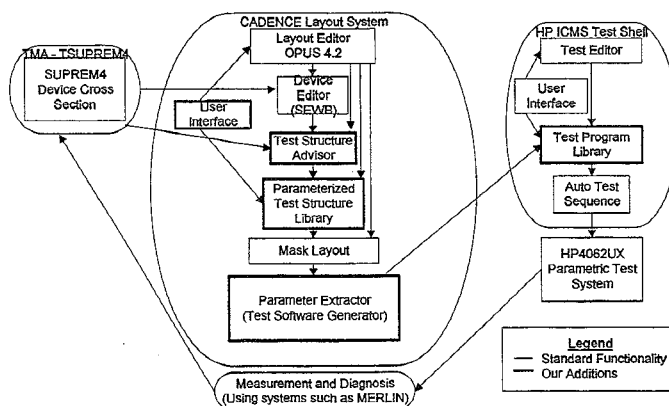


Figure 1: Stanford's Test Chip Design Environment

### TEST CHIP GENERATION

Cross-sections of the TFTs were drawn in DESTRUCTOR [8], a device structure editor, and sample cross-sections, such as that shown in figure 2, were used as the input to the test structure advisor. The advisor structurally decomposed the devices and recommended a set of orthogonal defect and parametric structures for the analysis of the devices and process.

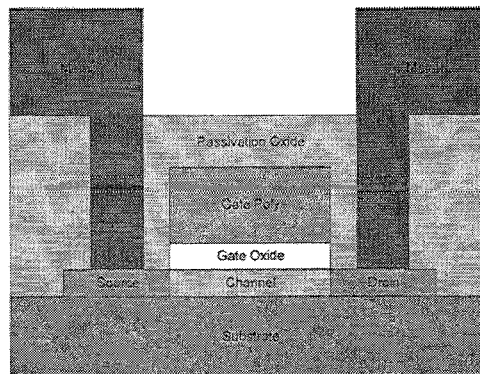


Figure 2: Typical planar top-gate TFT cross-section

Using structures from the parameterized test structure libraries, we were able to rapidly generate a test module. The module, shown in figure 3, contains 7 pad strips and 41 test structures. Padstrips PP1-PP3 contain parametric structures and PP4-PP7 contain defect structures. All the defect structures, both area and edge, are ratioed as 1:4:16. Test structures used

include van Der Pauws, line width structures, gate oxide leakage structures, contact chains, step coverage, etc. Additionally test structures were also generated in separate blocks tailored to the mask specifications, such as charge pumping structure [9], oxide reliability structures, and hall mobility structures. All the test structures were rapidly prototyped using Stanford's test chip design environment, with minimal input from the device engineer beyond a specification of the critical process issues and mask layers.

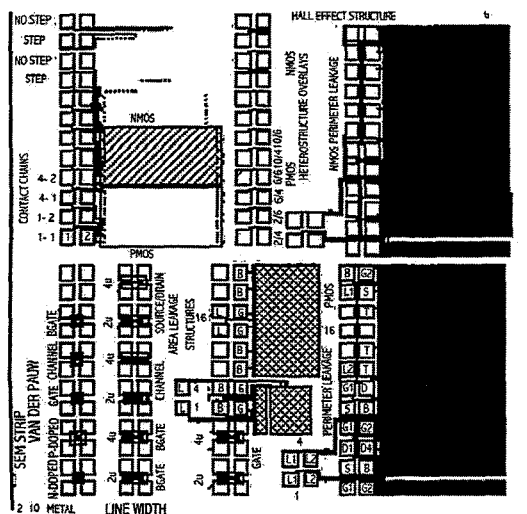


Figure 3: The TFT test module

#### TEST STRUCTURE DESCRIPTION AND RESULTS

##### Resistivity and Active Level Analysis

Resistivity of degenerately doped source/drain and gate regions was determined using standard van Der Pauw structures. The resistivity data was correlated to film thickness measurements made using optical techniques to obtain a measure of implant uniformity. For this analysis, dopants were activated in a furnace at 600°C to minimize variations due to activation non-uniformity. Uniformity was found to be good on silicon wafers (<2%). On quartz wafers, uniformity was found to be marginally worse (<4%). This was explained by charging effects occurring during ion implantation due to the insulating nature of the substrate [10]. Uniformity was found to improve by using a low-energy electron flood during implantation.

The efficiency of activation is a critical issue in glass compatible TFT processes. Activation is often done using a low temperature furnace anneal, as above. However, dopants are typically not fully activated, and sheet resistance is often substantially higher than sheet resistance obtained using a high temperature furnace step. A promising solution under consideration is the use of scanned rapid thermal annealing for dopant activation [11]. Resistivity structures were used to correlate the efficiency of activation with activation technique and temperature. Scanned RTA was found to be superior to low temperature furnace annealing. Sheet resistivity decreased with increasing peak transient temperature during the scan. The results of the above analyses are summarized below, in table I.

Table I: Comparison of activation techniques

Technique	Temperature (°C)	Sheet Resistivity ( $\Omega/\square$ )
Furnace anneal	600	295
Scanned RTA	700	223
Scanned RTA	800	192

A disadvantage of the SiGe system is the low level of activation achievable for many of n-type dopants [12]. In an attempt to compensate for this problem, a study was performed to determine the feasibility of making devices using Si source/drain regions and SiGe channel regions,

using the structure in figure 4. Using parameterized structures and devices generated by the advisor, it was determined that the simplistic assumptions above ignore the effect of the interface between the source/drain film and the channel film. Chains of interfaces showed a comparatively high resistance and some non-linear behavior. Devices were found to have poor on-off ratios and mobilities, as predicted by the parameterized component structures.

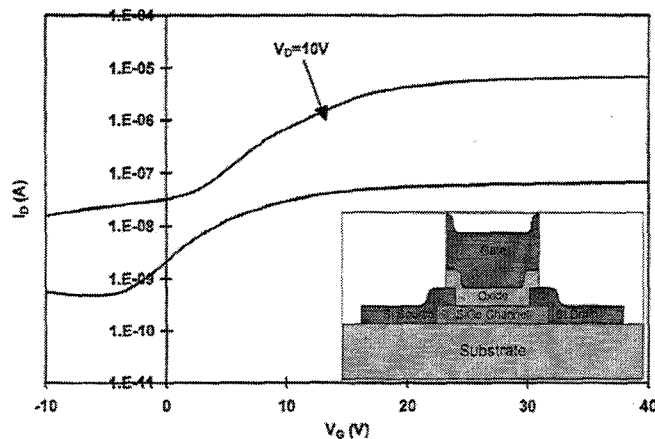


Figure 4: Transfer characteristics of independent terminal/channel film TFTs, showing degrading effect of poor film interface.

##### Lithography Analysis

Lithography requirements for display applications are different from those applying to standard VLSI processes [13]. In particular, the absence of a reflecting back-plane significantly complicates analysis of required exposure dose. Variations in thin films present greatly alter the absorbed dose to the resist. Additionally, due to the transparent substrate, absorbed dose showed some dependence on the wafer chuck, even for black anodized chucks. At insufficient exposures, chuck patterns were clearly visible in the resist scum. Line widths, as determined by parameterized line width structures, was found to vary greatly with film quality. For an identical initial film, the linewidth was found to vary depending on the phase of the film. For films amorphized during implantation, linewidth was found to be less than for films in the polycrystalline form due to the higher reflectivity of the former. This was verified using SAMPLE [14], a lithography simulator. The results obtained in the above analyses are summarized in table II.

Table II: Variation in linewidth due to wafer reflectivity

Wafer Details	Linewidth @110mJ
Poly-Si / Thick Oxide / Si Wafer	~0.9 $\mu$ m
Poly-Si / Quartz Wafer	~1 $\mu$ m
Amorphous-Si / Quartz Wafer	~0.9 $\mu$ m

##### Trap and Defect Analysis

The use of polycrystalline active layers and deposited dielectric layers make an analysis of defects with the channel and gate dielectric imperative, as these have a large effect on device performance. In particular, the dielectric is an area of intensive research. Numerous dielectric test structures were generated by the advisor. These include structures to analyze edge leakage and area leakage, structures to determine oxide charges, and structures to determine dielectric reliability. Results from these test structures were correlated to various process parameters. The oxide anneal was found to have a great impact on oxide quality, and in turn on device performance. RTA was found to be superior to low temperature furnace annealing for a similar thermal budget process [15]. Dielectric reliability was also found to have a strong dependence on annealing ambient. An oxidizing ambient was found to reduce dielectric reliability, as determined by constant current stressing of the capacitor test structures. This is shown figure 5.

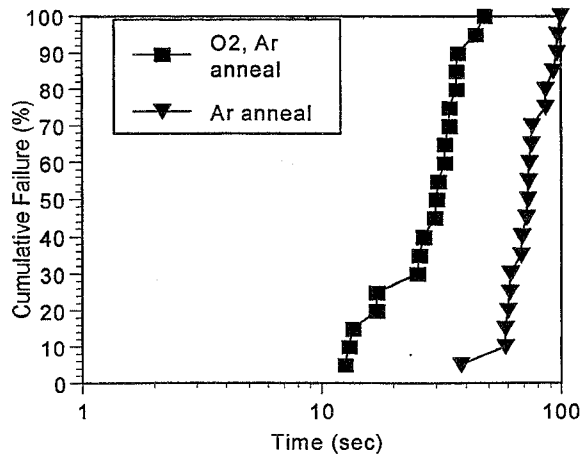


Figure 5: Dielectric Reliability tests: Effect of annealing ambient.

Dielectric deposited from different sources were also compared. Organic sources are promising for depositing gate dielectrics due to their quality and safety. Tetramethylcyclotetrasiloxane (TMCTS) was evaluated as an oxide source [16]. Results obtained from test structures suggest that TMCTS is superior to  $\text{SiO}_2$  deposited by LPCVD from  $\text{SiH}_4/\text{O}_2$  (LTO). This is reflected in device characteristics, as shown in figure 6.

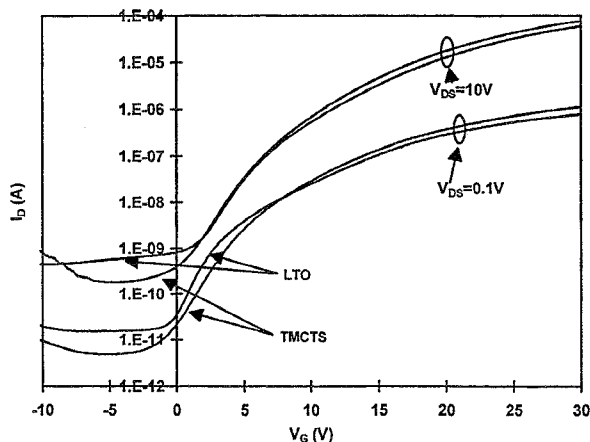


Figure 6: TFT transfer characteristics comparing LTO and TMCTS.

Defects in the channel film and dielectric interface can be evaluated using charge pumping. Charge pumping structures were used to analyze these parameters. Results obtained from charge pumping measurements indicate that it is an effective technique for determining device quality, and correlates well to both mobility and sub-threshold slope for similar films. Correlation was excellent for determination of cross-substrate variance, inter-wafer variance, and inter-batch variance for an identical process. Correlation was also good for devices having identical channel films but different dielectric properties. Correlation was poor for devices having different channel films, e.g., films having different Ge fractions. This suggests that charge pumping is an effective tool for analyzing non-uniformity and variance, but is unsuccessful at predicting optimization strategies for channel quality. This is explained by the fact that charge-pumping sums the effect of traps in the generation volume, and is unable to deconvolve combined effects of changes in generation volume, characteristics, and density.

#### CONCLUSIONS

The Stanford Test Chip Design Environment was used to generate a set of test structures for analysis and optimization of a SiGe TFT process. The test structures generated by the advisor were found to accurately provide an analysis of component parameters. These parameters correlate well to device performance, and were used to determine optimization strategies for

device performance improvement. Additionally, variance analysis of the results obtained from the structures was used to reduce non-uniformity in the process. This should enable the development of a high-performance, low-cost TFT process. The rapid turnaround and flexibility inherent to the test chip environment allowed this to be performance with a minimal overhead in design time for test structure layout.

#### ACKNOWLEDGMENTS

This work is funded by DARPA. Vivek Subramanian is partially funded through a Kodak fellowship. The authors wish to thank Dr. T.-J. King for assistance with device hydrogenation. The authors also wish to thank Dr. N. Bhat and Mr. Albert W. Wang for assistance with dielectric deposition processes.

#### REFERENCES

- [1] I.-W. Wu, "Polycrystalline Silicon Thin Film Transistors for Liquid Crystal Displays", *Solid State Phenomena*, Vol. 37-38, pp. 553-64, 1994.
- [2] S. Jurichich, T.-J. King, K. Saraswat, and J. Mehlhaff, "Low Thermal Budget Polycrystalline Silicon-Germanium Thin-Film Transistors Fabricated by Rapid Thermal Processing", *Japanese Journal of Applied Physics*, Part 2, Vol. 33, No. 8b, pp. L1139-41, 1994.
- [3] V. Subramanian, K. Saraswat, H. Hovagimian, and J. Mehlhaff, "Optimization and modeling of silicon-germanium thin film transistors for AMLCD applications using a Plackett-Burman experimental design." Presented at the First International Workshop on Statistical Metrology, Honolulu, HI, June 9, 1996.
- [4] M. V. Kumar, W. Lukaszek, and J. D. Plummer, "A Test Structure Advisor and a Coupled, Library-Based Test Structure Layout and Testing Environment", *Proceedings of the IEEE International Conference on Microelectronic Test Structures*, pp. 201-206, March 1996.
- [5] V. Subramanian, K. Saraswat, H. Hovagimian, and J. Mehlhaff, "Response surface optimization for high-performance solid-phase crystallized silicon-germanium thin film transistors", presented at the SPIE Conference on Electronic Imaging, San Jose, CA, February 8-14, 1997.
- [6] N. Bhat, P. P. Apte, and K. Saraswat, "Charge Trap Generation in LPCVD Oxides Under High Field Stressing", *IEEE Transactions on Electron Devices*, Vol. 43, No. 4, pp. 554-60, 1996.
- [7] A. Slaoui, C. Deng, S. Talwar, J. Kramer, and T. W. Sigmon, "Fabrication and doping of poly-SiGe using excimer laser processing", *Applied Physics. A (Solids and Surfaces)*, vol. A59, No. 2, pp. 203-7, 1994.
- [8] W. T. Wong, J. Y.-C. Pan., and J. D. Plummer, "A Virtual Factory-Based Environment for Semiconductor Device Development", *Proceedings of IEEE/SEMI International Semiconductor Manufacturing Science Symposium*, pp. 117-23, June 1992.
- [9] M. Koyanagi, Y. Baba, K. Hata, I.-W. Wu, A. G. Lewis, M. Fuse, and R. Bruce, "The Charge-Pumping Technique for Grain Boundary Trap Evaluation in Polysilicon TFTs", *IEEE Electron Device Letters*, Vol. 13, No. 3, pp. 152-4, 1992.
- [10] Y. Sato, K. Anzai, and F. Tadoroko, "Dose perturbation by wafer charging during ion implantation", *IEEE Transactions on Semiconductor Manufacturing*, Vol. 5, No. 4, pp. 329-36, 1992.
- [11] J. E. Fair, "Rapid thermal processing for active matrix devices", *Solid State Technology*, Vol. 35, No. 8, pp. 47-52, 1992.
- [12] T.-J. King, J. P. McVittie, K. C. Saraswat, and J. R. Pfister, "Electrical properties of heavily doped polycrystalline silicon-germanium films", *IEEE Transactions on Electron Devices*, Vol. 41, No. 2, pp. 228-32, 1994.
- [13] D. S. Holbrook, "Micropatterning for AMLCD fabrication", *SID International Symposium Digest of Technical Papers*, pp. 691-3, 1994.
- [14] SAMPLE User Guide - Version 1.8a, Electronics Research Lab, UC-Berkeley, June 1, 1991.
- [15] N. Bhat, A. Wang, and K. C. Saraswat, "Rapid Thermal Anneal of Gate Oxide for Low-Thermal-Budget TFTs", *SID International Symposium Digest of Technical Papers*, pp. 785-788, 1996.
- [16] A. W. Wang, N. Bhat, and K. C. Saraswat, "TMCTS for gate dielectric in thin film transistors", presented at the Spring Meeting of the Materials Research Society, San Francisco, CA, April 11, 1996.