# Response surface optimization for high-performance solid-phase crystallized silicon-germanium thin film transistors

Vivek Subramanian [a], Krishna Saraswat [a], Howard Hovagimian [b], and John Mehlhaff [b]

[a] Electrical Engineering Department, Stanford University, Stanford, CA 94305
[b] Intevac RTP Systems, Rocklin, CA 94765

## ABSTRACT

Silicon-Germanium (SiGe) is a promising material for polycrystalline thin film transistors (TFTs) for active matrix liquid crystal display applications due to its low thermal budget and temperature requirements. The use of SiGe as the channel material in a TFT allows for faster crystallization and dopant activation at lower temperatures than possible with pure silicon. Thus, a SiGe-based TFT technology has great promise as a high-performance, high throughput, uniform, glass-compatible TFT process.

Analysis of the SiGe system is difficult due to its binary nature. This complicates the development of optimization strategies for performance enhancement. The numerous variables and interactions affecting the SiGe system make a standard factorial characterization impractical. In this paper, we present the results of a reduced multifactorial response surface characterization of the system. The results obtained have been used to define optimization strategies for improving device performance. Tests have shown the strategies to be valid over a wide range of conditions. Using these strategies, n- and p-channel TFTs have been fabricated using a glass-compatible process and they exhibit substantially better performance than previously achieved using a similar thermal budget process. Further optimization using the determined guidelines should enable the development of a manufacturable high-performance poly-SiGe TFT process. Phenomena affecting the SiGe deposition system have also been identified, suggesting bounds on the optimization windows.

**Keywords:** Thin Film Transistor, TFT, SPC, Silicon-Germanium, SiGe, multifactorial

## 1. INTRODUCTION

The use of silicon-germanium (SiGe) as a channel material for low temperature polycrystalline thin film transistors (TFTs) has been studied extensively in recent years[1, 2, 3]. SiGe has substantially lower thermal budget requirements than pure silicon (Si), and is therefore promising as a material for use in a glass-compatible TFT technology. SiGe can be crystallized faster and at lower temperatures than silicon. Dopants can also be activated more rapidly at lower temperatures in SiGe than in Si. Thus, SiGe is an ideal candidate for use as a channel and gate material in a polycrystalline TFT.

Polycrystalline TFTs are typically made by depositing the channel in the amorphous phase and subsequently crystallizing it[4]. This enables the formation of a smooth, large-grain polycrystalline film. The ability to form high-quality large-grain polycrystalline channel films is critical to the fabrication of a high performance TFT. Several techniques are currently under consideration for crystallization of amorphous films. These include excimer laser annealing (ELA)[5], low temperature solid phase crystallization (SPC)[6], and rapid thermal annealing (RTA)[7]. Laser crystallization enables the production of extremely large grain polysilicon. Unfortunately, it suffers from low throughput and poor uniformity. This has adversely affected its adoption as a manufacturable TFT process. RTA has a high throughput, but suffers from poor performance due to the smaller grain sizes resulting from the excessive nucleation occurring at high crystallization temperatures. Low temperature SPC offers better performance than RTA at the expense of lower throughput. The combination of low-temperature SPC and SiGe should enable an improvement in the throughput of the SPC process, enabling the development of a spatially uniform, low-cost, glass-compatible polycrystalline TFT process.

The SiGe system, being binary in nature, is substantially more complicated than the pure silicon system. This complicates optimization strategies for the deposition and crystallization of the channel films. This is evidenced by the fact that, while SiGe has been studied as a TFT channel material for some time, little progress has been made in optimizing the deposition conditions to facilitate the fabrication of better-performance TFTs. Numerous variables affect the SiGe deposition system, including deposition temperature and pressure, germanium fraction, and silicon seed layer thickness[8]. The germanium

fraction is in turn a function of temperature and flow ratio. Thus, the system is a complicated one, with numerous parameters and interactions. This makes the use of a standard factorial experimental design impractical. We demonstrate the use of a multifactorial[9] approach to optimize the SiGe deposition system. Based on the results of this experiment, we define optimization strategies, which have been tested over extended ranges of the experimental space.

## 2. STATISTICAL FORMULATION

### 2.1 Problem definition

Numerous factors affect the final film quality of the SiGe low pressure chemical vapor deposition (LPCVD) system. These include deposition variables such as pressure and temperature, and crystallization variables such as crystallization temperature and the duration of the crystallization anneal. Additionally, various interactions between these variables complicate the analysis of the system. To reduce the scope of the problem to practical dimensions, it is necessary to employ statistical reduced multifactorial techniques to limit the size of the experimental matrix. To enable this reduction, the experimental space was subdivided by using a preliminary screening matrix to determine major effects and interactions[10]. Using the results of the screening experiment, a fully defined reduced multifactorial experimental matrix was designed to enable the determination of optimization rules.

Results obtained from the screening experiment indicated that the interactions between the crystallization parameters and most deposition parameters were not significant. The decision was made to fully characterize the effect of Ge fraction, and therefore, this parameter was maintained as fully independent. Based on Hall mobility measurements[11], the decision was made to study the performance of the 20% Ge system. Isolation of the Ge fraction as a variable allowed the separation of the deposition and crystallization systems without sacrificing any significant interaction determination capability, based on the results of the screening experiment. The crystallization variable optimization space is severely constrained by such technological issues as throughput and glass compatibility. The deposition variable optimization space, on the other hand, is far more flexible. Additionally, results obtained from the screening experiment indicated that the effect of deposition parameters on performance is extremely important for the SPC system. Therefore, in this work, we have developed optimization strategies for the deposition of SiGe by LPCVD, to enable the fabrication of high-performance poly-SiGe TFTs.

### 2.2 Experimental design

Based on the results of the screening experiment, the parameters selected for study were deposition pressure, deposition temperature, and silicon seed layer thickness. The first two parameters have already been established to be extremely important for the LPCVD of pure Si[12]. Seed layer thickness is unique to the SiGe system, and was therefore selected for immediate evaluation. The Si seed layer is used to improve uniformity of the deposited film, as SiGe exhibits some islanding when deposited directly on $SiO_2$. The ranges for study were selected as detailed below, in table I.

**Table I: Experimental range definition**

| Parameter | Levels | | Reasons for selection | |
|---|---|---|---|---|
| | ***Low*** | ***High*** | ***Low*** | ***High*** |
| Deposition temperature | 460°C | 510°C | Minimum for reasonable deposition rate | Transition to as deposited poly-SiGe |
| Deposition pressure | 250mtorr | 1000mtorr | Screening Experiment: higher is better | Limit of equipment |
| Seed layer thickness | 10Å | 50Å | Minimum for full wafer coverage | Screening experiment: Thinner is better |

Having determined the boundaries of the experimental space, the full matrix was formulated. To enable an acceptable resolution of effects and interactions while maintaining a manageable matrix size, a five-level design was chosen, with the

levels placed such that identification of both first and second order effects was possible. Such a design would enable the establishment of optimization strategies which were expected to follow physical models reasonably well within a defined range of values. The nodes were chosen such that some identification of physical processes was possible, and easily testable with additional experimentation. The experimental space definition is shown below, in figure 1.

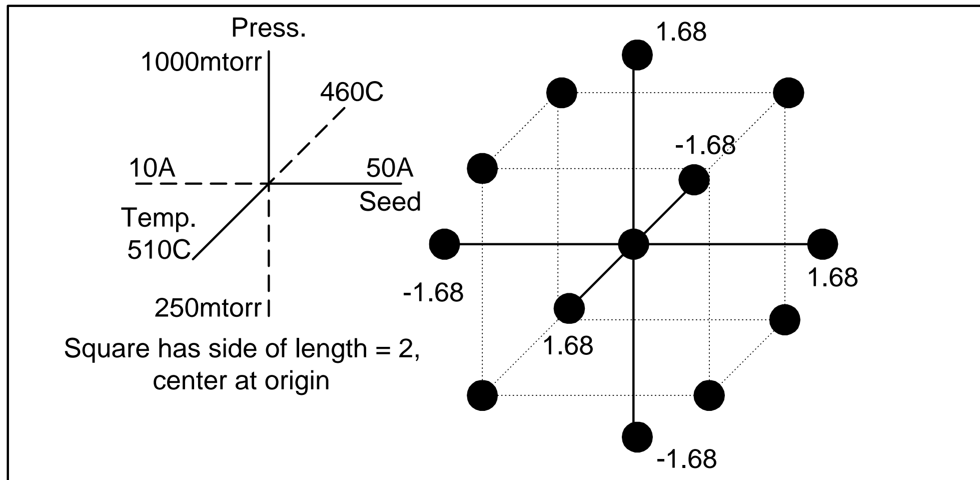


*Figure 1: Experimental definition, showing nodes and vertices.*

## 3. EXPERIMENTAL DETAILS

The TFTs were fabricated on quartz wafers using a low temperature (≤600°C) top-gate planar self-aligned process. 100nm $SiO_2$ was deposited as a barrier / smoothing layer on quartz wafers and subsequently densified. The channel films were deposited by LPCVD using the deposition conditions described above. All seed layers were deposited at 500ºC / 200mtorr. The SiGe channel layer was deposited after the seed layer without breaking vacuum, to ensure an atomically clean interface. The channel films were crystallized at 600ºC. All films were fully crystallized within 24hrs. The films were patterned and etched. 120nm $SiO_2$ (LTO) was deposited by LPCVD to form the gate dielectric. This was densified in Ar at 600ºC for 6hrs. Next, 250nm polycrystalline $Si_{0.6}Ge_{0.4}$ was deposited at 500ºC / 100mtorr and patterned to define the gate electrodes. The gate, source and drain regions were implanted with boron (PMOS) and phosphorus (NMOS) as appropriate. Dopants were activated at 600ºC. 400nm passivating oxide was deposited and contacts were defined. 1µm Al was sputtered and patterned to metallize the devices. The wafers were plasma hydrogenated to passivate traps.

Electrical measurements were performed to determine the various device parameters, which were analyzed to determine optimization strategies. Materials tests were also performed to determine the effect of the deposition parameters on material characteristics. Ge fractions were verified by x-ray diffraction (XRD) using a generalized focusing diffractometer (GFD), and by x-ray photoelectron spectroscopy (XPS / ESCA). Plan-view TEMs also performed to determine grain size. Intra-grain quality was determined from TEM and from XRD peak width. Material characteristics of the films were compared with electrical characteristics and optimization strategies to determine the phenomena affecting the device performance.

## 4. RESULTS

From the measured electrical characteristics, field-effect mobility, threshold voltage, sub-threshold slope and leakage current were determined for all devices and compared. In general, all parameters exhibited similar trends as a function of the deposition conditions. Performance in terms of all parameters except leakage current was found to improve with increasing deposition pressure and decreasing deposition temperature. Leakage current showed an inverse relationship, though the contrast between high and low was poor. The thickness of the seed layer was found to have no significant effect on device performance in the range considered. As per the screening experiment, significantly thicker seeding layers result in a deterioration in performance. The results obtained for the various devices are summarized in table II, along with a brief description of the definition of the various electrical parameters considered.

| Table II: Summary of electrical results (Device W / L=20μm / 20μm) | | | | |
|---|---|---|---|---|
| **Parameter** | **Range of results** | | | |
| | **NMOS** | | **PMOS** | |
| | ***Worst*** | ***Best*** | ***Worst*** | ***Best*** |
| Field-effect mobility, $\mu_{FE}$ ($cm^2$/V-s) | 5 | 38 | 6 | 44 |
| Threshold Voltage, $V_T$ (V) | 12 | 5.5 | -1.5 | -8.5 |
| Sub-threshold slope, sts (V/decade) | 2.4 | 1.5 | 2.3 | 1.1 |
| leakage current, $I_{off}$ (pA/μm) | 12 | 7 | 3 | 0.8 |
| Field-effect mobility is defined as the maximum mobility achieved for $V_{DS}$=\|0.1V\|, $V_{GS}$<40V<br>Threshold Voltage is defined at $I_D$=100nA·(W/L), $V_{DS}$=\|10V\|<br>Sub-threshold slope and leakage current are defined at $V_{DS}$=10V | | | | |

From the above table, it is evident that there is substantial variation in performance with deposition parameters. Additionally, the best achieved results represent, to our knowledge, the highest mobilities achieved for a polycrystalline TFT using LPCVD SiGe in a low temperature process. The results summarized above were used to determine optimization models for the system. The models account for first and second order effects. The models also account for intra-wafer and inter-wafer noise, and determine the effect of first and second order interactions as well. The determined optimization rules are best illustrated using surface maps, as shown in figures 2 and 3. Such maps are shown for field-effect mobility only, as it exhibits the maximum contrast, making it most visible.

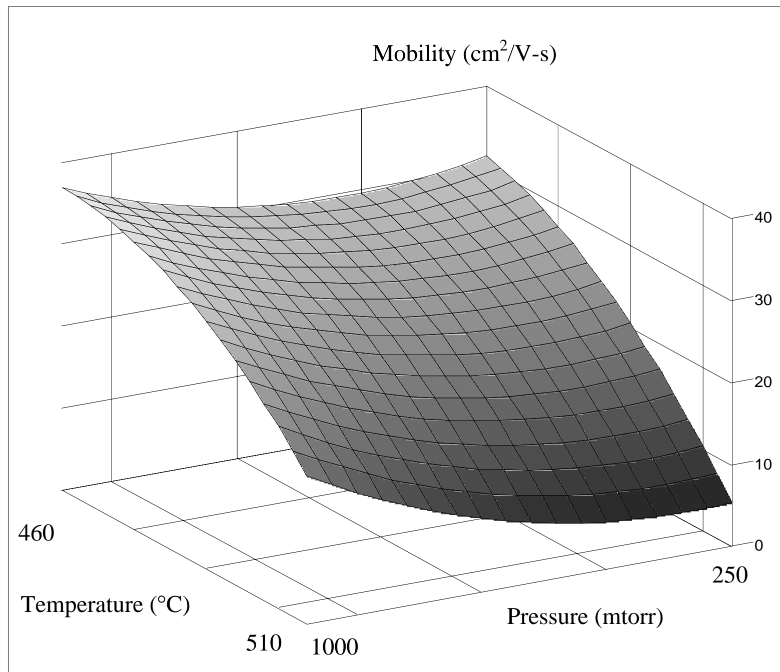


*Figure 2: Surface map of NMOS $\mu_{FE}$ vs. temperature and pressure*

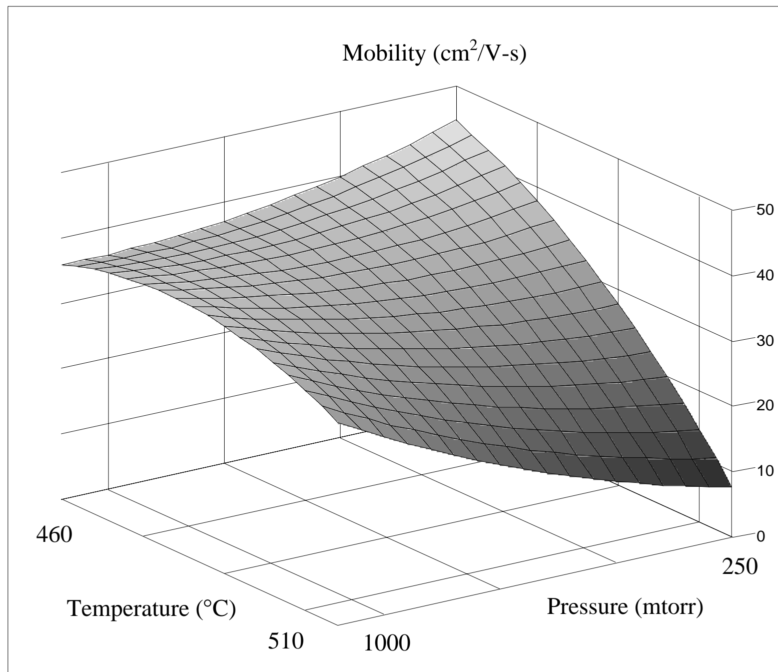


*Figure 3: Surface map of PMOS* $\mu_{FE}$ *vs. temperature and pressure*

From the above plots, it is clear that deposition temperature and pressure have a significant effect on device performance:

- Increasing pressure and decreasing temperature generally results in improved performance.
- There appears to be a saturation in device performance improvement at low temperatures.
- PMOS devices, unlike NMOS devices, show degradation in pressure-induced improvement at low temperatures.

To test the validity of the above observations, several test-point runs were made at various points both within and outside the optimization windows. All test runs matched predicted trends, though increasing deviations occurred from the predicted values as the conditions were moved beyond the optimization bounds. This is due to the failure of the second-order models used above to account for the extended deposition condition ranges. In all cases, however, general trends remained valid. Thus, the optimization rules are fairly accurate within the bounds above, and useful over wider ranges for trend prediction.

## 5. DISCUSSION

The trends described can be explained by considering models of nucleation and grain growth during LPCVD. At lower temperatures, surface diffusivity is reduced, and less organization of adsorbed atoms occurs during deposition. This reduces the frequency of grain-initiating nuclei present during SPC, increasing grain size. This is also true for higher pressures, where the increased deposition rates reduce diffusion lifetimes. These phenomena explain the trends seen. This is verified by TEM, which show that grains after SPC are larger for films deposited at lower temperatures and higher pressures. At the lowest temperatures studied, few nuclei are present, and homogeneous nucleation dominates during SPC, resulting in smaller grains. This explains the saturation observed. Test runs done beyond the temperature window exhibit a slight performance degradation, indicating homogenous nucleation. In NMOS devices, no saturation is found in pressure-induced enhancement. A saturation is visible as temperature is decreased. Films have been deposited at 1.5Torr showing further improvement. This is also true for PMOS devices with channels deposited at intermediate temperatures. At low temperatures, PMOS device improvement appeared to be saturated.

These conclusions indicate that further performance enhancement can be realized by increasing deposition pressure and maintaining an intermediate deposition temperature. For LPCVD, pressure cannot be increased indefinitely for a given temperature due to the onset of gas-phase nucleation. This suggests an upper bound on optimization. However, for SiGe, this boundary appears to be extended beyond that of Si. This is explained by the fact that the Ge-catalyzed reactivity

enhancement which occurs in the SiGe deposition system is a surface phenomenon[13]. For low Ge fractions, there is no significant reactivity enhancement in the gas-phase. Therefore, for a higher deposition rate (or the same deposition rate, but at a lower temperature), gas-phase nucleation is absent. This extends the optimization windows available for SiGe.

## 6. CONCLUSIONS

The deposition of amorphous SiGe by LPCVD for the channel material for low-temperature TFTs has been studied using a reduced multifactorial design. From the results obtained, optimization strategies have been defined. Performance can be significantly enhanced by depositing the film at a low temperature and high pressure. SiGe offers an advantage in this respect. The surface-catalyzed nature of SiGe deposition enables an extension of the windows available through the retardation of gas-phase nucleation relative to surface deposition. Results obtained have demonstrated the highest mobilities achieved to date using a SiGe technology of comparable thermal budget. Performance improvement is not saturated within the windows studied, suggesting the potential for substantial further improvement. Efforts are currently under way to extend the optimization window, enabling the development of a manufacturable high-performance poly-SiGe TFT process.

## ACKNOWLEDGEMENTS

The authors wish to thank Dr. T.-J. King for assistance with plasma hydrogenation. This work is funded by DARPA. Vivek Subramanian is partially funded through a Kodak fellowship.

## REFERENCES

1. T.-J. King and K. C. Saraswat, “Polycrystalline silicon-germanium thin-film transistors.”, *IEEE Trans. Electron Dev.* **41**(9), pp. 1581-1591, 1994.

2. H. L. Kao, S.-Y. Yang, and J.-W. Hong, “Study on recrystallisation of low temperature grown silicon-germanium films for thin film transistor applications.”, *Electronics Letters,* **32**(5), pp. 496-498, 1996.

3. A. J. Tang, J. A. Tsai, R. Reif, and T.-J. King, “A novel poly-silicon-capped poly-silicon-germanium thin-film transistor.”, *IEDM Technical Digest,* pp. 513-516, 1995.

4. I-W. Wu, “Polycrystalline silicon thin film transistors for liquid crystal displays.”, *Solid State Phenomena,* **37-38**, pp. 553-564, 1194.

5. K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko, and K. Hotta, “High-performance TFT’s fabricated by XeCl excimer laser annealing of hydrogenated amorphous silicon film.”, *IEEE Trans. Electron Dev.,* **106**, pp. 2868-2872, 1989

6. D. N. Kouvatsos, A. T. Voutsas, and M. K. Hatalis, “High-performance thin-film transistors in large grain size polysilicon deposited by thermal decomposition of disilane”, *IEEE Trans. Electron Dev.,* **43**(9), pp. 1399-1406, 1996

7. M. Bonnel, N. Duhamel, M. Guendouz, L. Haji, B. Loisel, and P. Ruault, “Poly-Si thin film transistors fabricated with rapid thermal annealed silicon films.”, *Jpn. J. Appl. Phys.,* **30**(11B), pp. L1924-L1926, 1991

8. M. Cao, A. Wang, and K. C. Saraswat, “Low pressure chemical vapor deposition of $Si_{1-x}Ge_x$ on $SiO_2$.”, *J. Electrochem. Soc.,* **142**(5), pp. 1566-1572, 1995.

9. R. L. Plackett and J. P. Burman, “The design of optimum multifactorial experiments.:, *Biometrika*, **33**, pp. 305-325, 1946

10. V. Subramanian, K. Saraswat, H . Hovagimian, and J. Mehlhaff, “Optimization and modeling of silicon-germanium thin film transistors for AMLCD applications using a Plackett-Burman experimental design.”, *First International Workshop on Statistical Metrology,* Honolulu, Hawaii, June 9, 1996.

11. J. A. Tsai, A. J. Tang, T. Noguchi, and Reif, “Effect of Ge on material and electrical properties of polycrystalline $Si_{1-x}Ge_x$ for thin-film transistors.”, *J. Electrochem. Soc.,* **142**(9), pp. 3220-3225, 1995.

12. M. K. Hatalis and D. W. Greve, “Large grain polycrystalline silicon by low-temperature annealing of low-pressure chemical vapor deposited amorphous-silicon films.”, *J. Appl. Phys.,* **63**(7), pp. 2260-2266, 1988

13. P. M. Garone, J. C. Sturm, P. V. Schwatrz, S. A. Schwatrz, and B. J. Wilkens, “Silicon vapor phase epitaxial growth catalysis by the presence of germane.”, *Appl. Phys. Lett.,* **56**(13), pp. 1275-1277, 1990.