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Applications of polycrystalline silicon-germanium thin films in metal-oxide-semiconductor technologies

King, Tsu-Jae, Ph.D.
Stanford University, 1994

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Applications of Polycrystalline Silicon-Germanium Thin Films in Metal-Oxide-Semiconductor Technologies

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING
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OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

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March 1994
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Abstract

Polycrystalline silicon (poly-Si) is an important component of silicon integrated-circuit (IC) technology and is currently used in a wide range of device applications. The fundamental properties of silicon-germanium (Si$_{1-x}$Ge$_x$) indicate that poly-Si$_{1-x}$Ge$_x$ can be a favorable alternative to poly-Si in many of these applications. Since the melting point of Si$_{1-x}$Ge$_x$ is lower than that of Si, physical phenomena controlling fabrication processes such as deposition, crystallization, and dopant activation occur at lower temperatures for Si$_{1-x}$Ge$_x$ than for Si. Thus, lower process temperatures can be used for poly-Si$_{1-x}$Ge$_x$, so that it is preferable to poly-Si for various applications in technologies which have limited thermal-budget allowances. In this work, a deposition technology for poly-Si$_{1-x}$Ge$_x$ films has been developed, and the physical and electrical properties of these films have been characterized. Two important potential applications of poly-Si$_{1-x}$Ge$_x$ films in metal-oxide-semiconductor (MOS) technologies have been investigated: first, the application as a gate-electrode material; second, the application as a thin-film transistor (TFT) channel material. The resistivity of heavily doped p-type (p$^+$) poly-Si$_{1-x}$Ge$_x$ is lower than that of comparably doped poly-Si, and its work function can be easily modified by adjusting its germanium content. These properties make p$^+$ poly-Si$_{1-x}$Ge$_x$ a very attractive candidate for the gate-electrode material in submicrometer complementary MOS (CMOS) technologies. p-channel TFTs fabricated in poly-Si$_{1-x}$Ge$_x$ exhibit well-behaved device characteristics and may be suitable for high-density static memory (SRAM) and three-dimensionally integrated circuit applications. n- and p-channel poly-Si$_{1-x}$Ge$_x$
TFTs have been successfully fabricated using conventional microelectronic fabrication techniques without exceeding 550°C. This demonstrated low-temperature-processing capability permits the fabrication of high-performance CMOS circuits on glass substrates using a process no more complex than that for fabricating silicon TFTs. Therefore, a poly-Si$_{1-x}$Ge$_x$ TFT technology is particularly attractive for large-area electronics applications.
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Chapter 1

Introduction

1.1 Motivation

Recently, there has been much interest in exploring the advantages of using single-crystalline silicon-germanium (Si$_{1-x}$Ge$_x$) epitaxial films for high-performance semiconductor device applications [1, 2, 3, 4]. Until the inception of this work, there was a lack of commensurate interest in polycrystalline Si$_{1-x}$Ge$_x$ films. The objective of this work was to characterize the physical and electrical properties of poly-Si$_{1-x}$Ge$_x$ films and to assess their advantages over poly-Si for various applications in metal-oxide-semiconductor (MOS) device technologies.

The resistivity and work function are two important electrical attributes of the gate-electrode material in MOS technologies. Heavily doped $n$-type polycrystalline silicon ($n^+$ poly-Si) has been traditionally used as the gate-electrode material for both the $n$-channel (NMOS) and the $p$-channel (PMOS) devices. As the dimensions of the devices are reduced, the high resistivity and the low work function of the $n^+$ poly-Si become increasingly problematic. The high resistivity results in large gate-level interconnection delays, while the low work function results in buried-channel PMOS devices, which are less scalable than surface-channel devices. Several techniques have been suggested to overcome these problems for submicrometer complementary MOS...
(CMOS) technologies, e.g. the use of dual n+/p+-doped polycide gates [5], and the use of a direct tungsten gate [6]. Although these alternatives provide low gate-line resistance and surface-channel NMOS and PMOS devices, they have practical limitations (i.e. lateral dopant diffusion in the connected n+ and p+ polycide gates causing threshold-voltage instabilities [5], and incompatibility of tungsten with Si fabrication processes) which make them difficult to implement in manufacturing. Because the electrical properties of Si$_{1-x}$Ge$_x$ can be tailored by changing its Ge content, the use of Si$_{1-x}$Ge$_x$ as the gate-electrode material can provide more flexibility in the design of a MOS field-effect transistor (FET) process: the gate resistivity can be lowered, and the gate work function can be modified in order to achieve a more-scalable CMOS technology.

Poly-Si thin-film transistors (TFTs) are currently used in various applications such as large-area electronics and three-dimensionally (3-D) integrated circuits[7, 8]. Low-temperature, short-time processing is desirable in these technologies, which have limited thermal budgets. TFTs fabricated in poly-Si films typically require process temperatures $\geq$600°C and/or long annealing times. Poly-Si$_{1-x}$Ge$_x$ films can be processed at significantly lower temperatures than poly-Si films. This capability suggests that poly-Si$_{1-x}$Ge$_x$ may be advantageous for TFT applications, since it could potentially provide a means of achieving high-performance devices with low-temperature ($\leq$550°C) processing. A poly-Si$_{1-x}$Ge$_x$ TFT technology would be no more complex than a poly-Si TFT technology, and would be compatible with low-cost glass substrates, and may thus open up a new domain of applications not accessible to Si TFT technologies.

1.2 Organization

Chapter 2 provides the background for this work. It gives an overview of the applications of poly-Si in integrated-circuit (IC) technologies, focusing on the uses of poly-Si as a gate-electrode material in MOS technologies and as the active layer in
Chapter 1. Introduction

TFT technologies.

Chapter 3 discusses methods for forming $\text{Si}_{1-x}\text{Ge}_x$ thin films. Two techniques are described in detail: first, the formation of thin $\text{Si}_{1-x}\text{Ge}_x$ films by high-dose germanium implantation; second, the growth of $\text{Si}_{1-x}\text{Ge}_x$ films by low-pressure chemical-vapor deposition (LPCVD).

Chapter 4 covers the properties of LPCVD $\text{Si}_{1-x}\text{Ge}_x$ films. In the first section of this chapter, the results of physical analyses using X-ray diffraction (XRD), transmission electron microscopy (TEM), and secondary ion mass spectrometry (SIMS) are presented. In the second section, the issue of poly-$\text{Si}_{1-x}\text{Ge}_x$ compatibility with modern silicon-based microelectronics fabrication processes is addressed. The electrical properties (resistivity, dopant-activation behavior, and work function) of heavily doped poly-$\text{Si}_{1-x}\text{Ge}_x$ films are presented in the final section of this chapter.

Chapter 5 covers the application of poly-$\text{Si}_{1-x}\text{Ge}_x$ as the gate-electrode material for various MOS technologies. The first section of this chapter discusses the advantage of using poly-$\text{Si}_{1-x}\text{Ge}_x$ in submicrometer CMOS technologies, due to its variable work function. In this section, the principles of gate work-function engineering are first reviewed. The current-voltage ($I-V$) characteristics of poly-$\text{Si}_{1-x}\text{Ge}_x$-gate MOS transistors, for gate materials of various germanium mole fractions, are then presented. Lastly, the advantage of using $\text{Si}_{1-x}\text{Ge}_x$ as a gate material is demonstrated through process and device simulations of short-channel devices, and the advantages of poly-$\text{Si}_{1-x}\text{Ge}_x$ are further elucidated. The second section of this chapter discusses the advantage of using poly-$\text{Si}_{1-x}\text{Ge}_x$ in TFT technologies, due to its low-temperature process compatibility. The fabrication and characterization of high-performance, low-temperature-processed ($\leq 550^\circ\text{C}$) poly-$\text{Si}_{0.5}\text{Ge}_{0.5}$-gate TFTs are presented in this section. This chapter concludes with a summary of the various advantages of poly-$\text{Si}_{1-x}\text{Ge}_x$, as compared to poly-Si, for use as the gate material in MOS technologies.

Chapter 6 covers the application of poly-$\text{Si}_{1-x}\text{Ge}_x$ as a TFT material. The first section of this chapter describes the high-temperature and low-temperature fabrication of $p$-channel devices, and presents the electrical characteristics of the first poly-$\text{Si}_{1-x}\text{Ge}_x$
Chapter 1. Introduction

TFTs. The second section describes the low-temperature (≤550°C) fabrication of n- and p-channel poly-Si$_{1-x}$Ge$_x$ TFTs, and presents an analysis of their electrical characteristics. The third section addresses various poly-Si$_{1-x}$Ge$_x$ TFT technology issues: the crystallization behavior of amorphous Si$_{1-x}$Ge$_x$, the effect of Ge at the SiO$_2$ interface, and the passivation of defects by hydrogenation. This chapter concludes with a summary of the potential advantages of poly-Si$_{1-x}$Ge$_x$, as compared to poly-Si, for TFT technologies.

Chapter 7 summarizes the contributions of this work and suggests further areas of investigation.
Chapter 2

Applications of Polycrystalline Silicon Films in MOS Technologies

Polycrystalline silicon (poly-Si) is used for a variety of applications in silicon integrated-circuit (IC) technologies, such as the gate material in metal-oxide-semiconductor (MOS) technologies, a contact and a diffusion source for the emitter and extrinsic base regions in bipolar technologies, high-value load resistors for static-memory (SRAM) cells, lateral diodes, and local interconnections. Recently, there has been much interest in the use of poly-Si as the active material in thin-film transistor (TFT) technologies, for applications such as three-dimensionally integrated circuits, high-density SRAMs, linear image sensors, thermal printer heads, and active-matrix liquid-crystal displays (AMLCDs). Detailed overviews of various applications of poly-Si in IC technologies are available in the literature [9, 10, 11]. The discussions in this chapter will thus focus only on the major applications of poly-Si as a MOS gate material and as a TFT material, to provide a background for the present work on polycrystalline silicon-germanium.
Figure 2.1: Schematic cross-sectional view of Al-gated NMOS transistor. The gate is lithographically aligned to the preformed source and drain regions, so that the minimum lateral overlap between the gate and the source/drain is limited by the alignment tolerance (Z) of the lithography process, which is typically much larger than the source/drain junction depth.

2.1 Poly-Si as a Gate-Electrode Material

The first silicon MOS transistors employed aluminum (Al) as the gate material (Figure 2.1). Since the melting point of Al is relatively low (660°C), this limited all process steps subsequent to gate-electrode formation to temperatures well below 500°C. Process temperatures in excess of ~600°C are required for dopant (e.g. arsenic, boron) activation in order to form the heavily doped source and drain regions; therefore, these regions had to be formed prior to the Al gate. To avoid the possibility of device failure due to an incomplete channel (where the gate does not fully extend to the source and drain regions), some overlap of the gate past the source and drain edges is required. In an Al-gate process, the gate must be lithographically aligned to the preformed source and drain regions, with an overlap large enough to allow for mask-alignment tolerances and variations in the lateral diffusion of source/drain dopants. This requirement not only prohibits the efficient scale-down of device size (channel length) for increased IC packing density, but it also results in a large gate-to-drain overlap capacitance. The parasitic capacitance leads to an undesirable feedback circuit effect (known as the Miller effect) between the input (gate) and output (drain) at high operating frequencies, limiting circuit speed.
Figure 2.2: Schematic cross-sectional view of NMOS transistor with poly-Si gate and self-aligned source/drain regions. The lateral overlap of the gate to the source/drain region is determined by lateral dopant diffusion and is therefore less than the source/drain junction depth $x_j$.

In order to overcome these problems, the source and drain regions must be formed after the gate electrode in a "self-aligned" process. This is accomplished by using the gate electrode as a mask for the formation of the source and drain regions (e.g. the implantation of source/drain dopants), so that the extent of the gate-overlap regions is determined by the extent of lateral dopant diffusion rather than by (much larger) lithographic tolerances (Figure 2.2). A self-aligned-gate material must be able to withstand the high temperatures required for the diffusion and activation of dopants and for the annealing of implantation-induced damage. Poly-Si is compatible with high-temperature processing, and it possesses many attributes which make it very suitable for application as a gate electrode:

- it can be readily deposited with excellent conformal step coverage by chemical-vapor deposition (CVD) technology;
- it can be easily etched using various wet or dry chemistries;
- it forms an excellent interface with the gate dielectric ($\text{SiO}_2$);
- it can be oxidized (to eliminate gate-edge leakage problems due to implantation-induced damage);
it can be heavily doped to approximate the desired properties of a metal electrode.

Poly-Si is thus the gate material of choice for modern MOS technologies.

Despite the many attractive properties of poly-Si, its use as a MOS gate material also poses some problems. For example, its relatively high resistivity (~1 mΩ·cm) can lead to large interconnection resistance-capacitance (RC) delays. This problem can be circumvented by depositing or forming a refractory silicide layer on top of the heavily doped poly-Si to obtain a low-resistivity “polycide” stack material with good gate-oxide-interface properties as well as a sheet resistivity sufficient for high-speed circuit operation.

The work function of poly-Si is problematic for gate applications in complementary MOS (CMOS) device technologies, which require symmetric, low n-channel and p-channel threshold voltages (i.e., \( V_{Tn} = |V_{Tp}| < 1 \text{ V} \)). This is because the work function of heavily doped n-type (n+) poly-Si is fairly low, so that its application as the gate material results in “buried” p-channel (PMOS) devices and highly doped “surface” n-channel (NMOS) devices, due to the nature of the required threshold-adjustment channel implants. In contrast, the work function of heavily doped p-type (p+) poly-Si is relatively high, so that its application as the gate material would result in buried-channel NMOS devices. Buried-channel devices are difficult to scale down because they are more susceptible to subthreshold-leakage problems due to punch-through and drain-induced barrier-lowering (DIBL) effects [12], which become more severe as device dimensions are decreased. Surface-channel NMOS devices with high channel-doping concentrations are more susceptible to hot-carrier reliability problems and become increasingly sensitive to hot-carrier degradation as channel lengths are reduced. Therefore, the use of either n+ or p+-poly-Si as the gate material results in a CMOS technology which cannot be easily scaled to deep submicrometer dimensions to achieve gains in performance and density.

The use of n+ poly-Si gate electrodes for the NMOS transistors and p+ poly-Si
gate electrodes for the PMOS transistors allows surface-channel NMOS and surface-channel PMOS devices to be concurrently obtained and therefore results in a more-scalable CMOS technology. However, it does not avoid hot-carrier reliability issues, and it also leads to complications in process integration. For example, $p$-$n$ junctions are created in the poly-Si layer from the connected NMOS and PMOS gate electrodes, resulting in high-resistivity interconnections. In order to shunt these $p$-$n$ junctions and reduce the resistance of the gate poly-Si layer, a silicide layer can be used to strap the poly-Si layer; however, rapid lateral diffusion of dopants in this overlying silicide layer can occur during high-temperature ($> 800^\circ$C) processing steps [13], resulting in threshold-voltage instabilities due to gate-work-function shifts [14]. Another complication which arises from the use of dual $n^+/p^+$ poly-Si gates is the need for an additional lithography step to separately define the $n^+$ and $p^+$ gate electrodes in technologies which employ in-situ-doped poly-Si films.

A more ideal CMOS gate material would not only possess all of the advantages of poly-Si but also have a work function in-between that of $n^+$ poly-Si and $p^+$ poly-Si, near that of intrinsic silicon. Such a “near-midgap” work-function gate material could be used to obtain both surface-channel NMOS and surface-channel PMOS devices which have the desired symmetrically low threshold voltages, and which have lower channel-doping concentrations for improved hot-carrier reliability. In general, as technologies are scaled to the deep submicrometer regime, it becomes desirable to minimize process “thermal budgets” since high-temperature processing causes thermal stresses and diffusion of dopants, resulting in reduced device yields. Therefore, it would also be advantageous for the gate material to be compatible with lower processing temperatures, so that it can be deposited, crystallized, and doped at low temperatures, at reasonable rates.
Figure 2.3: Equivalent-circuit diagram of a CMOS SRAM cell. The parasitic diodes between the connected PMOS and NMOS drains, which exist when the PMOS load transistors are implemented in an overlying poly-Si film, are also shown.

2.2 Poly-Si Thin-Film Transistors

2.2.1 Application in SRAM technology

In order to achieve a small cell size for high-density static-memory applications, the PMOS load transistors in a conventional six-transistor (6-T) CMOS SRAM cell (Figure 2.3) can be replaced by large-value resistors fabricated in a poly-Si layer overlying the NMOS drive transistors. However, resistive-load SRAM cells cannot simultaneously meet standby-current, stability, and soft-error-rate requirements for 4 Mbit and higher-density SRAMs [15]. A 6-T CMOS SRAM cell with overlying PMOS poly-Si TFT load transistors can meet these requirements because TFTs can have low leakage currents for reduced standby current and can provide large drive currents for improved stability. Various such “stacked-CMOS” cell technologies have been successfully demonstrated [16, 15, 17].
The main drawback of the stacked-CMOS cell is that it occupies more area than a resistive-load cell. The size of a stacked-CMOS cell can be reduced with improvements in TFT channel mobility for increased PMOS-drive capability [18]. Hole mobilities as high as $\sim 60 \text{ cm}^2/\text{V s}$ have been achieved in large-grained poly-Si films obtained by the solid-phase crystallization of amorphous silicon films [15]. The thermal budget for the PMOS TFT should generally be minimized in order to attain short-channel devices and to maintain high n$^+/p^+$ diode leakage currents (between the PMOS TFT drain and the NMOS drain – refer to Figure 2.3) for memory-cell stability and soft-error immunity [17]. However, the solid-phase crystallization process requires long anneal times (up to 24 hours [19]) at 600°C; in addition, subsequent high-temperature ($\geq 850^\circ\text{C}$) annealing is required to activate the implanted source/drain dopant (boron). Such large thermal-annealing requirements will become impractical as the dimensions of the cell transistors are reduced to well below 1 $\mu\text{m}$ for higher density memories. The development of a low-thermal-budget process for fabricating high-performance PMOS TFTs will thus be needed for future generations of high-density SRAM technology.

2.2.2 Application in AMLCD technology

The cathode-ray-tube (CRT) technology is the dominant display technology and therefore sets benchmarks in performance and cost for competing display technologies [20]. The major disadvantages of a CRT display are its large physical volume and weight, high power consumption, and relatively low brightness, which make it unsuitable for applications in portable electronic products and also for very large (> 40-inch diagonal) displays. Compared to the CRT, liquid-crystal displays (LCDs) offer the advantages of reduced volume and weight, lower power consumption, and improved brightness. Significant advances in the size, resolution, and performance of LCDs have been made in recent years, leading to the demonstration of large (up to 17-inch-diagonal), high-resolution, high-performance displays with color quality exceeding that of a CRT [21, 22, 23]. The $3 \text{ billion}$ worldwide LCD market is forecast
surpass $15$ billion by the turn of the century [24].

LCDS can be categorized into two types: passive-matrix (PMLCD) and active-matrix (AMLCD). In a PMLCD, the liquid crystal matrix is directly multiplexed by transparent conducting strips of indium/tin-oxide (ITO) patterned on the facing surfaces of two glass plates placed together with their respective strips running orthogonally and with a 6-10 µm gap for the liquid crystal [25]. The picture elements (pixels) are defined by the areas where ITO strips overlap. The disadvantage of direct multiplexing is that the voltage at one element affects the voltages at other elements which share a conductive strip with that element – a situation known as crosstalk. The optical response of the liquid crystal at each pixel is determined only by the root-mean-square (rms) value of the alternating (AC) voltage applied across the liquid crystal, so that it is possible to alter the liquid-crystal response at any individual pixel in the matrix with driving waveforms of the appropriate phase and polarity. However, the range of rms voltages that can be applied to the pixels is limited and becomes narrower as the number of multiplexed lines (N) increases. The available range is expressed as a selection ratio R, which is the ratio of the highest rms voltage to the lowest rms voltage, and is given by the equation [26]

$$R = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}}. \quad (2.1)$$

The selection ratio decreases with increasing N, approaching 1 for large values of N. For example, in a display with 100 multiplexed lines, a selected pixel will have only ~ 10% more rms voltage than a nonselected pixel. Because of this fundamental limitation on the rms liquid-crystal-drive voltage, the performance of high-density PMLCDs is limited to low contrast ratios and narrow ranges of good viewing angles.

The leading technology for high-quality flat-panel displays is the AMLCD technology. In an AMLCD, the limitation of the PMLCD's dependence of contrast ratio and viewing angle on the number of multiplexed lines is removed. This is done by using a semiconductor device with nonlinear electrical characteristics, e.g. a thin-film transistor (TFT) or thin-film diode (TFD), at every pixel to isolate and allow charge
Figure 2.4: Components of an AMLCD [27].

to be stored on the pixel for the duration of one frame time. The liquid-crystal-drive signal is directly applied through the semiconductor device to the pixel electrode, resulting in faster liquid-crystal response times. By independently controlling the voltage on each pixel, higher contrast ratios, wider viewing angles, and good gray-scale capability can be achieved at video rates. The components of a backlit color AMLCD are shown in Figure 2.4 [27]. The liquid-crystal cell (consisting of an active-matrix plate and a cover-sheet plate sandwiching the liquid-crystal layer) is driven by an addressing matrix to modulate the light from a backlight: a color filter (which is typically incorporated with the cover sheet) allows full-color images to be displayed.

TFT-AMLCDs are limited in gray-scale performance and display size, due to stringent requirements on device uniformity and threshold stability [28]. Therefore, the TFT has become the prevalent choice for the pixel-controlling semiconductor device in AMLCDs. An equivalent-circuit diagram for a TFT-AMLCD is shown in Figure 2.5. In contrast to a PMLCD, the pixels in an AMLCD are defined by separate ITO electrodes located on the active-matrix plate. A conductive layer of ITO on the
cover sheet (typically unpatterned) serves as a common counter-electrode. In a TFT-AMLCD, each pixel electrode is connected to a data line via a TFT. The scan lines are sequentially addressed to switch the TFTs on, one row at a time, and apply the data-line voltages to the pixel electrodes. For high-resolution (e.g. > 200 lines per inch) displays, a storage capacitor is added at each pixel to increase the total pixel capacitance and thereby improve pixel-charge retention (for enhancing gray-scale performance and avoiding flicker problems). This capacitor can be either a general ground capacitor or a capacitor formed between the pixel electrode and the prior scan line (as shown in Figure 2.5).

A brief history of the TFT and its application to LCDs is available in the literature [28]. Since the early 1980’s, there has been much interest in TFT-AMLCD technology, due to several reasons [28]:

- the availability of amorphous silicon (α-Si) and poly-Si as the TFT semiconductor material, allowing conventional semiconductor processing equipment/technology to be used for LCD fabrication;
Figure 2.6: Schematic cross-sectional view of standard inverted-staggered α-Si TFT structure.

- the development of portable computers, which require high-performance flat-panel displays;
- the inadequate performance of PMLCDs;
- the potential for the development of a pocket television market.

The α-Si TFT technology is currently the most developed and popular technology for TFT-AMLCDs, due to the low leakage (needed for good gray-scale performance) and adequate drive current (needed for pixel charging) of α-Si TFTs, and the broad base of process technology which can be derived from MOS VLSI technologies.

α-Si TFTs can be made with a variety of architectures, but the “inverted-staggered” structure (Figure 2.6) is the one most prevalently used. The α-Si channel film is deposited by plasma-enhanced chemical-vapor deposition (PECVD), and contains a significant amount of hydrogen (typically several atomic percent). For proper device operation, the α-Si film must remain hydrogenated; thus, all processing steps subsequent to the α-Si deposition step must be carried out at temperatures below ~350°C. Because it is difficult to obtain highly conductive α-Si by dopant-ion implantation (limiting processing temperatures to below 350°C), the TFT source-and-drain ohmic-contact regions are obtained by the deposition of heavily doped (n+) α-Si.
A major drawback of the α-Si TFT is its non-self-aligned-gate structure, which not only prevents the efficient scale-down of TFT channel lengths (as discussed in Section 2.1), but also leads to a relatively large parasitic overlap capacitance \( C_{gd} \) between the gate and the source/drain. This leads to the need for a larger pixel storage capacitance \( C_s \) in order to maintain a low feed-through voltage (to achieve good gray-scale performance and avoid flicker problems). The feed-through voltage \( \Delta V_p \) is the shift in pixel voltage which occurs as a result of capacitive coupling between the pixels and the scan line when the scan-line voltage is dropped from \( V_{ON} \) to \( V_{OFF} \) to turn off the corresponding row of TFTs:

\[
\Delta V_p = \Delta V_g \frac{C_{gd}}{C_{gd} + C_{lc} + C_s}.
\]  

(2.2)

In Equation 2.2, \( C_{lc} \) is the liquid-crystal capacitance, and \( \Delta V_g \) is the scan-line voltage swing, \( V_{ON} - V_{OFF} \). The relatively large (opaque) storage capacitor needed to effect a low \( \Delta V_p \) limits the display aperture ratio (fractional area of each matrix element which can be used for transmitting light) and results in reduced display performance.

Another drawback of α-Si TFTs is their low carrier mobilities, which typically range from 0.3 to 1 cm²/V s for NMOS devices, and are less than 0.01 cm²/V s for PMOS devices. Such low mobilities are inadequate for effective implementation of CMOS circuitry in α-Si and thus prohibit the integration of driver circuitry with the addressing matrix, needed for very-high-density (less than \( \sim 50-\mu m \) line-pitch) displays because of packaging constraints. As the number of addressed lines in the display is increased, the pixel-charging time is decreased (for a constant frame time), so that higher TFT-drive currents are required. Because of the relatively low electron mobility, large (wide) α-Si pixel TFTs will be needed (since the channel length cannot be easily scaled down), which further limits the aperture ratio. In short, the limitations stemming from a non-self-aligned structure and low carrier mobilities make α-Si TFTs inadequate for high-performance, very-high-density applications such as high-definition projection AMLCDs.

Poly-Si TFTs offer significantly improved device performance (~two orders of
magnitude higher mobility) compared to α-Si TFTs. Both NMOS and PMOS high-mobility (> 10 cm²/V s) devices can be achieved, making it possible to implement reasonably fast (≫ 100 kHz) CMOS circuits in poly-Si for the integration of peripheral driver circuitry with the AMLCD. Such integration reduces the number of external connections and driver chips required, and thereby improves reliability and lowers cost. A cross-sectional view of a conventional poly-Si TFT structure is shown in Figure 2.7. The Si channel layer is typically deposited by low-pressure chemical vapor deposition (LPCVD), and is patterned prior to the growth/deposition of the gate oxide. Heavily doped poly-Si is the preferred choice for the gate-electrode material, because of its excellent SiO₂-interface properties and its refractory nature. The TFT source-and-drain ohmic-contact regions are formed by dopant-ion implantation (using the patterned poly-Si gate electrode as a mask) and subsequent thermal annealing. The resulting self-aligned-gate structure minimizes parasitic overlap capacitances and facilitates reductions in channel length. Coupled with the high carrier mobilities, this allows for smaller TFTs as well as smaller pixel storage capacitors, and therefore larger aperture ratios.

A critical issue in the application of poly-Si TFTs to AMLCDs is the relatively high poly-Si TFT leakage current. This leakage current is directly proportional to the TFT channel width and is roughly one to two orders of magnitude larger per
unit channel width than in an $\alpha$-Si TFT [29] due to the smaller energy bandgap of poly-Si ($\sim 1.1$ eV compared to $\sim 1.6$ eV for $\alpha$-Si). It is important to note that substantially narrower poly-Si TFTs can be used to meet pixel-charging requirements (due to the higher carrier mobilities and shorter channel lengths), so that the leakage current of a (narrow) poly-Si pixel TFT will actually be fairly comparable to that of a (much wider) $\alpha$-Si TFT. In addition, several techniques have been demonstrated to provide substantial reductions in leakage current, including the use of offset-gate structures [30], secondary gate-induced drains [31], and multiple-gate TFTs [32], so that poly-Si TFTs can easily meet the sub-pA leakage requirements for gray-scale AMLCDs [29].

Poly-Si TFTs are clearly superior to $\alpha$-Si TFTs for application in high-density, high-performance AMLCDs. The major drawback of a conventional poly-Si TFT technology is its large thermal budget (typically tens of hours at temperatures $\geq 550^\circ$C), which makes it incompatible with commercially available large-area glass substrates due to glass shrinkage and warpage problems. (In comparison, an $\alpha$-Si TFT technology typically has a thermal budget of several hours at temperatures $\leq 350^\circ$C, and is therefore compatible with low-cost large-area glass substrates.) For low-cost AMLCD manufacturing, large-area substrates are needed in order to increase the number of displays per plate and thereby improve throughput and yield; the use of relatively inexpensive glass substrates is needed for maintaining low material cost. Quartz substrates are compatible with the high processing temperatures and long annealing times required for high-performance poly-Si TFT fabrication, but they are much more expensive than glass substrates, and are not as readily available in large ($e.g. \geq 360$ mm $\times$ 450 mm) sizes. It should be noted that new glasses which can withstand prolonged exposure to temperatures as high as $600^\circ$C are currently under development for use in poly-Si TFT technologies [33]; however, it is unlikely that the cost of these high strain-point materials will be competitive with that of Corning 7059 glass (which has a strain point of $593^\circ$C), the industry standard for $\alpha$-Si technologies.
Chapter 2. Applications of Polycrystalline Silicon Films in MOS Technologies

A preponderance of the thermal budget for a poly-Si TFT fabrication process is allotted to the channel-crystallization and dopant-activation annealing steps. Smooth, large-grained poly-Si films suitable for high-performance TFT applications are typically prepared by solid-phase crystallization of amorphous Si films, which requires very long annealing times (up to many tens of hours) at temperatures $\geq 550^\circ$C. The activation of implanted source/drain dopants also requires many hours at temperatures $\geq 550^\circ$C. Excimer-laser annealing is an alternative to conventional furnace annealing for crystallization and dopant activation [34, 35]. It is compatible with glass substrates, since the pulsed laser energy is absorbed only by the Si film, locally melting the Si for very short times (e.g., 200 ns), so that the substrate is not heated substantially. However, it tends to result in higher TFT leakage currents [35, 36], and its use necessitates a tradeoff between film quality (including uniformity) and process throughput [34, 37]. (Small-pitch scanning, two-step annealing, and substrate heating can each be used to improve the quality of the laser-crystallized film, at a cost to throughput.) Therefore, the use of laser annealing is not an ideal approach to alleviating the thermal-budget problem.

The development of a low-thermal-budget CMOS TFT technology which is compatible with large-area glass substrates is needed in order to make the low-cost manufacturing of high-performance, high-density AMLCDs viable in the future. The most significant contributions in this endeavor will likely be made by innovations in materials and processing which allow lower process temperatures to be used and/or higher process throughputs to be achieved, and which do not require the use of unconventional, expensive tools (such as laser-annealing equipment).

2.3 Summary

Poly-Si has many attractive properties, notably its compatibility with high temperatures and IC-fabrication processes, which make it very useful for IC applications. Its application as the gate-electrode material in MOS technologies has enabled the rapid
scale-down of device sizes for denser, more complex ICs. As the minimum feature size in CMOS technologies is scaled to well below 1 μm, however, the poly-Si work function becomes a serious problem, because it results in a either a severe tradeoff between NMOS and PMOS device performance or significantly increased process complexity. The high carrier mobilities which can be achieved in poly-Si (as compared with α-Si) make it attractive for application as the active layer in TFTs. However, poly-Si TFTs require large process thermal budgets, which cannot be afforded by very-high-density stacked-CMOS SRAM technologies and large-area (glass-substrate) electronics technologies. For these and other applications, a suitable alternative to poly-Si may ultimately be needed. Such a material would not only retain the desirable properties of poly-Si, but also possess a better-suited work function and allow significantly lower processing temperatures and/or shorter processing times to be used for deposition, crystallization, and dopant activation.
Chapter 3

Formation of $\text{Si}_{1-x}\text{Ge}_x$ Thin Films

The formation of $\text{Si}_{1-x}\text{Ge}_x$ thin films is described in this chapter. Two techniques are discussed: high-dose Ge implantation into silicon thin films, and deposition of $\text{Si}_{1-x}\text{Ge}_x$ by pyrolysis of silane ($\text{SiH}_4$) and germane ($\text{GeH}_4$) in a low-pressure chemical-vapor deposition (LPCVD) system.

3.1 Formation of Thin $\text{Si}_{1-x}\text{Ge}_x$ Films by Ge Implantation

Thin-film silicon-on-insulator (SOI) technologies are currently of great interest for very-large-scale integration (VLSI) because they can achieve better circuit performance and higher packing densities than conventional bulk-silicon technologies, for the same minimum feature size [38]. The formation of thin layers of $\text{Si}_{1-x}\text{Ge}_x$ by implantation of Ge was investigated, since this technique could potentially allow $\text{Si}_{1-x}\text{Ge}_x$ TFTs to be realized alongside conventional SOI MOSFETs. The implantation-based method was also chosen because of the widespread availability and relatively low cost of ion implantation (as compared to selective chemical vapor deposition or selective molecular-beam epitaxy). In this section, the results of this investigation are summarized.
Figure 3.1: Thermal oxide thickness as a function of Ge implant dose.

Bare silicon wafers (n-type, 5-10 Ω-cm, (100) orientation) were implanted with 60 keV $^{70}$Ge$^+$ ions to doses of $5 \times 10^{15}$, $1 \times 10^{16}$, $2 \times 10^{16}$, $4 \times 10^{16}$, or $6 \times 10^{16}$ cm$^{-2}$. The wafers were then oxidized in steam, at temperatures ranging from 800°C to 950°C, to entirely consume the originally implanted region of silicon and to “pile up” the Ge at the SiO$_2$/Si interface. During the oxidation process, the low diffusivity of Ge in silicon [39], coupled with the preferential segregation of the Ge into silicon, leads to the formation of a distinct, Ge-rich layer of Si$_{1-x}$Ge$_x$ at the rapidly oxidizing interface; this Si$_{1-x}$Ge$_x$ layer is epitaxially aligned with the silicon substrate [40, 41].

In order to determine the effect of Ge on the oxidation rate of silicon, the thicknesses of the silicon dioxide films were measured using an ellipsometer and also using a Nanospec interferometer. The ellipsometer and Nanospec measurements were in close agreement, and were very similar to thicknesses determined from capacitance measurements (Figure 3.1). It was found that Ge-implanted wafers oxidize more rapidly than an unimplanted wafer, and that the enhancement in oxide thickness increases with increasing implant dose (for a given oxidation time and temperature – see Figure 3.1) but decreases with increasing oxidation temperature (for a given implant
dose and oxidation time). These results corroborate the theory that the presence of Ge affects the interfacial reaction kinetics at the oxidizing interface, resulting in an enhancement in oxidation rate during the linear regime of the steady-state oxidation process described by the Deal-Grove model [41]. (The reduction in enhanced oxidation rate at higher temperatures is consistent with an increase in diffusion of Ge away from the oxidizing interface.)

The silicon dioxide films were next examined with an optical microscope under dark-field illumination. The oxides were found to be of poor quality, with noticeable pinholes. The density of pinholes was found to increase with increasing Ge implant dose, and to decrease with increasing oxidation temperature. The poor oxide quality was confirmed by electrical measurements of breakdown field, shown in Figure 3.2. The significant reduction in breakdown field for oxides grown on Ge-implanted Si (compared with oxides grown on virgin Si) has also been observed by other researchers [42]. Since the thermally grown oxide film is clearly unsuitable for either field-insulator or gate-dielectric applications, it would have to be removed and replaced by a deposited insulator in a device-fabrication process.

In order to determine the thickness of the Si$_{1-x}$Ge$_x$ layer formed at the interface between the silicon substrate and the silicon dioxide, wafer samples were analyzed by cross-sectional transmission electron microscopy (XTEM). It was found that the thickness of the Si$_{1-x}$Ge$_x$ layer increases with Ge implant dose, from 2 nm for an implant dose of $5 \times 10^{15}$ cm$^{-2}$ to approximately 25 nm for an implant dose of $6 \times 10^{16}$ cm$^{-2}$. Assuming that no Ge was incorporated into the oxide film, these results indicate that the average Ge mole fraction in the Si$_{1-x}$Ge$_x$ layers is $\sim$50%.

TEM was also used to characterize the physical defects associated with the Si$_{1-x}$Ge$_x$ layer. For the samples which were implanted with a dose $\geq 1 \times 10^{16}$ cm$^{-2}$, the characterizations showed that the Si$_{1-x}$Ge$_x$ layer is inhomogeneously strained, due to local reductions in strain via misfit dislocations located at the Si$_{1-x}$Ge$_x$/Si interface. The presence of misfit dislocations was verified by high-resolution electron microscopy (HREM). Stacking faults were also observed in most of the samples, with
Figure 3.2: SiO₂ breakdown field as a function of implanted Ge dose. The silicon substrate was implanted with Ge at 60 keV, then oxidized in steam at 900°C for 1 hour. The resultant oxide was etched back to its final thickness of ~30 nm before the Al gate-metal was deposited. Capacitors of sizes 200μm×200μm, 50μm×50μm, and 10μm×10μm were measured. The data shown are the average values for 10 measurements. (Standard deviation is less than 2 percent.)
higher densities for samples implanted with higher doses of Ge. From the HREM photographs, it was deduced that the nucleation of stacking faults occurred at the Si$_{1-x}$Ge$_x$/SiO$_2$ interface during the oxidation process, possibly due to the presence of super-saturated interstitial silicon atoms at that interface. These results clearly indicate that, in order to obtain a uniform, defect-free, strained layer of Si$_{1-x}$Ge$_x$, low Ge implant doses ($<1 \times 10^{16}$ cm$^{-2}$) must be used.

The interface roughness associated with the Si$_{1-x}$Ge$_x$ layer was also studied by HREM. It was found that both the roughness of the SiO$_2$/Si$_{1-x}$Ge$_x$ interface and the roughness of the Si$_{1-x}$Ge$_x$/Si interface increase with increasing implant dose, and also with increasing oxidation temperature, with the Si$_{1-x}$Ge$_x$/Si interface roughness increasing more dramatically. The increasing roughness of the SiO$_2$/Si$_{1-x}$Ge$_x$ interface with increasing implant dose may partially account for the observed increase in density of stacking faults with increasing implant dose, since surface roughness at the oxidizing interface can facilitate the nucleation of stacking faults. Since surface roughness is also known to reduce the effective carrier mobility in MOS devices, these HREM results indicate that lower dose Ge implants would be more desirable for MOS applications.

Secondary Ion Mass Spectrometry (SIMS), using a primary beam of 10 keV oxygen ions, was used to analyze samples of various wafers. Because of matrix effects, it was not possible to measure the absolute Ge concentration profile in the Si$_{1-x}$Ge$_x$ layer; in addition, because of "knock-on" and sputtering-induced roughness effects, the resolution of the SIMS method used was greater than 20 nm, which made it difficult to accurately determine the shape of the Ge concentration profile. However, trends in the variations of Si$_{1-x}$Ge$_x$-layer thickness and maximum Ge concentration could be determined by comparing the SIMS profiles of the Si$_{1-x}$Ge$_x$ layers for various Ge-implant doses and oxidation temperatures. From these comparisons, it was found that the peak Ge concentration in the Si$_{1-x}$Ge$_x$ layer does not vary significantly with oxidation temperature, although it increases dramatically with Ge implant dose; also, the thickness of the Si$_{1-x}$Ge$_x$ layer increases with oxidation temperature as well as
Figure 3.3: Ge profile width and peak concentration after steam oxidation at 800°C (determined from RBS data) as a function of implanted Ge dose.

with implant dose.

Rutherford Backscattering Spectrometry (RBS) analyses were performed on various wafer samples using 2.4 MeV He⁺ ions and a scattering angle of 170°. The depth resolution of the RBS method used is approximately 20 nm. Since the thickness of the Si₁₋ₓGeₓ layers in the various samples is (in general) smaller than the depth resolution of this analysis method, the Ge distribution profile once again could not be accurately determined; however, the integrated Ge dose in the Si₁₋ₓGeₓ layer could be estimated from the peak concentration and half-width of the RBS profile and was consistently found to be slightly greater than the implanted dose (an artifact of the measurement technique). Also, to within the detection limits of RBS, no Ge was detected in the silicon dioxide. It can thus be concluded from the RBS analyses that no Ge was lost to the silicon dioxide during the oxidation step. Comparison of the RBS profiles for various Ge-implant doses and oxidation temperatures confirmed the variation trends in peak Ge concentration and Si₁₋ₓGeₓ layer thickness observed by SIMS (Figures 3.3 and 3.4).
Figure 3.4: Ge profile width and peak concentration after steam oxidation (determined from RBS data) as a function of oxidation temperature.

Simple MOS capacitors were fabricated by the sputter-deposition and patterning of aluminum to form gates for capacitance-vs.-voltage (C-V) measurements. Prior to measurement, the samples were given a 30-minute forming-gas anneal at 400°C. For each sample, the capacitance was found to be relatively constant with applied voltage (which ranged from -35 V to 35 V), indicating that the Fermi level at the oxide/substrate interface is “pinned.” This pinning effect may be due to electrically active defects associated with the stacking faults which are known (from TEM analyses) to be present in the Si$_{1-x}$Ge$_x$/Si substrate. Since prior oxidation studies of Si$_{1-x}$Ge$_x$ have shown that oxides grown on bulk single-crystalline Si$_{1-x}$Ge$_x$ have high negative fixed charge and high interface trap density (near $10^{12}$ cm$^{-2}$ and $10^{12}$ cm$^{-2}$eV$^{-1}$, respectively) [43, 44], it is also possible that the (n-type) surfaces of the Si$_{1-x}$Ge$_x$/Si substrates are simply inverted. In any case, an oxide interface which is formed concomitantly with the piling-up of Ge at that interface is of insufficient quality for device applications.

In summary, Ge-rich Si$_{1-x}$Ge$_x$ films can be achieved by the implantation of Ge
into Si and subsequent steam oxidation to “snowplow” the implanted Ge into a thin layer. Both the interface and the bulk properties of the resultant SiO₂ film are poor; thus, this oxide would have to be replaced by a deposited dielectric, if the Si₁₋ₓGeₓ layer were to be used for MOS device applications. In order to obtain a low-defect Si₁₋ₓGeₓ layer with smooth interfaces to the overlying SiO₂ film and the underlying Si substrate, a low Ge-implant dose (< 1 × 10¹⁶ cm⁻²) must be used; however, the thickness (several nanometers) of a Si₁₋ₓGeₓ layer formed using such a low dose may be too small to have a significant effect on device conduction. In short, the implantation method is not well-suited to the formation of Si₁₋ₓGeₓ films for MOS applications, although the Si₁₋ₓGeₓ/Si heterostructures formed by this technique may be potentially useful for other applications [40].

3.2 Low-Pressure Chemical-Vapor Deposition of Si₁₋ₓGeₓ

Because Si₁₋ₓGeₓ films of significant Ge content are difficult to achieve by implantation of Ge into Si (due to the impractically high implant doses required), a Si₁₋ₓGeₓ deposition process was developed for this work. A conventional hot-wall LPCVD system, originally used for the deposition of poly-Si films, was modified to allow the deposition of Si₁₋ₓGeₓ films. (The only modification which was required was the installation of an additional gas line for the Ge source.) Si₁₋ₓGeₓ films were subsequently deposited onto oxidized Si wafers in this system (Figure 3.5), using silane (SiH₄) and germane (GeH₄) as the gaseous deposition sources, with no diluent gases. The characteristics of the deposition process are presented in this section.

Films were deposited onto 0.1 μm-thick thermally grown SiO₂ on 100 mm-diameter Si substrates, at temperatures ranging from 400°C up to 625°C. Because the LPCVD system does not have an independent pressure-control system, the deposition pressure
Chapter 3. Formation of $\text{Si}_{1-x}\text{Ge}_x$ Thin Films

Figure 3.5: Schematic of the LPCVD system used to deposit polycrystalline Si and $\text{Si}_{1-x}\text{Ge}_x$ films in this work.

varied with the total gas-flow rate and ranged from 0.1 torr up to 0.4 torr. The thicknesses of the deposited films were determined by using a masked etch and measuring the step height using a surface profilometer. A standard SF$_6$-plasma etch process was used to pattern the deposited films (Figure 4.9). Plots of film thickness vs. deposition time indicated that an initial delay exists in the deposition process. This incubation time increases with decreasing deposition temperature and also with increasing Ge content. For deposition temperatures $\geq 550^\circ$C, and for films with Ge content $<30\%$, the delay is fairly short ($< 1$ minute). For a 50\% Ge film deposited at 500$^\circ$C, the delay is $\sim 3$ minutes; at 450$^\circ$C, the delay is $\sim 20$ minutes. Other researchers have found that LPCVD $\text{Si}_{1-x}\text{Ge}_x$ films nucleate poorly on oxide [45]. It is likely that the $\text{Si}_{1-x}\text{Ge}_x$ deposition process occurs by the initial formation of a thin layer (monolayer) of Si on the oxide, followed by the growth of $\text{Si}_{1-x}\text{Ge}_x$ on this nucleation layer; this would account for the exponential dependence of the incubation time on deposition temperature, since Si deposition rate increases exponentially with temperature (see
Figure 3.6: Film deposition rate as a function of the inverse of deposition temperature, for various GeH₄ flow rates.

Figure 3.11).

Figure 3.6 is an Arrhenius plot of film deposition rate, for a SiH₄ flow rate of 100 sccm and several GeH₄ flow rates. At temperatures \( \leq 500^\circ \text{C} \), the deposition rate increases with increasing GeH₄ flow rate. However, at temperatures \( > 550^\circ \text{C} \), the deposition rate does not exhibit a strong dependence on GeH₄ flow rate, because it is limited by the mass transport of the germanium-containing deposition species to the deposition surface [46]. The uniformity of reaction-rate-limited deposition of Si\(_{1-x}\)Ge\(_x\) films was found to be comparable to that for Si films deposited in the same system (\( < \pm 5\% \) across a wafer, \( < \pm 10\% \) across a boat-load of 25 wafers).

The germanium contents in the deposited films were determined by Rutherford backscattering spectrometry (RBS). As shown in Figure 3.7, the amount of germanium incorporated into the Si\(_{1-x}\)Ge\(_x\) film decreases with increasing deposition temperature, for fixed SiH₄ and GeH₄ flow rates. As a result, the percentage of GeH₄ in
Chapter 3. Formation of $\text{Si}_{1-x}\text{Ge}_x$ Thin Films

Figure 3.7: Ge mole fraction in deposited $\text{Si}_{1-x}\text{Ge}_x$ film as a function of deposition temperature, for various $\text{GeH}_4$ flow rates.

the source which is required to achieve a specific Ge mole fraction in the deposited film increases (roughly linearly) with deposition temperature (Figure 3.8). This observation is consistent with previous findings of lower activation energies associated with germanium deposition compared to those associated with silicon deposition [46, 47]. The $\text{Si}_{1-x}\text{Ge}_x$ deposition rate is plotted as a function of Ge mole fraction in Figure 3.9, and can be seen to increase with increasing Ge content at temperatures below 600°C. This effect has been attributed to germanium-enhanced desorption of hydrogen from the deposition surface [48], and has been observed in other LPCVD systems [49] and also in an atmospheric-pressure deposition system [50].

If the growth rate in this deposition system were limited by the adsorption of Si and Ge growth species, and all of the adsorbing species competed for the same type of adsorption site, and all adsorbed Si- and Ge-containing species contributed to the growth rate, then the $\text{Si}_{1-x}\text{Ge}_x$ alloy growth rate $R$ could be simply modelled as

$$R = R_{\text{Si}} + R_{\text{Ge}},$$  \hspace{1cm} (3.1)
Figure 3.8: Percentage of GeH₄ in the gaseous deposition source required in order to attain a specific Ge mole fraction in the deposited Si₁₋ₓGeₓ film.

Figure 3.9: Film deposition rate as a function of Ge content.
where

\[ R_{\text{Si}} = K'_{\text{Si}}(1 - \phi)e^{-\frac{E_{\text{Si}}}{RT}} \]  

(3.2)

and

\[ R_{\text{Ge}} = K'_{\text{Ge}}(1 - \phi)e^{-\frac{E_{\text{Ge}}}{RT}} \]  

(3.3)

are the respective component growth rates of Si and Ge [47]. In Equations 3.2 and 3.3, \( K'_{\text{Si}} \) and \( K'_{\text{Ge}} \) are constants proportional to the partial pressures of SiH\(_4\) and GeH\(_4\), respectively, \((1 - \phi)\) is the fraction of available adsorption sites, \( E_{\text{Si}} \) and \( E_{\text{Ge}} \) are the respective activation energies associated with the deposition of Si and Ge, \( k \) is Boltzmann’s constant, and \( T \) is the absolute temperature. The Ge content in the deposited film, \( x \), would then be given by the equation

\[ \frac{x}{1 - x} = m \frac{P_{\text{GeH}_4}}{P_{\text{SiH}_4}} \]  

(3.4)

where \( m \) is a function only of temperature, and \( P_{\text{SiH}_4} \) and \( P_{\text{GeH}_4} \) are the partial pressures of silane and germane, respectively. The ratio of Ge to Si has been found increase linearly with increasing ratio of GeH\(_4\) flow rate to SiH\(_4\) flow rate, according to Equation 3.4, for Si\(_{1-x}\)Ge\(_x\) films deposited at temperatures between 570°C and 700°C in another LPCVD system [49]. Figure 3.10 shows the Ge:Si ratio as a function of the GeH\(_4\):SiH\(_4\) ratio for Si\(_{1-x}\)Ge\(_x\) films deposited in this work. The Ge content in the deposited films increases monotonically with increasing percentage of germane in the gaseous deposition source, but it clearly does not follow the linear relationship given by Equation 3.4, particularly for lower deposition temperatures. (Note that the best-fit lines for the data in Figure 3.10 do not intersect the origin.) This suggests that, for temperatures below ~600°C, the deposition rate is not limited by the adsorption of growth species, but is instead limited by other factors, such as gas-phase kinetics or surface nucleation [47]. Recently, a new model based on the sticking probability of Si and Ge precursors has been proposed to more accurately model the Ge content in LPCVD Si\(_{1-x}\)Ge\(_x\) films as a function of deposition temperature and GeH\(_4\) partial pressure [51].
Figure 3.10: Ge:Si ratio in the deposited film as a function of GeH₄:SiH₄ ratio in the gaseous deposition source, for various deposition temperatures.

Figure 3.11 is an Arrhenius plot of deposition rate, for films of various Ge mole fractions. The transition temperatures between polycrystalline- and amorphous-film deposition are delineated by the dotted line in this figure: above the dotted line, the films are deposited polycrystalline form; below the dotted line, the films are deposited in amorphous form. (The determinations of crystallinity were made by X-ray diffraction analyses.) Depending upon the Ge content, LPCVD Si₁₋ₓGeₓ films can be deposited in polycrystalline form at temperatures as low as 400°C, in contrast to LPCVD silicon films, which cannot be deposited in polycrystalline form at temperatures below ~575°C [52, 53]. At lower temperatures, the Si₁₋ₓGeₓ deposition rate is limited by surface reactions, with an activation energy ~1.5 eV; at higher temperatures, it is limited by mass-transport effects, with an activation energy less than 0.3 eV. The fact that polycrystalline Si₁₋ₓGeₓ films can be attained at temperatures well below 600°C is of significant importance in regard to large-area electronics applications, since the use of low-cost glass substrates limits processing temperatures to
Figure 3.11: Deposition rate as a function of the inverse of deposition temperature, for films of various Ge mole fractions.

below 600°C [54]. The substantial reduction in temperatures afforded by a Si$_{1-x}$Ge$_x$-based technology (in comparison with a Si-based technology) can alleviate problems associated with substrate warpage and shrinkage. It can be seen from Figure 3.11 that the deposition rate for amorphous-phase deposition decreases with increasing Ge content. This may be a cause for some concern, since amorphous-phase deposition and subsequent crystallization is the preferred method for preparing high-quality thin-film-transistor (TFT) films with low surface roughness, low strain, and high structural perfection [55]. Lower deposition rates not only result in lower throughput, but also exacerbate the problem of oxygen incorporation into the deposited films, resulting in retarded crystallization rates [56]. Since Si$_{1-x}$Ge$_x$ films incorporate oxygen more easily than Si films [57], higher Si$_{1-x}$Ge$_x$ deposition rates are needed to mitigate this problem. These can be achieved through the use of disilane (Si$_2$H$_6$) rather than silane as the silicon source gas [50].
3.3 Summary

Thin Si$_{1-x}$Ge$_x$ films can be formed by implantation of Ge into Si and subsequent oxidation in a steam ambient; however, these films are not of sufficient quality for MOS applications.

Conventional LPCVD equipment can be used to deposit Si$_{1-x}$Ge$_x$ films, using SiH$_4$ and GeH$_4$ as the source gases, with thickness uniformities comparable to those of Si films. The GeH$_4$:SiH$_4$ ratio required to obtain a specific Ge mole fraction in the deposited film increases predictably with Ge content and deposition temperature, and the deposition rate increases with Ge film content as well as with deposition temperature. Depending upon their Ge content, Si$_{1-x}$Ge$_x$ films can be deposited in polycrystalline form at temperatures as low as 400°C, because the transition temperature between polycrystalline- and amorphous-film deposition decreases with increasing Ge content. This reduction in temperature, along with the increase in deposition rate, makes Si$_{1-x}$Ge$_x$ films potentially attractive for applications in technologies which have limited "thermal budget" requirements.
Chapter 4

Properties of LPCVD $\text{Si}_{1-x}\text{Ge}_x$ Thin Films

This chapter covers the physical and electrical properties of LPCVD poly-$\text{Si}_{1-x}\text{Ge}_x$ films. First, the grain structure in poly-$\text{Si}_{1-x}\text{Ge}_x$ films described. Next, the issue of $\text{Si}_{1-x}\text{Ge}_x$ compatibility with modern silicon-based microelectronics fabrication processes is addressed. Finally, the results of characterization work on the resistivity, work function, and dopant-annealing behavior of heavily doped films are presented.

4.1 Physical Characterization of LPCVD $\text{Si}_{1-x}\text{Ge}_x$ Films

Various analytical techniques were employed in this work in order to study the physical properties of LPCVD $\text{Si}_{1-x}\text{Ge}_x$ films. X-ray diffraction (XRD) was used to characterize crystal structure, Transmission Electron Microscopy (TEM) was used to study grain microstructure, and Secondary Ion Mass Spectrometry (SIMS) was used to determine contaminant concentration levels.
4.1.1 X-Ray Diffraction Analysis

XRD analyses of Si$_{1-x}$Ge$_x$ films were conducted using a generalized focusing diffractometer [58] operating in the Seemann-Bohlin mode in order to eliminate diffraction from the Si substrate, with a fixed incident-beam angle ($\alpha$) of 7°. The XRD step-scans of polycrystalline Si$_{1-x}$Ge$_x$ films were each found to exhibit singular peaks, corresponding to the {111}, {220} and {311} planes (Figure 4.1a), characteristic of a material with the diamond-cubic crystal structure. The fact that dual peaks are not seen indicates that the deposited films are composed of Si$_{1-x}$Ge$_x$ alloy material, rather than clusters of Ge or Ge-rich material embedded in a Si matrix. The locations of the singular peaks are located in-between those of poly-Si and poly-Ge, and are shifted more towards those of pure Ge for the films with higher Ge content (Figure 4.1b). The interplanar spacings, $d_{hkl}$, can be determined from Bragg’s law:

$$n\lambda = 2d_{hkl}\sin\Theta,$$

with $n=1$, and are plotted in Figure 4.2 for films deposited at various temperatures. These spacings vary proportionately with the amount of Ge in the film, indicating that Vegard’s law [59] can be used to estimate the Ge mole fraction in poly-Si$_{1-x}$Ge$_x$ films from XRD measurements. In Figure 4.3, the Ge mole fractions estimated from {220} peak locations are plotted against the actual Ge mole fractions (as determined by RBS). The data indicate that XRD can be used to consistently determine Ge content to within 2 atomic percent. It is of interest to note that, unlike the $d_{220}$ values, the $d_{111}$ values are noticeably larger than those predicted by Vegard’s law. This indicates that some lattice distortion exists and therefore strain is present in the as-deposited poly-Si$_{1-x}$Ge$_x$ films.

Although determinations of film crystallinity could be made by XRD analysis, the focusing geometry precluded accurate determinations of texture (i.e. preferred orientation) and measurements of strain [58]. However, comparisons of XRD data for films deposited at different temperatures indicate that a maximum in {110} texture occurs at intermediate deposition temperatures (e.g. $\sim$500°C for Si$_{0.5}$Ge$_{0.5}$ films), and that
Figure 4.1: X-ray diffraction data for ~220-nm-thick poly-Si$_{1-x}$Ge$_x$ films deposited at 625°C: (a) diffraction intensity as a function of Bragg angle 2θ; (b) relative location of diffraction peaks as a function of film Ge content.
Chapter 4. Properties of LPCVD $Si_{1-x}Ge_x$ Thin Films

![Graph showing interplanar spacings as a function of Ge mole fraction for different deposition temperatures.]

Figure 4.2: Interplanar spacings in as-deposited poly-$Si_{1-x}Ge_x$ films as a function of Ge content, for several deposition temperatures.
Figure 4.3: XRD-estimated Ge mole fractions in as-deposited poly-Si$_{1-x}$Ge$_x$ films versus that determined by RBS, for several deposition temperatures.

the \{111\} texture increases monotonically with deposition temperature (Figure 4.4); these variations in texture are analogous to those observed for poly-Si films [60].

4.1.2 Transmission Electron Microscopy Analysis

Plan-view transmission electron micrographs of polycrystalline Si$_{1-x}$Ge$_x$ films deposited at 625°C are shown in Figures 4.6 and 4.7. The equiaxed grain structure of poly-Si$_{1-x}$Ge$_x$ films is very similar to that of poly-Si films (see [61], for instance). At any given deposition temperature, the average grain size is larger in films with higher Ge content: for example, the average grain sizes (determined using the grain-boundary-crossing technique [9]) in ~0.25 μm-thick films deposited at 625°C are 50 nm, 150 nm, 250 nm, and 350 nm for films with 0%, 26%, 46%, and 56% Ge, respectively. Diffraction patterns exhibit only one set of rings characteristic of a material with the diamond-cubic crystal structure (Figure 4.7 inset), corroborating XRD-analysis indications that the deposited films are composed of Si$_{1-x}$Ge$_x$ alloy material.
Chapter 4. Properties of LPCVD $\text{Si}_{1-x}\text{Ge}_x$ Thin Films

Figure 4.4: Comparison of X-ray diffraction data for $\text{Si}_{0.5}\text{Ge}_{0.5}$ films deposited at 450°C, 500°C, 550°C, and 600°C. The respective film thicknesses are 156 nm, 486 nm, 520 nm, and 363 nm, and the respective deposition rates were 4 nm/min, 16 nm/min, 26 nm/min, and 24 nm/min.
Figure 4.5: Maximum peak-to-peak surface roughness of as-deposited poly-Si and poly-SiGe films, normalized to film thickness, as a function of deposition temperature.

Because the microstructure of polycrystalline thin films profoundly affects the electrical performance of devices fabricated within these films, cross-sectional TEM (XTEM) analysis was used to elucidate the details of poly-Si$_{1-x}$Ge$_x$ grain structure across the depth of the film. The representative XTEM micrograph shown in Figure 4.8 reveals that poly-Si$_{1-x}$Ge$_x$ grains are columnar in the direction perpendicular to the film surface, and that these grains have a low density of microtwins compared to undoped poly-Si grains [62]. The low density of microtwins is further evidenced by the absence of radial streaking in the corresponding diffraction pattern (Figure 4.7 inset). The structure of Si$_{1-x}$Ge$_x$ films deposited in polycrystalline form more closely resembles that of phosphorus-doped poly-Si films[9]. It should be noted that the surface roughness of poly-Si$_{1-x}$Ge$_x$ films is slightly higher than that of poly-Si films deposited at the same temperature, in correlation with the average grain size (Figure 4.5); smoother films are obtained by lowering the deposition temperature. Its larger grain sizes and lower intragranular-defect densities, coupled with its low-temperature-processing capability, make poly-Si$_{1-x}$Ge$_x$ a promising material for
Figure 4.6: Plan-view TEM micrographs of (a) \(\sim230\) nm-thick poly-Si\(_{0.74}\)Ge\(_{0.26}\) film, and (b) \(\sim310\) nm-thick poly-Si\(_{0.44}\)Ge\(_{0.56}\) film, as deposited at 625°C. The respective deposition pressures were 0.15 torr and 0.19 torr; the respective deposition rates were 8.8 nm/min and 9.6 nm/min.

various TFT applications such as high-density memories [63] and large-area integrated circuits [54].

4.1.3 Secondary Ion Mass Spectrometry Analysis

Contaminants can be incorporated into a growing film during the LPCVD process unless stringent precautions are taken. Impurities such as carbon, nitrogen, and oxygen in amorphous silicon films have been shown to significantly retard the crystallization process [64], and can be expected to have similarly deleterious effects on Si\(_{1-x}\)Ge\(_x\) films, thereby degrading the electrical characteristics of devices fabricated in these films. Furthermore, the presence of oxygen in Si\(_{1-x}\)Ge\(_x\) films has been shown to detrimentally affect minority-carrier lifetime [57]. SIMS analyses were performed using 14.5 keV Cs\(^+\) primary ion bombardment with negative secondary ion spectrometry. In Table 4.1, the measured levels of impurity contamination for amorphous
Figure 4.7: Plan-view TEM micrograph of \(~250\) nm-thick poly-Si_{0.54}Ge_{0.46} film, as deposited at \(625^\circ\)C. The deposition pressure was 0.17 torr. and the deposition rate was 8.8 nm/min.
silicon and Si$_{0.8}$Ge$_{0.2}$ films are compared. It can be seen from this table that the level of oxygen contamination is several times higher in the Si$_{0.8}$Ge$_{0.2}$ film than in the Si film, while the levels of carbon and nitrogen contamination are lower in the Si$_{0.8}$Ge$_{0.2}$ film than in the Si film. The higher level of oxygen in the Si$_{0.8}$Ge$_{0.2}$ film may be partially attributed to the lower deposition temperature, since vacuum requirements become more stringent as deposition temperature is decreased [65]. Nonetheless, it can be expected that the levels of oxygen will be higher for films with even higher Ge content [57]. Since the crystallization of amorphous silicon films is adversely affected for oxygen concentrations greater than $\sim 1 \times 10^{20}$ cm$^{-3}$ [64], the issue of oxygen incorporation may be especially critical for Si$_{1-x}$Ge$_x$ films. It should be noted that the LPCVD system used in this work could only achieve base pressures $\sim 40$ millitorr. The incorporated-impurity levels should be significantly lower for systems which can achieve lower base pressures ($\ll 10^{-3}$ torr).
Table 4.1: Levels of impurity contamination in LPCVD films, as determined from SIMS analyses. The film deposition rates were 1.9 nm/min; the deposition temperatures were 550°C and 490°C, and deposition pressures were 0.20 torr and 0.29 torr, for Si and Si$_{0.8}$Ge$_{0.2}$, respectively.

<table>
<thead>
<tr>
<th>IMPURITY ELEMENT</th>
<th>CONCENTRATION (cm$^{-3}$) in Si</th>
<th>CONCENTRATION (cm$^{-3}$) in Si$<em>{0.8}$Ge$</em>{0.2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>O</td>
<td>$1.4 \times 10^{19}$</td>
<td>$4 \times 10^{19}$</td>
</tr>
<tr>
<td>H</td>
<td>$5 \times 10^{18}$</td>
<td>$8 \times 10^{18}$</td>
</tr>
<tr>
<td>C</td>
<td>$2.2 \times 10^{18}$</td>
<td>$1.5 \times 10^{18}$</td>
</tr>
<tr>
<td>N</td>
<td>$3 \times 10^{16}$</td>
<td>$9 \times 10^{15}$</td>
</tr>
</tbody>
</table>

4.2 Compatibility of Poly-Si$_{1-x}$ Ge$_x$ with Si Processing Techniques

Silicon and germanium are each etched in flourine-based plasmas[66]. In this work, poly-Si$_{1-x}$ Ge$_x$ films were etched in a SF$_6$/Freon 115 plasma, in a Drytek DRIE100 Plasma Etcher. The etch rate is plotted in Figure 4.9 for Si$_{1-x}$ Ge$_x$ films deposited at various temperatures, and can be seen to increase slightly with Ge content. This increase is not as large as that which has been found for epitaxial strained Si$_{1-x}$ Ge$_x$ thin films on Si(100), which suggests that it is simply due to the greater gasification rate of Ge atoms and that Si atoms and Ge atoms are removed from the Si$_{1-x}$ Ge$_x$ surface independently, at rates measured for the pure elements for the same plasma conditions [67].

Germanium oxides are water-soluble [68]; consequently, germanium is etched in oxidizing solutions [69, 70]. The compatibility of poly-Si$_{1-x}$ Ge$_x$ films with the standard chemical solutions used in silicon integrated-circuit fabrication is therefore a potential issue. Tests were conducted to determine the effects of the following wet-cleaning processes on poly-Si$_{1-x}$ Ge$_x$ films: photoresist strip (20 minutes @ 120°C in 10:1 H$_2$SO$_4$:H$_2$O$_2$); organic clean (10 minutes @ 90°C in 4:1 H$_2$SO$_4$:H$_2$O$_2$); metallic clean (10 minutes @ 70°C in 1:1:5 HCl:H$_2$O$_2$:H$_2$O); and oxide etch (30 seconds in 50:1 HF).
Chapter 4. Properties of LPCVD $\text{Si}_{1-x}\text{Ge}_x$ Thin Films

Figure 4.9: Plasma etch rates of poly-$\text{Si}_{1-x}\text{Ge}_x$ films as a function of the Ge mole fraction in the film.

Films with Ge content below 60% were not affected by these baths; however, films with higher Ge content were etched in strong oxidizing solutions (i.e. $\text{H}_2\text{SO}_4$:$\text{H}_2\text{O}_2$ baths). Poly-$\text{Si}_{1-x}\text{Ge}_x$ films with Ge content greater than $\sim$30% have been found to be etched in the standard RCA clean "SC1" bath (1:1:5 $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$:$\text{H}_2\text{O}$) [71]. Since germanium is not etched by nonoxidizing acids and bases [68], no other chemical baths were tested in this work. For films with high Ge content, a thin capping layer of silicon (which can be deposited in-situ) should be sufficient to protect the $\text{Si}_{1-x}\text{Ge}_x$ from being etched in oxidizing solutions.

In this work, $\text{Si}_{1-x}\text{Ge}_x$ film thickness and deposition uniformity were monitored using a Nanometrics Nanospec interferometric measurement system. The Nanospec measurements were calibrated by profilometer measurements obtained with a Sloan Dektak IIA Surface Profile Measuring System. The relative index of refraction of poly-$\text{Si}_{1-x}\text{Ge}_x$ (normalized to that of poly-Si) is defined here as

$$n_{r,\text{relative}} = \frac{d_{\text{Nanospec}}}{d_{\text{Dektak}}}$$

where $d_{\text{Nanospec}}$ and $d_{\text{Dektak}}$ are the film thicknesses as measured by the Dektak and
Figure 4.10: Index of refraction, relative to that of poly-Si, of poly-Si$_{1-x}$Ge$_x$ films, as a function of the Ge mole fraction in the film.

the Nanospec (assuming $n_f = n_{f,poly-Si}$), respectively. $n_{f,relative}$ is plotted in Figure 4.10 as a function of Ge content, and can be seen to generally increase with Ge content. This is to be expected, since the refractive index of Ge is significantly higher than that of Si.

### 4.3 Electrical Properties of Heavily Doped Poly-Si$_{1-x}$Ge$_x$ Thin Films

#### 4.3.1 Resistivity and Hall Measurement

To study the resistivity of heavily doped $p$-type ($p^+$) and $n$-type ($n^+$) films as a function of Ge content, polycrystalline Si$_{1-x}$Ge$_x$ films 0.3 $\mu$m thick were implanted with either boron or phosphorus, at a dose of $4 \times 10^{15}$ cm$^{-2}$, and then annealed for 40 minutes at 900°C in argon. Implant energies of 20 keV and 60 keV were used for boron and phosphorus, respectively, and the resultant film resistivities are plotted
in Figure 4.11. The resistivities of the boron-doped poly-Si$_{1-x}$Ge$_x$ films are all substantially lower than the resistivity of the poly-Si film, decreasing with increasing Ge content. In contrast, the resistivities of the phosphorus-doped poly-Si$_{1-x}$Ge$_x$ films decrease only slightly with increasing Ge content for Ge mole fractions below $\sim$45%, and increase considerably for higher Ge mole fractions. Hall measurements performed on the p$^+$ films indicate that boron activation and hole mobility each increase significantly with Ge content (Figure 4.12), to account for the decrease in film resistivity seen in Figure 4.11. Hall measurements performed on the n$^+$ films show that, for films with low Ge content, phosphorus activation and electron mobility each increase slightly with increasing Ge content, reaching peaks at 35% Ge (Figure 4.13). For films with higher Ge content, a large drop in phosphorus activation and a concomitant decrease in electron mobility account for the large increase in resistivity seen in Figure 4.11. The drop in activation may be the result of increased phosphorus segregation to the grain boundaries. A more detailed study of phosphorus activation behavior will be discussed in a separate report [72].
Figure 4.12: Dopant activation (based on Hall measurement of free-carrier concentration) and Hall hole mobility for heavily boron-doped poly-Si$_{1-x}$Ge$_x$ films.

Figure 4.13: Dopant activation (based on Hall measurement of free-carrier concentration) and Hall electron mobility for heavily phosphorus-doped poly-Si$_{1-x}$Ge$_x$ films.
4.3.2 Rapid Thermal Annealing Behavior of Boron-Implanted Films

Rapid thermal annealing (RTA) was used to study the dependence of film resistivity on boron implant dose and anneal temperature. Si$_{1-x}$Ge$_x$ films 0.25 μm thick were implanted with various doses of boron, at an energy of 20 keV, and then annealed for 30 seconds each at successively higher temperatures. The resistivity is plotted as a function of the final anneal temperature for films of different Ge contents in Figure 4.14, for an implant dose of $1 \times 10^{15}$ cm$^{-2}$. It is evident that the anneal temperature required to activate the boron decreases dramatically as the Ge content in the film increases; for example, the resistivity of the Si$_{0.48}$Ge$_{0.52}$ film annealed for 30 seconds at 500°C is half that of the Si film annealed for 30 seconds at 900°C and 1000°C. Alternatively, much lower implant doses of boron can be used for poly-Si$_{1-x}$Ge$_x$ films than for poly-Si films to achieve the same film resistivity (Figure 4.15). For the application of Si$_{1-x}$Ge$_x$ as a gate-electrode material, these reductions in required dose and anneal temperature can help to alleviate the problem of boron diffusion through the thin gate oxide in a submicron boron-doped gate CMOS technology [73].

4.3.3 Work Function

A comparison of the conduction-band and valence-band energy levels in bulk crystalline Si, Si$_{1-x}$Ge$_x$ and Ge materials is shown in Figure 4.16 [74]. (The energy levels in Si$_{1-x}$Ge$_x$ are assumed to be intermediate to those in Si and Ge.) Si and Ge have similar electron affinities; however, Ge has a much smaller bandgap. Therefore, a relatively large energy difference ($> 0.5$ eV) exists between the valence-band edges of Si and Ge. The work function qΦ is defined to be the difference between the free-electron (vacuum) energy $E_o$ and the Fermi level $E_f$. Since the Fermi level is close to the conduction band in an $n$-doped semiconductor, whereas it is close to the valence band in a $p$-doped semiconductor, the work function of $n^+$ Si$_{1-x}$Ge$_x$ can be expected to decrease only slightly with increasing Ge content, whereas the work
Figure 4.14: Resistivity of poly-Si$_{1-x}$Ge$_x$ films implanted with boron (dose = $1 \times 10^{15}$ cm$^{-2}$ @ 20 keV) and then annealed for 30 seconds each at successively higher temperatures.

Figure 4.15: Resistivity of poly-Si$_{1-x}$Ge$_x$ films (annealed for 30 seconds at 600$^\circ$C) as a function of boron implant dose.
function of p⁺ Si₁₋ₓGeₓ can be expected to decrease noticeably with increasing Ge content. In order to characterize the change in work function for n⁺ and p⁺ polycrystalline Si₁₋ₓGeₓ films as a function of Ge content, metal-oxide-semiconductor (MOS) capacitors of various gate-oxide thicknesses were fabricated on n-type silicon wafers using n⁺ and p⁺ poly-Si₁₋ₓGeₓ films as the gate material (Figure 4.17). Details of the fabrication process are given in Table 4.3.3. The flat-band voltages for the various capacitors were determined from high-frequency capacitance-versus-voltage (C-V) measurements, and are plotted as a function of gate-oxide thickness (dOX) in Figure 4.18. The "metal-to-semiconductor" work-function difference Φ_MS is defined to be the difference in the work functions of the gate material and the semiconducting
### Table 4.2: Fabrication process for poly-Si$_{1-x}$Ge$_x$-gate capacitor structures

<table>
<thead>
<tr>
<th>Step</th>
<th>Procedure</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Starting Material: (100), n-type, 5-10 ohm-cm, 4-inch silicon wafers</td>
</tr>
<tr>
<td>1</td>
<td>Backside Implant: arsenic implant – 100 keV, 1 x 10$^{16}$ cm$^{-2}$</td>
</tr>
<tr>
<td>2</td>
<td>Thermal Oxidation: 10' dry /40' wet /10' dry @ 1000°C ; 250 nm</td>
</tr>
<tr>
<td>3</td>
<td>Anneal: 60' @ 1000°C in Ar</td>
</tr>
<tr>
<td>4</td>
<td>SiO$_2$ Etchback: 10:1 H$_2$O:HF; final SiO$_2$ thicknesses: 50 nm - 250 nm</td>
</tr>
<tr>
<td>5</td>
<td>Poly-Si$_{1-x}$Ge$<em>x$ Deposition (by LPCVD): $T</em>{deposition} = 625$°C ; 300 nm</td>
</tr>
<tr>
<td>6</td>
<td>Poly-Si$_{1-x}$Ge$_x$ Doping: p$^+$: Boron implant – 20 keV, 4 x 10$^{16}$ cm$^{-2}$; n$^+$: Phosphorus implant – 60 keV, 1 x 10$^{16}$ cm$^{-2}$</td>
</tr>
<tr>
<td>7</td>
<td>SiO$_2$ Deposition (LTO): @ 400°C; 30 nm</td>
</tr>
<tr>
<td>8</td>
<td>Implant Anneal: 40' @ 900°C in Ar</td>
</tr>
<tr>
<td>9</td>
<td>SiO$_2$ Etch: 50:1 H$_2$O:HF, until hydrophobic</td>
</tr>
<tr>
<td>10</td>
<td>Poly-Si$_{1-x}$Ge$_x$ Photolithography (capacitor mask)</td>
</tr>
<tr>
<td>11</td>
<td>Poly-Si$_{1-x}$Ge$_x$ Etch: 50 sccm SF$_6$, 50 sccm C$_2$ClF$_5$, 150 mT, 375 W</td>
</tr>
<tr>
<td>12</td>
<td>Backside Poly-Si$_{1-x}$Ge$_x$ Etch: 50 sccm SF$_6$, 50 sccm C$_2$ClF$_5$, 150 mT, 375 W</td>
</tr>
<tr>
<td>13</td>
<td>Backside SiO$_2$ Etch: 6:1 BOE, until hydrophobic</td>
</tr>
<tr>
<td>14</td>
<td>Forming-Gas Anneal: 30' @ 400°C</td>
</tr>
</tbody>
</table>

![Graph](image)

**Figure 4.18:** Flat-band voltage versus gate-oxide thickness for poly-Si$_{1-x}$Ge$_x$ gate capacitors.
Figure 4.19: Gate-to-semiconductor work function difference for poly-$\text{Si}_{1-x}\text{Ge}_x$-gate capacitors, extrapolated from measurements of flat-band voltage versus gate-oxide thickness.

substrate,

$$\Phi_{MS} = \Phi_M - \Phi_S,$$

and it can be extrapolated from flat-band data according to the equation

$$V_{FB} = \Phi_{MS} - \frac{Q_f'}{C'_{ox}},$$  \hspace{1cm} (4.1)

where $V_{FB}$ is the flat-band voltage, $Q_f'$ is the interface fixed charge areal density, and $C'_{ox}$ is the oxide capacitance per unit area, assuming that negligible mobile ions or oxide trapped charges exist [74]. Values of $\Phi_{MS}$ extrapolated from the data in Figure 4.18 are plotted in Figure 4.19. Since $Q_f'$ in Equation 4.1 must be a constant in order to obtain meaningful values for $\Phi_{MS}$, each data point was extrapolated from $V_{FB}$ vs. $d_{ox}$ data obtained on a single wafer, to ensure that $Q_f'$ was the same for all of the data points corresponding to a specific gate material. (The midgap interface trap density was determined from quasi-static $C-V$ measurements, and was verified to be the same for all capacitors located on a single wafer.) $Q_f'$ was found to vary
somewhat from wafer to wafer; the value of 4 x 10^{10} \text{ cm}^{-2} \text{ given in Figure 4.19 is the average value for all of the wafers included in this experiment.}

The $\Phi_{MS}$ data indicate that the work function of p+ poly-Si$_{1-x}$Ge$_x$ decreases significantly as the Ge content is increased (e.g. by more than 0.4 Volts from 0% Ge to 56% Ge), whereas the work function of n+ poly-Si$_{1-x}$Ge$_x$ decreases only slightly, as expected. Since the capacitor-gate films in this experiment are degenerately doped, the Fermi level can be assumed to represent the valence-band energy in the p+ films, and the Fermi level can be assumed to represent the conduction-band energy in the n+ films. Therefore, the $\Phi_{MS}$ data show that the energy bandgap in polycrystalline Si$_{1-x}$Ge$_x$ decreases with increasing Ge content primarily because of a change in the valence-band energy, as in single-crystalline Si$_{1-x}$Ge$_x$ material [75, 76]. This reduction in bandgap (as determined from changes in $\Phi_{MS_{p+}} - \Phi_{MS_{n+}}$) is plotted in Figure 4.20. For the 26% Ge film, the change in bandgap is close to that measured for unstrained single-crystalline Si$_{1-x}$Ge$_x$ material [77]; however, for the 56% Ge film, it is more similar to that seen for strained single-crystalline Si$_{1-x}$Ge$_x$ material [76, 78, 79]. The presence of strain in poly-Si$_{1-x}$Ge$_x$ films is corroborated by the X-ray diffraction results presented in Section 4.1.1.

4.4 Summary

Analyses of LPCVD Si$_{1-x}$Ge$_x$ films by X-ray diffraction and transmission electron microscopy show that these films are composed of alloy material, rather than clusters of Ge embedded in a Si matrix. Poly-Si$_{1-x}$Ge$_x$ grains are columnar in structure and have a relatively low density of microtwins, and their average size is larger than that of grains in poly-Si films deposited at the same temperature. Because of its larger grain sizes and lower defect densities, poly-Si$_{1-x}$Ge$_x$ is a potentially attractive alternative to poly-Si for thin-film transistor (TFT) applications.

Si$_{1-x}$Ge$_x$ films can be etched using a conventional SF$_6$-based plasma-etch process, at slightly higher rates than for poly-Si films. The practical etch rates, along with
Figure 4.20: Reduction in poly-Si$_{1-x}$Ge$_x$ energy bandgap as a function of Ge content. Published measurements of $\Delta E_g$ for unstrained single-crystalline Si$_{1-x}$Ge$_x$ [77] and calculations for $\Delta E_g$ in strained single-crystalline Si$_{1-x}$Ge$_x$ [78] are also shown for reference.

the well-characterized deposition rates (presented in Chapter 3), make the formation and patterning of poly-Si$_{1-x}$Ge$_x$ films very controllable processes. Films with less than 60% Ge content are not affected by various chemical solutions typically used in silicon-wafer processing. Thus, poly-Si$_{1-x}$Ge$_x$ is compatible with standard VLSI fabrication processes, and its use should not introduce significant additional process complexity into a Si-based technology.

Poly-Si$_{1-x}$Ge$_x$ films can be heavily doped p-type to achieve resistivities significantly lower than that achievable in p-type poly-Si films. The resistivity of n$^+$ poly-Si$_{1-x}$Ge$_x$ films with low Ge content (< 45%) is only slightly reduced from that of n$^+$ poly-Si; films with higher Ge content exhibit substantially higher resistivities. The lower p$^+$ film resistivities are the consequence of substantial increases in boron activation and hole mobility which accompany increases in Ge content, while the higher n$^+$ film resistivities are the consequence of significantly reduced phosphorus activation in high-Ge-content films. Considerably lower temperatures ($\sim$500$^\circ$C) can be
used to anneal boron-implanted poly-Si$_{1-x}$Ge$_x$ films, and lower boron implant doses can be used to obtain low resistivities in poly-Si$_{1-x}$Ge$_x$ films, compared to poly-Si films. The work function of p$^+$ poly-Si$_{1-x}$Ge$_x$ decreases significantly (by up to $\sim$0.4 Volts), whereas the work function of n$^+$ poly-Si$_{1-x}$Ge$_x$ decreases only slightly, as Ge content is increased. An estimate of the energy bandgap reduction in a 56\% Ge film (from p$^+$-n$^+$ work-function difference calculations) indicates that it is similar to the reduction observed for strained single-crystalline Si$_{0.44}$Ge$_{0.56}$ and thus provides some evidence of strain in high-Ge-content poly-Si$_{1-x}$Ge$_x$ films. The electrical properties of poly-Si$_{1-x}$Ge$_x$ make it a potentially favorable alternative to poly-Si for applications such as the p$^+$ gate material in MOS technologies and the active layer for p-channel TFTs.
Chapter 5

Polycrystalline Si$_{1-x}$Ge$_x$: A New Gate-Electrode Material

In this chapter, the application of Si$_{1-x}$Ge$_x$ as a gate-electrode material in complementary metal-oxide-semiconductor (CMOS) technologies is discussed. Poly-Si$_{1-x}$Ge$_x$ is demonstrated to be a promising alternative to poly-Si for this application due to its adjustable work function and lower-temperature-processing compatibility.

5.1 A Variable-Work-Function Gate Material for Submicrometer CMOS Technologies

Polycrystalline silicon (poly-Si) is the material traditionally used for the gate electrode in CMOS technologies. It must be degenerately doped, either heavily $n$-type ($n^+$) or heavily $p$-type ($p^+$), in order to avoid gate-depletion effects [80, 81, 82] and to achieve reasonably low resistivities for minimal $RC$ delays in circuit operation. The work function of $n^+$ poly-Si is relatively low ($\sim$4.15 eV), so that if it were to be used as the gate material, both the $n$-channel (NMOS) and the $p$-channel (PMOS) devices would require $p$-type (e.g. boron) channel implants in order to achieve proper threshold voltages for low-voltage very-large-scale-integration (VLSI) applications [12]. The
required PMOS threshold-adjustment implant is large enough to form a p-n junction in the surface region ("buried-channel" structure), making the PMOS device more susceptible to short-channel effects such as threshold-voltage lowering and poor OFF-state characteristics than a surface-channel device. Alternatively, the work function of p+ poly-Si is relatively high (≈5.25 eV), so that if it were to be used as the gate material, buried-channel NMOS devices would result.

As the device dimensions in single-crystalline CMOS technologies are reduced to the deep-submicrometer regime, the use of buried-channel devices becomes increasingly problematic. Several techniques have been suggested to overcome these problems, including the use of dual n+/p+-doped gates [5], and the use of a direct tungsten gate [6]. Although these alternatives provide surface-channel NMOS and PMOS devices, they have practical limitations (i.e. lateral dopant diffusion in the connected n+ and p+ gates causing threshold-voltage instabilities [5], and incompatibility of tungsten with Si fabrication processes) which make them difficult to implement in manufacturing. The investigation of poly-Si$_{1-x}$Ge$_x$ as an alternative to poly-Si for CMOS gate-electrode applications was prompted by the need for a material with a better-suited work function. In this work, a CMOS technology is proposed which uses a single p+ variable-work-function poly-Si$_{1-x}$Ge$_x$ gate material to achieve both NMOS and PMOS surface-channel devices.

5.1.1 Basic Principles of Gate Work-Function Engineering

The impact of the gate work function on NMOS and PMOS device design can be understood by considering the classical equation for MOS threshold voltage:

$$V_T = \Phi_{MS} - \frac{Q_f}{C_{ox}} + 2\phi_f - \frac{Q_d(2\phi_f)}{C'_{ox}},$$

(5.1)

which assumes that negligible amounts of mobile ions or trapped charges exist in the gate oxide, and that the substrate bias is zero. In Equation 5.1, $\Phi_{MS}$ is the metal-to-semiconductor work-function difference, $Q_f$ is the areal density of fixed charge at the oxide interface, $C'_{ox}$ is the oxide capacitance per unit area, $\phi_f$ is the semiconductor
Fermi potential, and $Q_d$ is the depletion-charge density in the semiconductor when the surface is strongly inverted:

$$\phi_f = \begin{cases} \frac{kT}{q} \ln \left( \frac{N_a}{n_i} \right) & \text{for } n\text{-channel devices} \\ -\frac{kT}{q} \ln \left( \frac{N_d}{n_i} \right) & \text{for } p\text{-channel devices} \end{cases}$$

(5.2)

$$Q_d = \begin{cases} -\sqrt{4\varepsilon_s q N_a |\phi_f|} & \text{for } n\text{-channel devices} \\ \sqrt{4\varepsilon_s q N_d |\phi_f|} & \text{for } p\text{-channel devices} \end{cases}$$

(5.3)

In Equations 5.2 and 5.3, $kT/q$ is the thermal voltage, $N_a$ and $N_d$ are the acceptor and donor dopant concentrations in the NMOS and PMOS channel regions, respectively, and $\varepsilon_s$ is the permittivity of the semiconductor. In modern MOS technologies, the fixed oxide charge is very small (e.g. in the low $10^{10}$ cm$^{-2}$ range) and does not appreciably affect the threshold voltage. For example, a charge density of $5 \times 10^{10}$ cm$^{-2}$ would contribute a voltage of less than 35 mV for a 15 nm-thick gate oxide. Therefore, the second term on the right-hand side of Equation 5.1 can be neglected for simplicity. The room-temperature threshold voltage is plotted as a function of the channel dopant concentration in Figure 5.1 for silicon NMOS and PMOS devices; data for various gate-oxide thicknesses and gate materials are shown. In this figure, the work function of p$^+$ poly-Si$_{0.5}$Ge$_{0.5}$ is conservatively taken to be 0.3 V lower than that of p$^+$ poly-Si, although the experimental data shown in Figure 4.19 suggest that the work-function difference is closer to 0.4 V.

Enhancement-mode devices are necessary for proper CMOS circuit operation; for low-voltage (e.g. 5-Volt or 3.3-Volt) VLSI applications, typical targeted threshold values are +0.7 V for NMOS devices and -0.7 V for PMOS devices. The desired threshold voltages can be achieved by adjusting the substrate dopant concentrations; however, high concentrations ($\gg 10^{16}$ cm$^{-3}$) are undesirable because they lead to high parasitic junction capacitances and low junction breakdown voltages. Therefore, the preferred method for adjusting threshold voltage is by shallow ion implantation to selectively adjust the channel dopant concentration, using a moderate substrate dopant concentration in order to avoid drain punch-through effects. The MOS threshold
Figure 5.1: Comparison of native (i.e. no threshold-adjustment implant) NMOS and PMOS threshold voltages, as a function of the channel-doping level, for various choices of gate material.
voltage is then given by the equation

\[ V_T \approx \Phi_{MS} + 2\phi_f - \frac{Q_s(2\phi_f)}{C'_{ox}} + \frac{qN_i}{C'_{ox}}, \]  

(5.4)

where \( q \) is the electronic charge and \( N_i \) is the threshold-adjustment implant dose (positive for acceptor dopants, negative for donor dopants).

Typical substrate-doping levels for submicrometer CMOS technologies fall in the \( 10^{16} \) cm\(^{-3} \) to \( 10^{17} \) cm\(^{-3} \) range. From Figure 5.1, the following observations can be made:

- The use of n\(^+ \) poly-Si as the gate material necessitates the use of a counterdoping p-channel implant to lower the doping level and achieve a desired threshold voltage of -0.7 V. This results in buried-channel PMOS devices, which are more difficult to scale down in size compared to surface-channel devices because of punch-through and drain-induced barrier-lowering (DIBL) effects [12].

- The use of p\(^+ \) poly-Si as the gate material necessitates the use of a counterdoping n-channel implant to achieve a desired threshold voltage of 0.7 V, resulting in buried-channel NMOS devices, which again are difficult to scale down in size.

- The use of p\(^+ \) poly-Si\(_{0.5}\)Ge\(_{0.5}\) rather than p\(^+ \) poly-Si as the gate material will either substantially reduce or eliminate the counterdoping n-channel implant dose needed to achieve a threshold voltage of 0.7 V, depending upon the background substrate-doping level and the gate-oxide thickness. It concurrently reduces the p-channel implant dose required to achieve a threshold voltage of -0.7 V.

As shown in Section 4.3.3, the work function of p\(^+ \) poly-Si\(_{1-x}\)Ge\(_x\) can be varied by changing the Ge content. Therefore, its use provides a means for fine-tuning and optimizing the tradeoff between the n-channel and p-channel doping designs in order to simultaneously achieve NMOS surface-channel devices and PMOS surface-channel devices. This capability cannot be provided by any other current material which is suitable for gate-electrode applications. It should be noted that as the gate-oxide
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thickness is scaled down, the threshold voltage becomes less sensitive to changes in the channel dopant concentration; $C'_{ox}$ increases so that a larger threshold-adjust implant dose is required in order to achieve a specific shift in threshold voltage. The higher channel dopant concentration results in degraded device performance. In contrast, threshold-voltage adjustments made by changing the gate work function are independent of device geometry, so that they do not scale with the gate-oxide thickness. Thus, the technological leverage which a variable-work-function gate material offers becomes increasingly important as device dimensions are scaled down. p$^+$ poly-Si$_{1-x}$Ge$_x$ is therefore a promising candidate for the gate material in submicrometer CMOS technologies.

5.1.2 Fabrication and Characterization of Poly-Si$_{1-x}$Ge$_x$-Gate MOSFETs

Simple NMOS and PMOS field-effect transistors (FETs) (Figure 5.2) were fabricated in order to demonstrate the viability of poly-Si$_{1-x}$Ge$_x$ as a CMOS gate material, using a modified version of Stanford’s standard 2$\mu$m CMOS process [83]. The 9-mask, n-well CMOS process features the use of p$^+$ poly-Si$_{1-x}$Ge$_x$ as the gate material, a gate-oxide thickness of 25 nm, and a minimum gate-length of 2 $\mu$m. The starting material is a p-type (100)-oriented silicon wafer with a resistivity between 10 and 20 $\Omega$-cm. The masked n-well phosphorus implant (2.5 x 10$^{12}$ cm$^{-2}$ $^{31}$P$^+$ at 100 keV) is performed through 240 nm of initially grown thermal SiO$_2$, and is driven in with a 16-hour anneal in an inert ambient at 1150°C, to achieve a junction depth of 4 $\mu$m and a surface concentration of 1.15 x 10$^{16}$ cm$^{-2}$. After the initial oxide layer is removed, a 25-nm-thick pad oxide layer is thermally grown, and a 85-nm-thick silicon nitride layer is deposited by LPCVD. Photolithography is used to define the active regions, and the nitride layer is etched away in the field regions using a SF$_6$-based plasma-etch process. With a layer of photoresist still covering the nitride/oxide layers in the active
Figure 5.2: Schematic cross-sectional view of CMOS devices fabricated in this work.
regions, an additional layer of photoresist is spun on and patterned to protect the n-well regions as well as the active regions during the subsequent channel-stop implant (1 x 10^{13} \text{ cm}^{-2} \text{ 11B}^+ \text{ at } 100 \text{ keV}) which is used to raise the field threshold voltage in the p-substrate regions. After the removal of the dual-layer photoresist, a 750-nm-thick field oxide is grown and the nitride and pad-oxide layers are removed by wet etching. A 20-nm-thick sacrificial oxide layer is subsequently grown, through which the masked p-channel threshold-adjustment implant (1 \times 10^{12} \text{ cm}^{-2} \text{ 75As}^+ \text{ at } 80 \text{ keV}) is performed. The sacrificial oxide layer is then removed by wet etching, and a 25-nm-thick gate oxide is thermally grown. After a backside oxide strip, the 0.5-\mu m-thick poly-Si_{1-x}Ge_x gate material is deposited by LPCVD, doped by boron implantation (1 \times 10^{16} \text{ cm}^{-2} \text{ 11B}^+ \text{ at } 35 \text{ keV}), and patterned using a masked SF_6-based plasma-etch process. Photolithography is then used to expose only the NMOS devices during the self-aligned n+ source/drain implant (6 \times 10^{15} \text{ cm}^{-2} \text{ 75As}^+ \text{ at } 100 \text{ keV}). This arsenic implant is driven in with a 10-minute anneal in O_2 at 1000°C. Afterwards, photolithography is used to expose only the PMOS devices during the self-aligned p+ source/drain implant (1 \times 10^{15} \text{ cm}^{-2} \text{ 11B}^+ \text{ at } 35 \text{ keV}). The source/drain implants are then annealed for 30 minutes in O_2 at 900°C. A 550-nm-thick passivation layer of undoped LPCVD SiO_2 (LTO) layer is subsequently deposited, and contact holes are defined using a masked reactive-ion etch process. A dual layer of sputtered Ti (100 nm thick) and sputtered Al (1 \mu m thick) is used as a metal layer; this dual layer is patterned by photolithography and successive chlorine-based-plasma Al-etch and wet Ti-etch processes. Device fabrication is completed with a 45-minute, 400°C forming-gas anneal.

Typical measured current-vs.-voltage (I-V) characteristics of poly-Si_{1-x}Ge_x-gate PMOS and NMOS transistors are shown in Figures 5.3 and 5.4, respectively. Shifts in threshold voltage due to the presence of Ge in the gate material are apparent in the subthreshold I-V plots. The noticeable “kinks” in the PMOS subthreshold characteristics are the consequence of a problem which occurred during device fabrication:
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Figure 5.3: Measured $I$-$V$ characteristics of Si$_{1-x}$Ge$_x$-gate PMOS transistors.

due to an equipment failure during the field-oxidation process, the wafers were re-worked – the original field oxide (thinner than targeted) was etched away in HF, after which the wafers were reoxidized; the nonuniform nature of the field-oxide etch coupled with the lack of an $n$-well channel-stop implant resulted in leakage problems. In short, the anomalous PMOS subthreshold characteristic (the "kink") is due to a parasitic current path resulting from a low field-threshold voltage. This problem can be circumvented with the use of thicker field oxide and/or with the use of an $n$-well channel-stop implant. The shifts in NMOS threshold voltage seen in Figure 5.4 are significantly higher than expected. This is most likely attributed to a difference in the counterdoping effect of the NMOS source/drain implant for materials of different Ge mole fractions; the high dose of arsenic probably compensated the boron gate implant more effectively in the poly-Si$_{1-x}$Ge$_x$ gates than in the poly-Si gate, resulting in slightly $n$-type rather than $p^+$ poly-Si$_{1-x}$Ge$_x$ gates. This problem can be circumvented by protecting the gate electrode during the NMOS source/drain implant (e.g., using a double-layer photoresist process or using a capping oxide layer).
5.1.3 Simulated Short-Channel Behavior of Si$_{1-x}$Ge$_x$-Gate MOSFETs

The short-channel behavior of NMOS and PMOS transistors was examined by use of numerical process [84] and device [85] simulation. Typical parameters for a submicrometer CMOS process were chosen and are listed in Table 5.3. The threshold-adjust implant doses were selected to give nominal threshold voltages of ±0.7 V for long-channel (5 μm) devices. From the plot of NMOS threshold voltage vs. effective channel length in Figure 5.5, it is apparent that NMOS short-channel behavior can be noticeably improved by using p$^+$ poly-Si$_{1-x}$Ge$_x$ for the gate material rather than p$^+$ poly-Si. The curve for an n$^+$-poly-Si-gate transistors is shown in this figure to provide a best-case reference. It should be noted that a p$^+$-poly-Si$_{1-x}$Ge$_x$-gate NMOS device exhibits better performance (e.g., higher mobility and steeper subthreshold slope) than either its n$^+$- or p$^+$-poly-Si-gate counterparts, because of its lower channel dopant concentration. From Figure 5.6, it can be seen that PMOS short-channel behavior is not compromised by using p$^+$ poly-Si$_{1-x}$Ge$_x$ as the gate material rather
Table 5.3: SUPREM-III and PISCES parameters used for simulation of short-channel NMOS and PMOS transistors.

than $p^+$ poly-Si. In fact, since the channel dopant concentration is lower for a $p^+$-poly-$Si_{1-x}Ge_x$-gate device, its performance is superior to that of a $p^+$ poly-Si-gate device.

5.1.4 Discussion

In general, a $p^+$-poly-Si-gate CMOS technology is more easily scaled to submicrometer dimensions than an $n^+$-poly-Si-gate CMOS technology, since buried-channel NMOS devices can be made more punch-through resistant at short channel lengths than buried-channel PMOS devices [86]. Buried-channel NMOS devices and surface-channel PMOS devices are also more resistant to hot-carrier instability problems [87]. The use of $p^+$ poly-$Si_{0.5}Ge_{0.5}$ rather than $p^+$ poly-Si as the gate material will either substantially reduce or eliminate the counterdoping $n$-channel threshold-adjustment implant dose, resulting in NMOS devices with superior short-channel behavior; it will
Figure 5.5: Simulated NMOS threshold voltage as a function of electrical channel length, for various choices of gate material.

Figure 5.6: Simulated PMOS threshold voltage as a function of electrical channel length, for various choices of gate material.
also reduce the \( p \)-channel threshold-adjustment implant dose, resulting in surface-channel PMOS devices with improved performance. The device-performance benefits of the lower channel-doping levels include [88]:

- higher carrier mobility [86, 12]

- steeper subthreshold slope due to reduced depletion capacitance

- reduced back-gate-bias effect (threshold-voltage shift with increasing substrate bias) [12]

- improved hot-carrier reliability due to lower electric fields near the drain region.

Thus, a \( p^+ \) poly-Si\(_{1-x}\)Ge\(_x\)-gate CMOS technology is advantageous compared to a poly-Si-gate CMOS technology.

It should be noted that a counterdoping channel implant does not necessarily lead to a buried-channel structure. The Ge content of a \( p^+ \) poly-Si\(_{1-x}\)Ge\(_x\) gate material could be increased to lower its work function only to an extent where the required counterdoping implant dose falls below the amount which would cause an \( n-p \) junction to be formed in the NMOS channel region (i.e. the implanted \( n \)-type channel region is fully depleted). In this case, the peak electric field would be located at the surface (in contrast to a typical buried-channel device, in which the peak electric field, and therefore the current path, is located below the surface), so that surface-channel operation would be achieved under turnoff conditions. At the same time, the higher channel mobility obtained with a buried-channel structure as a result of the reduction in transverse electric field would be preserved [86]. Since large reductions in the gate work function may compromise the PMOS short-channel behavior, there is a tradeoff between the \( n \)-channel and \( p \)-channel doping designs, which can be optimized by adjusting the Ge mole fraction of the \( p^+ \) gate material for each specific CMOS process.

For CMOS technologies in which the background channel-doping concentrations are relatively low (e.g. silicon-on-insulator technologies), the work function of a \( p^+ \) poly-Si\(_{1-x}\)Ge\(_x\) gate material can easily be reduced enough so that a counterdoping
implant is not required for the NMOS devices and hence NMOS and PMOS surface-channel devices may be simultaneously obtained. Recently, the application of p\textsuperscript{+} poly-Si\textsubscript{1-x}Ge\textsubscript{x} as a gate material for fully depleted silicon-on-insulator technologies has been demonstrated to provide greater flexibility in NMOS and PMOS device design, with improved threshold-voltage control [89].

5.2 A Gate Material for Thin-Film Transistor Technologies

Poly-Si thin-film transistors (TFTs) are presently used to implement integrated CMOS circuitry in various large-area-electronics products such as linear image sensors [90] and active-matrix liquid-crystal displays (AMLCDs) [91, 92, 93]. The development of a low-temperature (< 600°C) self-aligned-gate CMOS fabrication process for high-performance TFTs is essential for these applications [54]. The low process temperatures would reduce manufacturing cost by allowing the use of inexpensive glass substrates rather than costly quartz substrates; the self-aligned-gate TFTs would allow higher pixel aperture ratios to be achieved and facilitate high-speed circuit operation due to their low parasitic capacitances; and the use of CMOS (rather than all-NMOS) circuits would reduce display power consumption and also allow the display-driver circuits to operate at higher frequencies.

To date, many researchers have successfully used conventional fabrication processes to achieve high-performance poly-Si TFTs on glass substrates, limiting the maximum process temperature to 600°C [54, 93, 94]. However, as the size of the substrates is increased, problems with warpage occurring during the high-temperature (600°C) process steps are aggravated and thus yield is detrimentally affected. These problems can be assuaged by minimizing exposure of the glass substrates to high temperatures; therefore, a substantial reduction in the maximum process temperature would be beneficial, provided that device performance is not compromised. Using
laser-induced crystallization, high-performance devices have been achieved without exceeding a process temperature of 450°C [95]. However, the higher cost and lower throughput of laser processing, as well as its potential problems with controllability and uniformity over large areas, make its use less than ideal for large-area-electronics applications. In this work, conventional NMOS and PMOS poly-Si TFTs have been fabricated using a significantly reduced temperature (≤550°C) process without compromising the device performance of higher temperature (600 °C) technologies. This process features the use of polycrystalline Si$_{0.5}$Ge$_{0.5}$ for the gate material, in addition to high-dose H$^{+}$ implantation for grain-boundary passivation, so that shorter process times can be used. This technology is therefore practical for low-cost manufacturing of large-area electronics products.

5.2.1 Low-Temperature (≤550°C) Fabrication of Poly-Si TFTs

Standard self-aligned-gate n-channel and p-channel TFTs were fabricated using conventional Si processing techniques. Silicon wafers with 0.5 μm of thermally grown SiO$_2$ were used for the insulating substrates. The 150 nm-thick active layer of silicon was deposited in amorphous form at 550°C in a commercial low-pressure chemical-vapor deposition (LPCVD) system using SiH$_4$ as the gaseous deposition source, and was subsequently crystallized during a 24-hour anneal at 550°C. The average grain size in the Si film after this crystallization step was determined by transmission electron microscopy (TEM) to be ~300 nm. X-ray diffraction (XRD) analyses show that these crystallized films have a {111} preferential orientation (Figure 5.7). After the active regions were defined by plasma etching, a 45 nm-thick gate oxide was deposited by LPCVD at 400°C and was then annealed at 550°C for 6 hours in O$_2$ and 6 hours in N$_2$. Polycrystalline Si$_{0.5}$Ge$_{0.5}$ deposited at 500°C was used for the gate electrode material. This gate material was 200 nm thick, and was doped by implantation of boron (to a dose of 4 x 10$^{18}$ cm$^{-2}$ at 40 keV) followed by annealing for 1 hour at
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Figure 5.7: X-ray diffraction data for the 150 nm-thick poly-Si TFT channel film, which was deposited at 550°C, then crystallized during a 24-hour anneal at 550°C. The average grain size was determined by TEM analysis to be \(~300\) nm.

550°C. After the gate material was patterned, the source and drain regions were formed by ion implantation of phosphorus (to a dose of \(4 \times 10^{15}\) cm$^{-2}$ at 120 keV) and boron (to a dose of \(4 \times 10^{15}\) cm$^{-2}$ at 46 keV) for the NMOS and PMOS devices, respectively. The PMOS devices were then annealed for 8 hours; however, because of the high-energy and high-dose phosphorus implant conditions, an anneal time of approximately 60 hours at 550°C was required to completely recrystallize the NMOS source and drain regions. This problem could have been readily avoided by using a lower implant dose and a lower implant energy for the NMOS devices. In subsequent experiments, TFTs with 100 nm-thick Si channel layers were successfully fabricated using low-dose (\(2 \times 10^{15}\) cm$^{-2}$) shallow source/drain implants (boron implanted at 20 keV, phosphorus implanted at 45 keV) annealed for 1 hour at 550°C, and sheet resistivities \(<1\) kΩ/□ were attained for the NMOS and PMOS source/drain regions. For the devices reported in this work, the final sheet resistivities of the source and drain regions were \(~300\) Ω/□, and the final sheet resistivity of the p$^+$ poly-Si$_{0.5}$Ge$_{0.5}$ gate
Chapter 5. Polycrystalline \( \text{Si}_{1-x}\text{Ge}_x \): A New Gate-Electrode Material

<table>
<thead>
<tr>
<th></th>
<th>NMOS ( V_{DS} = 0.1 \text{ V} )</th>
<th>PMOS ( V_{DS} = -10 \text{ V} )</th>
</tr>
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<tbody>
<tr>
<td>Threshold voltage (V)</td>
<td>2.8</td>
<td>-0.2</td>
</tr>
<tr>
<td>Inverse sub-threshold slope (V/dec)</td>
<td>0.62</td>
<td>1.37</td>
</tr>
<tr>
<td>Field-effect mobility (cm²/V-s)</td>
<td>35</td>
<td>34</td>
</tr>
<tr>
<td>Leakage current (pA/μm channel width)</td>
<td>0.05</td>
<td>0.8</td>
</tr>
<tr>
<td>Maximum ON/OFF current ratio</td>
<td>( 7 \times 10^6 )</td>
<td>( 4 \times 10^5 )</td>
</tr>
</tbody>
</table>

Table 5.4: Summary of poly-SiGe-gate low-temperature-processed poly-Si TFT performance. Drawn channel width = drawn channel length = 10 μm. The maximum ON/OFF current ratios are for gate voltage swings of ~20 V.

material was 137 \( \Omega/\square \). Following the low-temperature SiO₂ (LTO) passivation-layer deposition, contact definition and Al-Si metallization steps, the devices were given a 30-minute forming-gas anneal at 300°C. Finally, the channel poly-Si regions were hydrogenated by implantation of \( \text{H}^+ \) (to a dose of \( 3 \times 10^{15} \text{ cm}^{-2} \) at 32 keV) followed by a 10-minute forming-gas anneal at 400°C [96]. The short post-\( \text{H}^+ \)-implant annealing step was sufficient to achieve well-hydrogenated devices. In contrast, much longer annealing times (many hours) would have been needed if plasma hydrogenation had been used, due to the finite diffusion rate of hydrogen into the channel regions [97, 98].

5.2.2 Electrical Characteristics of Poly-SiGe-Gate TFTs

Typical measured \( I-V \) characteristics are shown in Figure 5.8 for large (\( W_{\text{drawn}} = L_{\text{drawn}} = 10 \mu\text{m} \)) transistors, and a summary of various device parameters is given in Table 5.4. The gate current was monitored during the subthreshold measurements, and was found to be less than 1 pA for \( |V_G| \) up to 20 V. From plots of inverse peak transconductance vs. drawn channel length, the lateral source/drain diffusion lengths were found to be 0.14 μm for the NMOS devices and 0.42 μm for the PMOS devices.
Figure 5.8: Measured I-V characteristics of low-temperature-processed, poly-SiGe-gate poly-Si TFTs which have drawn channel widths of 10 μm. The effective NMOS and PMOS channel lengths are 9.72 μm and 9.16 μm, respectively.
Chapter 5. Polycrystalline $\text{Si}_{1-x}\text{Ge}_x$: A New Gate-Electrode Material

Taking these diffusion lengths into account, the effective electron and hole mobilities were 35 and 28 cm$^2$/V·s, respectively. For threshold voltage defined at a fixed normalized drain current of 100 nA at 10 V drain bias, the respective NMOS and PMOS device threshold voltages were 2.9 V and -0.1 V. (This definition of threshold voltage at a fixed drain current scaled by the device geometry – that is, at a certain surface band-bending condition – avoids the ambiguity associated with an extrapolated threshold voltage, which arises in TFTs because the effective channel mobility depends strongly on the gate bias [99].) The trap-state density, $N_t$, was calculated from the slope of the $\ln(I_{DS}/V_{GS})$ vs. $1/V_{GS}$ plot at low drain bias (0.1 V) to be $\sim7 \times 10^{11}$ cm$^{-2}$ for the NMOS devices.

The performance of the transistors fabricated in this work is comparable to that reported by others for TFTs fabricated using 600°C technologies, and is sufficient for large-area display driver applications [93, 100]. In addition, this low-temperature (550°C) technology provides devices with threshold voltages which are significantly lower than for those provided by previously reported 600°C technologies, so that lower gate-drive voltages and therefore lower-voltage driver circuits may be used. The PMOS threshold voltage is especially low; this is because the undoped poly-Si channel material is slightly $p$-type [101], so that the PMOS TFT is an accumulation-mode device (which also accounts for its relatively high leakage). The poor PMOS subthreshold slope arises from a high density of unpassivated trap states in the lower portion of the Si energy band gap [101]; a steeper slope should be achievable with further optimization of the post-H$^+$-implant annealing process.

5.2.3 Discussion

Poly-SiGe is an ideal alternative to poly-Si for the TFT gate material because of its compatibility with low-temperature processing and its low resistivity. $\text{Si}_{0.5}\text{Ge}_{0.5}$ is deposited in polycrystalline form for temperatures down to $\sim425$°C (Figure 3.11), and therefore does not require a crystallization anneal step after low-temperature
Chapter 5. Polycrystalline Si$_{1-x}$Ge$_x$: A New Gate-Electrode Material

(≤500°C) deposition; in contrast, Si is deposited in amorphous form for temperatures below ∼570°C [62], and it therefore requires a very long annealing step to be converted into polycrystalline material, in order to achieve low resistivity. In addition, a high degree of boron activation can be achieved in poly-Si$_{0.5}$Ge$_{0.5}$ by short-time annealing at ∼500°C (Figure 4.14). This not only allows for a low thermal-processing budget, but it also mitigates the problem of insufficient dopant activation at the gate-material/gate-dielectric interface. It is well known that depletion effects in a poly-Si gate material significantly degrade MOS device performance [81]. The use of Si$_{0.5}$Ge$_{0.5}$ rather than Si for the gate material does affect device threshold voltages, however. Since the work function of p$^+$ poly-Si$_{0.5}$Ge$_{0.5}$ is larger (by ∼0.8 V – refer to Figure 4.19) than that of n$^+$ poly-Si, the NMOS threshold voltage is larger (more positive) and the PMOS threshold voltage is smaller (less negative) compared to n$^+$ poly-Si gate devices.

It should be noted that for large-area gray-scale displays, a pixel (NMOS) TFT must have leakage below ∼0.1 pA per μm channel width (at $V_{DS} = 10$ V) in order to sufficiently maintain the charge on a pixel over one addressing cycle [102]. The NMOS devices fabricated in this work have leakage currents which are approximately one order of magnitude too high for pixel applications. It should be possible, however, to significantly reduce this leakage current by using multiple-gate structures [103] and gate-offset structures [104] to minimize the electric field near the drain.

It is difficult to directly compare the results of this work with those previously reported in the literature because of differences in specific process parameters (e.g. process temperatures, process times, poly-Si channel thickness, gate-insulator material, gate-insulator thickness, etc.). Two factors may have contributed to the achievement of good device characteristics in this work:

1. the use of a thinner gate insulator (45 nm thick): Typical gate-insulator thicknesses used in previously reported works are ∼100 nm. The use of a thinner gate dielectric improves (steepens) the subthreshold slope [105]. Since the gate leakage was verified to be small for gate biases up to 20 V, the use of this thinner
2. the use of poly-Si$_{0.5}$Ge$_{0.5}$ as the gate material: As explained earlier, a benefit of using Si$_{0.5}$Ge$_{0.5}$ as the gate material is the high degree of dopant (boron) activation which can be achieved with low-temperature, short-time annealing. Deleterious gate-depletion effects are thus avoided without excessively long anneals. (Depletion in a semiconductor gate material which is nondegenerately doped near the oxide interface results in an increased “equivalent” gate oxide thickness, thereby degrading the transconductance or effective carrier mobility.)

Significantly reduced manufacturing costs can be realized for poly-Si TFT products by lowering process temperatures to allow the use of less-expensive Corning 7059 glass. Since this glass has a strain point of 593°C, its manufacturer does not recommend processing it above 575°C. Therefore, the reduction of the maximum process temperature from 600°C (typical of state-of-the-art “low-temperature” poly-Si TFT processes) down to 550°C is an important contribution. Czubatij et al. have reported on poly-Si TFTs fabricated using conventional (i.e. non-laser) equipment; however, in their work, only NMOS TFTs were fabricated, and the device performance was relatively poor [106]. In this work, both n-channel and p-channel poly-Si TFTs with good characteristics have been successfully fabricated using conventional processing equipment without exceeding 550°C, and the performance of these devices is comparable to the performance of 600°C-processed TFTs. The two novel elements of the 550°C TFT process are the use of Si$_{0.5}$Ge$_{0.5}$ as the gate material and the use of H$^+$ implantation for defect passivation. Each allows significantly shorter process times to be used in the TFT fabrication process and thus facilitates the fabrication of high-performance poly-Si TFTs on low-cost glass substrates.
5.3 Summary

$p^+$ poly-Si$_{1-x}$Ge$_x$ has been demonstrated to be a promising alternative to poly-Si for the gate material in CMOS technologies. The work function of $p^+$ poly-Si$_{1-x}$Ge$_x$ can be modified by varying the Ge content, to optimize the trade-off between the PMOS and NMOS channel-doping designs and achieve devices which are more easily scalable to sub-micrometer dimensions. This optimization is not possible with any other choice of gate material. Because of its compatibility with low-temperature ($\leq 550^\circ$C) processing, $p^+$ poly-Si$_{1-x}$Ge$_x$ is especially attractive for applications as the gate material in TFT technologies which have limited thermal budget and hence require low-temperature processing. With its ease of formation and compatibility with VLSI fabrication techniques, poly-Si$_{1-x}$Ge$_x$ should be easy to assimilate into any existing Si-based CMOS process.
Chapter 6

Polycrystalline \( \text{Si}_{1-x}\text{Ge}_x \) Thin-Film Transistors

In this chapter, the fabrication and the characterization of poly-Si\(_{1-x}\text{Ge}_x \) TFTs are described. Several technology issues are then discussed: crystallization of amorphous Si\(_{1-x}\text{Ge}_x \) films, properties of the SiO\(_2\)/Si\(_{1-x}\text{Ge}_x \) interface, and passivation of defects in poly-Si\(_{1-x}\text{Ge}_x \) via hydrogenation.

6.1 Fabrication and Characterization of Poly-Si\(_{1-x}\text{Ge}_x \) TFTs

6.1.1 \( p \)-Channel Poly-Si\(_{0.75}\text{Ge}_{0.25} \) TFTs

The resistivity of heavily \( p \)-type doped (\( p^+ \)) poly-Si\(_{1-x}\text{Ge}_x \) is substantially lower than that of comparably doped poly-Si; in addition, significantly lower anneal temperatures (as low as 500°C) are sufficient to achieve a high degree of boron activation in poly-Si\(_{1-x}\text{Ge}_x \) as compared to poly-Si. (Refer to Section 4.3). This low-temperature processing capability, along with the potential enhancement in carrier mobilities [107], provided the motivation for an initial investigation of the characteristics of \( p \)-channel
poly-Si$_{1-x}$Ge$_x$ TFTs. In this section, results of the first attempt at fabrication and electrical characterization of enhancement-mode $p$-channel MOS transistors in undoped poly-Si$_{75}$Ge$_{25}$ films are summarized.

Figure 6.1 shows a schematic cross-sectional view of the poly-Si$_{0.75}$Ge$_{0.25}$ TFTs fabricated in this work. Conventional processing techniques were used to fabricate the TFTs, as detailed in Table 6.5, using either a low-temperature ($\leq 600^\circ$C) or a high-temperature ($\leq 950^\circ$C) process. The differences between these two processes lie in the poly-Si$_{0.75}$Ge$_{0.25}$ channel-layer deposition temperature, the gate-oxide anneal temperature, the gate-electrode material, and the source/drain implant-anneal temperature. In each process, 100 mm-diameter silicon wafers with thermally grown SiO$_2$ are used for the starting substrates. In the high-temperature process, the 180
<table>
<thead>
<tr>
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<th>PROCESS DETAILS</th>
</tr>
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<tr>
<td></td>
<td></td>
<td>HIGH-TEMP. PROCESS</td>
</tr>
<tr>
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</tr>
<tr>
<td>1</td>
<td>poly-Si$<em>{0.75}$Ge$</em>{0.25}$ deposition</td>
<td>$T_{\text{deposition}} = 625^\circ\text{C}$</td>
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<tr>
<td>2</td>
<td>Si implantation</td>
<td>$2 \times 10^{15}$ cm$^{-2}$ @ 75 keV</td>
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<tr>
<td>3</td>
<td>recrystallization anneal</td>
<td>120 hours in N$_2$ @ 600$^\circ$C</td>
</tr>
<tr>
<td>4</td>
<td>“active area” island patterning</td>
<td>SF$_6$-based plasma etch process</td>
</tr>
<tr>
<td>5</td>
<td>gate-oxide deposition</td>
<td>LPCVD SiO$<em>2$: $T</em>{\text{deposition}} = 400^\circ$C</td>
</tr>
<tr>
<td>6</td>
<td>gate-oxide anneal/densification</td>
<td>15' in O$<em>2$ + 20' in Ar $T</em>{\text{anneal}} = 950^\circ$C</td>
</tr>
<tr>
<td>7</td>
<td>gate-material deposition</td>
<td>poly-Si $T_{\text{deposition}} = 620^\circ$C</td>
</tr>
<tr>
<td>8</td>
<td>gate doping</td>
<td>20' @ 900$^\circ$C in POCl$_3$ (none)</td>
</tr>
<tr>
<td>9</td>
<td>gate patterning</td>
<td>SF$_6$-based plasma etch process</td>
</tr>
<tr>
<td>10</td>
<td>source/drain/gate implant</td>
<td>boron implant: $2 \times 10^{15}$ cm$^{-2}$ @ 60 keV</td>
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<tr>
<td>11</td>
<td>passivation-layer deposition</td>
<td>LPCVD SiO$_2$ @ 400$^\circ$C followed by LPCVD Si$_3$N$_4$ @ 785$^\circ$C</td>
</tr>
<tr>
<td>12</td>
<td>source/drain/gate implant anneal</td>
<td>30' @ 900$^\circ$C in Ar</td>
</tr>
<tr>
<td>13</td>
<td>contact definition</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>metallization</td>
<td>by sputter deposition; Al-Si(1%)</td>
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<tr>
<td>15</td>
<td>forming-gas anneal</td>
<td>30' @ 400$^\circ$C in 80% N$_2$/20% H$_2$</td>
</tr>
</tbody>
</table>

Table 6.5: $p$-channel poly-Si$_{0.75}$Ge$_{0.25}$ TFT fabrication process details.
nm-thick channel layer is deposited in polycrystalline form at 625°C, the 100 nm-thick LPCVD gate oxide is annealed at 950°C, the gate-electrode material is poly-Si (300 nm thick), and the source/drain boron implant is annealed at 900°C. In the low-temperature process, the channel layer is deposited in amorphous form at 550°C, the gate oxide is annealed at 600°C, the gate-electrode material is poly-Si$_{0.8}$Ge$_{0.2}$, and the gate/source/drain boron implant is annealed at 550°C. After initial current-vs.-voltage ($I-V$) measurements were made, the poly-Si$_{0.75}$Ge$_{0.25}$ TFTs were hydrogenated by implanting H$^+$ (to a dose of $1 \times 10^{17}$ cm$^{-2}$ for the high-temperature-processed devices, and to a dose of $3 \times 10^{16}$ cm$^{-2}$ for the low-temperature-processed devices) into the channel region and annealing for 10 minutes at 275°C. The devices were subsequently re-tested.

Typical transfer characteristics are shown in Figure 6.2 for large ($W = 10 \ \mu$m, $L = 5 \ \mu$m) transistors fabricated using the high-temperature and the low-temperature processes. These characteristics were obtained with the drain and source voltages fixed at -1 V and 0 V, respectively, and the body bias left floating. The corresponding drain characteristics for these transistors are shown in Figure 6.3, for gate biases of 0, -5, -10, -15, and -20 V. It can be seen from Figures 6.2 and 6.3 that hydrogenation renders a dramatic improvement in device performance for poly-Si$_{0.75}$Ge$_{0.25}$ TFTs, as it does for poly-Si TFTs [96]. Typical threshold voltages (defined at a fixed normalized drain current of 10 nA [108]) achieved are -5 V and -9 V for the hydrogenated high-temperature-processed (HT) devices and the low-temperature-processed (LT) devices, respectively. Slightly smaller HT and LT devices ($W = 10 \ \mu$m, $L = 2 \ \mu$m) exhibit subthreshold slopes of 1.0 dec/V and 0.4 dec/V, and peak hole mobilities (measured in the linear region of operation, with drain bias -1 V) of 30 cm$^2$/V·s and 8 cm$^2$/V·s, respectively. Leakage currents $\sim$0.1 pA and $\sim$0.5 pA per $\mu$m channel width, and $I_{\text{ON}}/I_{\text{OFF}}$ current ratios $\sim 10^7$ and $\sim 10^6$, are achieved in the HT and LT devices, respectively.

These initial results indicate that TFTs with well-behaved characteristics can be realized in poly-Si$_{1-x}$Ge$_x$ films, even though various fabrication-process parameters
Figure 6.2: Measured subthreshold characteristics of high-temperature-processed (HT) and low-temperature-processed (LT) p-channel poly-Si$_{0.75}$Ge$_{0.25}$ TFTs.

were not optimized in this study. Since the electrical performance of polycrystalline MOS transistors is degraded by the presence of carrier traps associated with defects within the active layer [109, 110, 111], it can be expected that the performance of poly-Si$_{0.75}$Ge$_{0.25}$ TFTs would improve considerably upon optimization of the crystallization and grain-boundary passivation processes, as is the case with poly-Si TFTs [112, 113]. Improvements should also be attainable through the use of a thinner gate oxide or a thinner channel film [8, 114].

From the $I$-$V$ characteristics shown in Figure 6.3b, it is apparent that a 30-minute anneal at 550°C is sufficient to activate the boron implanted into the gate and source/drain regions. Reasonably low sheet resistivities of 136 $\Omega/\square$ and $\sim$300 $\Omega/\square$ are achieved in these regions, respectively. These results indicate that it should be possible to fabricate poly-Si$_{1-x}$Ge$_x$ TFTs using process temperatures $\leq$550°C, which are compatible with glass substrates.
Figure 6.3: Measured drain characteristics of $p$-channel poly-Si$_{0.75}$Ge$_{0.25}$ TFTs: (a) 950°C-processed device; (b) 600°C-processed device.
Figure 6.4: Schematic cross-sectional view of 550°C-processed poly-Si$_{0.8}$Ge$_{0.2}$ TFT.

6.1.2 \textit{n-} and \textit{p-}Channel Poly-Si$_{0.8}$Ge$_{0.2}$ TFTs

In this section, a low-temperature poly-Si$_{1-x}$Ge$_x$ CMOS TFT technology is presented. Conventional microelectronics fabrication techniques are used to fabricate the TFTs using process temperatures $\leq$ 550°C, which makes this technology suitable for the fabrication of polycrystalline-film TFTs on glass substrates. The Ge mole fraction of the channel film was more conservatively chosen to be 0.2, in order to avoid potential problems with leakage currents (which tend to be higher in low-temperature-processed TFTs [100]) due to a large reduction in energy band gap (seen in Figure 4.20).

Figure 6.4 shows a schematic cross-sectional view of the poly-Si$_{0.8}$Ge$_{0.2}$ TFT structure. As outlined in Table 6.6, a self-aligned-gate process was used to fabricate \textit{n-} and \textit{p-}channel MOS field-effect transistors on oxidized 100 mm-diameter silicon wafers. In this process, the 160 nm-thick active layer of Si$_{0.8}$Ge$_{0.2}$ is deposited in amorphous form at 490°C and is subsequently crystallized by a 24-hour, 550°C anneal. From transmission electron microscopy (TEM) analysis, the average grain size in the crystallized film was determined to be $\sim$ 0.15 $\mu$m (Figure 6.5). After the active regions were de-
<table>
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<th>PROCESS DETAILS</th>
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<td>starting substrate</td>
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<td>channel Si₀.₈Ge₀.₂ deposition</td>
<td>T&lt;sub&gt;dep&lt;/sub&gt; = 490°C</td>
</tr>
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<td>2</td>
<td>crystallization anneal</td>
<td>24 h in N&lt;sub&gt;2&lt;/sub&gt; at 550°C</td>
</tr>
<tr>
<td>3</td>
<td>“active area” definition</td>
<td>SF&lt;sub&gt;6&lt;/sub&gt;-based plasma etch</td>
</tr>
<tr>
<td>4</td>
<td>gate-oxide deposition</td>
<td>by LPCVD; T&lt;sub&gt;dep&lt;/sub&gt; = 400°C</td>
</tr>
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<td>5</td>
<td>gate-oxide anneal</td>
<td>6 h in O&lt;sub&gt;2&lt;/sub&gt; + 6 h in N&lt;sub&gt;2&lt;/sub&gt; at 550°C</td>
</tr>
<tr>
<td>6</td>
<td>gate-material deposition</td>
<td>poly-Si₀.₅Ge₀.₅; T&lt;sub&gt;dep&lt;/sub&gt; = 500°C</td>
</tr>
<tr>
<td>7</td>
<td>gate doping (by implantation)</td>
<td>4 x 10&lt;sup&gt;15&lt;/sup&gt; B&lt;sup&gt;⁺&lt;/sup&gt; cm&lt;sup&gt;−2&lt;/sup&gt; @ 40 keV + 1 h anneal in N&lt;sub&gt;2&lt;/sub&gt; at 550°C</td>
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<tr>
<td>8</td>
<td>gate patterning</td>
<td>SF&lt;sub&gt;6&lt;/sub&gt;-based plasma etch</td>
</tr>
<tr>
<td>9</td>
<td>source/drain implant (dose = 4 x 10&lt;sup&gt;15&lt;/sup&gt; cm&lt;sup&gt;−2&lt;/sup&gt;)</td>
<td>NMOS: P&lt;sup&gt;⁺&lt;/sup&gt; @ 120 keV PMOS: B&lt;sup&gt;⁺&lt;/sup&gt; @ 46 keV</td>
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<td>10</td>
<td>passivation-layer deposition</td>
<td>LPCVD SiO₂ at 400°C</td>
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<td>11</td>
<td>source/drain implant anneal</td>
<td>60 h at 550°C</td>
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<td>12-13</td>
<td>contact definition, Al metallization</td>
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<td>14</td>
<td>forming-gas anneal</td>
<td>30 min at 300°C</td>
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<tr>
<td>15</td>
<td>hydrogenation (by implantation)</td>
<td>5 x 10&lt;sup&gt;16&lt;/sup&gt; H&lt;sup&gt;⁺&lt;/sup&gt; cm&lt;sup&gt;−2&lt;/sup&gt; @ 32 keV + 10 min anneal in N&lt;sub&gt;2&lt;/sub&gt; at 275°C</td>
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</table>

Table 6.6: Low-temperature (550°C) poly-Si₀.₅Ge₀.₂ TFT fabrication process details.
Figure 6.5: Plan-view TEM micrograph of the 160-nm-thick Si$_{0.8}$Ge$_{0.2}$ TFT channel film, which was deposited in amorphous form at 490°C and ~0.3 torr and then crystallized by a 24-hour, 550°C anneal. The average grain size is 0.15 μm.
fined by plasma etching, a 50 nm-thick gate oxide was deposited by LPCVD at 400°C and densified by 550°C annealing (6 hours in O₂ and 6 hours in N₂). Boron-doped poly-Si₀.₅Ge₀.₅ was used for the gate-electrode material. After the patterning of the gate material, the source and drain regions were formed by ion implantation of phosphorus or boron for the n- or p-channel TFTs, respectively. A 1-hour anneal at 550°C was sufficient to achieve a sheet resistivity of 900 Ω/□ in the source and drain regions of the p-channel devices; however, the source and drain regions of the n-channel devices required ~ 60 hours @ 550°C to recrystallize because a deep, high-dose phosphorus implant was used. This long anneal could have been avoided by using a lower implant dose and a lower implant energy for the n-channel devices. Sheet resistivities of ~10 kΩ/□ and ~200 Ω/□ were achieved in the n-channel source-and-drain regions and the p⁺ poly-Si₀.₅Ge₀.₅ gate material, respectively. Following the passivation-layer deposition, contact definition and Al-Si metallization steps, the devices were given a 30-minute forming-gas anneal at 300°C. Finally, the channel poly-Si₀.₈Ge₀.₂ regions were hydrogenated by high-dose H⁺ implantation (5×10¹⁶ cm⁻² @ 32 keV) followed by a 10-minute forming-gas anneal at 275°C.

Typical measured device characteristics are shown in Figure 6.6, and a summary of TFT performance parameters is given in Table 6.7. Both the n- and p-channel devices exhibit fairly well-behaved transistor characteristics. Under high drain bias, however, the n-channel device displays a large leakage current; this is because the undoped poly-Si₀.₈Ge₀.₂ channel material is slightly n-type, as will be shown later, so that the device is operating in the accumulation mode. Lower leakage currents should be attainable by doping the channel region slightly p-type (e.g. with a low-dose boron implant). These first results demonstrate the feasibility of fabricating both n-channel and p-channel TFTs (and hence CMOS circuits) in polycrystalline silicon-germanium films at temperatures compatible with glass substrates.

The electrical characteristics of poly-Si₁₋ₓGeₓ TFTs can be expected to be strongly dependent on electronic trap states associated with intergranular and intragranular defects in the channel film, similarly to poly-Si TFTs [115, 116, 117].
Figure 6.6: Measured I-V characteristics of 550°C-processed n-channel (top) and p-channel (bottom) poly-Si$_{0.8}$Ge$_{0.2}$ TFTs.
### Table 6.7: Summary of 550°C-processed Si_{0.8}Ge_{0.2} TFT characteristics. (L_{drawn} = W_{drawn} = 10 \, \mu m.) The I_{ON}/I_{OFF} ratios are for gate voltage swings of \sim 30 \, V.

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<th>PMOS</th>
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<tr>
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<td>V_{DS} = 0.1 V</td>
<td>V_{DS} = -0.1 V</td>
</tr>
<tr>
<td>Threshold voltage (V)</td>
<td>11</td>
<td>-7</td>
</tr>
<tr>
<td>Channel mobility (cm²/V·s)</td>
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<td>1.2</td>
</tr>
<tr>
<td>Subthreshold slope (dec/V)</td>
<td>0.9</td>
<td>0.6</td>
</tr>
<tr>
<td>Leakage current (pA/μm)</td>
<td>0.03</td>
<td>0.15</td>
</tr>
<tr>
<td>Maximum I_{ON}/I_{OFF}</td>
<td>7.5x10⁴</td>
<td>10⁵</td>
</tr>
</tbody>
</table>
Previous works on poly-Si TFTs have suggested that various TFT-performance parameters are strongly correlated with trap-state densities in separate portions of the Si bandgap. For example, both the threshold voltage and subthreshold slope improve more quickly during hydrogenation than do the leakage current and mobility [118]; in addition, steady-state bias stress has been found to cause a noticeable increase in threshold voltage, but no significant change in either the leakage current or the mobility [119, 120]. Since electrical stressing results in an increase in trap-state densities located near midgap [121], these findings together indicate that both the threshold voltage and the subthreshold slope are more closely associated with trap states located near midgap, while both the leakage current and mobility are more closely associated with trap-states located near the band edges. Therefore, the relatively high threshold voltages and shallow subthreshold slopes exhibited by the poly-Si$_{0.8}$Ge$_{0.2}$ TFTs in this work (Figure 6.6) are indicative of a relatively high density of trap states near midgap, and the relatively low channel mobilities are indicative of high densities of trap states near the band edges.

Valuable information about the effective density-of-states (DOS) distribution in poly-Si$_{1-x}$Ge$_x$ can be gained from studies of the temperature dependence of TFT conductance in these films. The field-effect conductance, $G = I_{DS}/V_{DS}$, is thermally activated and can be described by the equation

$$G = G_0 \exp(-E_a/kT)$$

(6.1)

where $I_{DS}$ is the drain current, $V_{DS}$ is the drain bias, $G_0$ is a constant, $E_a$ is the conductance activation energy, $k$ is the Boltzmann constant, and $T$ is the measurement temperature [122]. If potential barriers do not exist at the grain boundaries in the channel film, the activation energy $E_a$ is simply the energy difference between the Fermi level and the conduction band (for $n$-channel devices) or the valence band (for $p$-channel devices) in the surface region of the channel film. If barriers do exist at the grain boundaries, then $E_a$ is approximately the sum of the aforementioned energy difference within the grains and the barrier height at the grain boundaries[123]. In
short, $E_a$ is the energy difference between the effective conduction band edge and the Fermi level for $n$-channel TFTs, and the energy difference between the Fermi level and the effective valence band edge for $p$-channel TFTs. As the TFT gate voltage is increased, trap states in the channel film at the Fermi level are charged or discharged, and the Fermi level moves closer to the band edge, inducing a conducting layer of carriers near the surface [124]. Since part of the applied gate voltage is used to fill traps rather than to bend the energy bands (i.e. to induce free carriers), the amount of decrease in $E_a$ which results from an increase in gate voltage is a measure of the trap-state density effectively at an energy $E_a$ away from the band edge in the bandgap: the higher the trap-state density, the more difficult it is to move the Fermi level and thus reduce $E_a$.

The subthreshold $I$-$V$ characteristics of the poly-Si$_{0.8}$Ge$_{0.2}$ TFTs were measured at temperatures ranging from 21°C to 125°C, with $|V_{DS}| = 0.1$ V to avoid large potential variations across the channel region; $E_a$ was then calculated from the slope of the straight-line Arrhenius plot of $\log G$ vs. $1/kT$ for each gate bias (Figure 6.7). $E_a$ is plotted as a function of the gate voltage in Figure 6.8, both for the unhydrogenated devices and for the hydrogenated devices. It can be seen to vary more slowly with gate voltage for the unhydrogenated TFTs than for the hydrogenated TFTs, due to the higher trap-state densities in the unhydrogenated channel film. For the unhydrogenated $n$-channel TFT, $E_a$ increases with increasing gate voltage, which suggests that trap levels near the valence-band edge are being filled, causing the potential barriers to electron flow to increase. These trap states are most likely associated with germanium, since the trap levels in poly-Ge films are located in the lower half of the bandgap whereas those in poly-Si are located closer to midgap [125], and they cause poly-Si$_{1-x}$Ge$_x$ to exhibit properties similar to p$^+$ material [126]. Upon the passivation of these trap states by hydrogenation, the $n$-channel TFT conductance activation energy decreases with increasing gate voltage as required for proper TFT operation.

$E_a$ is plotted for the hydrogenated devices in Figure 6.9 as a function of gate drive ($|V_G - V_{FB}|$, where $V_{FB}$ is the gate voltage corresponding to maximum $E_a$). Also in-
Figure 6.7: Determination of conductance activation energies for 550°C-processed, hydrogenated poly-Si$_{0.8}$Ge$_{0.2}$ TFTs ($L_{\text{drawn}} = W_{\text{drawn}} = 10$ μm, $|V_{\text{DS}}| = 0.1$ V): (a) NMOS device; (b) PMOS device.
Figure 6.8: Conductance activation energy of 550°C-processed n-channel (NMOS) and p-channel (PMOS) poly-Si$_{0.8}$Ge$_{0.2}$ TFTs, as a function of gate voltage.

Figure 6.9: Conductance activation energy as a function of gate drive ($|V_G - V_{FB}|$), for n-channel (NMOS) and p-channel (PMOS) poly-Si$_{0.8}$Ge$_{0.2}$ and poly-Si TFTs.
cluded in this figure are data for hydrogenated poly-Si TFTs which were fabricated using a similar low-temperature process [127]. $E_a$ decreases much more slowly with gate voltage for the poly-Si$_{0.8}$Ge$_{0.2}$ devices than for the poly-Si devices, which indicates that the trap-state density in poly-Si$_{0.8}$Ge$_{0.2}$ is higher than that in poly-Si. $E_a$ decreases more slowly for the $n$-channel device than for the $p$-channel device in poly-Si$_{0.8}$Ge$_{0.2}$, which shows that higher trap-state densities exist in the upper half of the poly-Si$_{0.8}$Ge$_{0.2}$ bandgap than in the lower half. In poly-Si, the opposite is true: $E_a$ decreases more slowly for the $p$-channel device than for the $n$-channel device, which shows that higher trap-state densities exist in the lower half of the poly-Si bandgap.

At zero gate drive, a TFT is in the “OFF” state, and the activation energy of the drain (leakage) current, $E_{a0}$, is approximately equal to the channel-to-source barrier height [128]. Since the TFT source/drain regions are degenerately doped, the Fermi level in a $n$-channel TFT source region can be assumed to be located at the conduction band edge, and the Fermi level in a $p$-channel TFT source region can be assumed to be located at the valence band edge. Therefore, the respective $n$-channel and $p$-channel leakage activation energies are

$$E_{a0n} = E_c - E_F$$

and

$$E_{a0p} = E_F - E_v,$$

where $E_c$, $E_v$, and $E_F$ are the conduction-band-edge energy, valence-band-edge energy, and the Fermi level in the channel region, respectively. From these two equations, it follows that

$$E_{a0n} + E_{a0p} = E_c - E_v = E_g$$

where $E_g$ is the bandgap of the channel material. The bandgap and the location of the Fermi level within the bandgap of a TFT channel film can thus be determined from the leakage activation energies. Table 6.8 provides a summary of the leakage activation energies (taken from Figure 6.9) and bandgap energies for poly-Si and poly-Si$_{0.8}$Ge$_{0.2}$. These results indicate that the Fermi level in hydrogenated poly-
Table 6.8: Comparison of poly-Si and poly-Si$_{0.8}$Ge$_{0.2}$ TFT leakage activation energies and bandgap energies.

<table>
<thead>
<tr>
<th>TFT channel material</th>
<th>$E_{a0n}$ (eV)</th>
<th>$E_{a0p}$ (eV)</th>
<th>$E_g$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>poly-Si$<em>{0.8}$Ge$</em>{0.2}$</td>
<td>0.39</td>
<td>0.51</td>
<td>0.90</td>
</tr>
<tr>
<td>poly-Si</td>
<td>0.52</td>
<td>0.51</td>
<td>1.03</td>
</tr>
</tbody>
</table>

Si$_{0.8}$Ge$_{0.2}$ is located 0.06 eV above midgap, so that it is $n$-type; in contrast, the Fermi level in hydrogenated poly-Si is located 0.05 below midgap, so that it is slightly $p$-type. The 0.13 eV reduction in bandgap seen for poly-Si$_{0.8}$Ge$_{0.2}$ compared to poly-Si is intermediate to the reductions observed for unstrained single-crystalline Si$_{1-x}$Ge$_x$ and strained single-crystalline Si$_{1-x}$Ge$_x$ [77, 76, 78, 79].

6.1.3 Effective Density-of-States Distribution in Poly-Si$_{0.8}$Ge$_{0.2}$

A method for the calculation of gap-state densities in amorphous semiconductors from field-effect measurements was first proposed by Suzuki et al. [129]. The field-effect conductance (FEC) analysis method provides useful information on the effective density of gap states in spite of some interpretation difficulties, such as distinguishing bulk states from interface states, and has been successfully applied to poly-Si [130]. In this section, the results of FEC analyses of hydrogenated poly-Si$_{0.8}$Ge$_{0.2}$ TFTs are presented.

The FEC method assumes the distribution of gap states in a TFT channel film to be spatially uniform, so that the energy-band bending $\psi$ can be described by a one-dimensional Poisson’s equation. Under the zero-temperature approximation, the
gap-state density \( N_g(E) \) (per unit volume) is then given by

\[
N_g(E_F + \psi_s) = \frac{\epsilon_s}{2q} \frac{\partial^2}{\partial x^2} \left( \frac{d\psi}{dx} \bigg|_{x=0} \right)^2.
\]

(6.5)

In equation 6.5, \( E_F \) is the Fermi energy, \( \psi_s \) is the energy-band bending at the channel/gate-dielectric interface (where \( x = 0 \)), \( \epsilon_s \) is the dielectric constant of the channel semiconductor material, and \( q \) is the electronic charge. The electric field at the channel/gate-dielectric interface is given by

\[
\frac{d\psi}{dx} \bigg|_{x=0} = -\frac{\epsilon_{ox}}{\epsilon_s} \left( \frac{V_G - V_{FB} - \psi_s}{t_{ox}} \right),
\]

(6.6)

where \( \epsilon_{ox} \) and \( t_{ox} \) are the dielectric constant and thickness of the gate-dielectric (oxide) layer, respectively, \( V_{FB} \) is the flat-band voltage, and \( V_G \) is the gate voltage. The density of gap states is determined from Equations 6.5 and 6.6 once the flat-band voltage and the relationship between \( V_G \) and \( \psi_s \) are known. The flat-band voltage is determined as the voltage where \( T(d(\log I_{DS})/dV_G) \) is temperature independent. The relationship between \( V_G \) and \( \psi_s \) is determined by the “temperature method”:

\[
q\psi_s = \Delta E(0) - \Delta E(V_G),
\]

(6.7)

where \( \Delta E(V_G) \) is the slope of the \( \ln(dI_{DS}/dV_G) \)-vs.-1/\( kT \) plot, determined by the method of least squares, for a gate bias \( V_G \).

The FEC method was used to derive the effective density-of-states (DOS) distribution shown in Figure 6.10 for hydrogenated poly-Si\(_{0.8}\)Ge\(_{0.2}\) from the subthreshold \( I-V \) measurements described in the previous section. The valence-band-edge and conduction-band-edge energies, determined from the data in Table 6.8 using Equations 6.2 and 6.3, are delineated for reference. The data in Figure 6.10 confirm that relatively high trap-state densities exist in the poly-Si\(_{0.8}\)Ge\(_{0.2}\) bandgap (roughly an order of magnitude higher than in poly-Si \([101]\]) and that the densities are somewhat higher in the upper half of the bandgap than in the lower half.

It is likely that the hydrogenated Si\(_{0.8}\)Ge\(_{0.2}\) films used in this work contain a relatively high density of Ge dangling bonds, since studies of hydrogenated amorphous
Figure 6.10: Effective density of gap states in undoped, hydrogenated poly-Si_{0.8}Ge_{0.2}.

Si_{1-x}Ge_x alloys have found that hydrogen attaches preferentially to Si rather than to Ge [131]. These dangling-bond states can partially account for the high density of states seen near the midgap energy (Figure 6.10), while the inherently larger proportion of strained-bond defects in an alloy material can partially account for the higher "tail" states near the band edges.

6.2 Poly-Si_{1-x}Ge_x TFT Technology Issues

Improvements in the crystallization and defect-passage processes are needed in order to reduce the effective density of trap states within the poly-Si_{1-x}Ge_x bandgap and thereby obtain improvements in TFT performance. In this section, the results of initial investigations of the crystallization behavior, SiO_2-interface properties, and hydrogenation of Si_{1-x}Ge_x films are briefly presented.
6.2.1 Crystallization of LPCVD Si$_{0.8}$Ge$_{0.2}$ Films by Low-Temperature Annealing

Since amorphous-phase deposition and subsequent crystallization is the preferred method for preparing high-quality TFT films with low surface roughness, low strain, and high structural perfection [55], the crystallization behavior of amorphous Si$_{0.8}$Ge$_{0.2}$ films was studied.

For an LPCVD film, a transition temperature exists below which the film is deposited in amorphous form. This transition temperature is approximately 500°C for Si$_{0.8}$Ge$_{0.2}$ (compared to ~550°C for Si) [132]. In this study, Si$_{0.8}$Ge$_{0.2}$ was deposited at 475°C and ~0.3 torr onto thermally oxidized silicon wafers, to a thickness of 100 nm; these films were then annealed in a N$_2$ ambient for 24 hours at either 500°C or 550°C, and subsequently analyzed using X-ray diffraction (XRD) and TEM.

As can be seen from Figure 6.11a, a 24-hour anneal at 500°C is insufficient for achieving the complete crystallization of an amorphous Si$_{0.8}$Ge$_{0.2}$ film. The 500°C-annealed film consists of crystalline regions in an amorphous background, and the XRD results (Figure 6.11b) indicate that these crystallites have a {110} orientation, similar to those in partially crystallized Si films [133]. In contrast, a 24-hour anneal at 550°C is sufficient for achieving complete crystallization. As shown in Figure 6.12, the 550°C-annealed film has an average grain size of 0.2 μm and a dominant {111} texture (preferred orientation). This grain size is somewhat larger than the 0.15 μm grain size obtained when a slightly higher deposition temperature of 490°C is used (Figure 6.5). The grains in each of the 550°C-crystallized films contain many {111} microtwin defects. These defects may partially account for the relatively high trap-state densities shown in Figure 6.10. For comparison, a poly-Si$_{0.8}$Ge$_{0.2}$ film deposited at 550°C is shown in Figure 6.13. The as-deposited polycrystalline film has a considerably smaller average grain size (0.07 μm) and less pronounced texture than either of the crystallized films. These results indicate that the crystallization behavior of Si$_{0.8}$Ge$_{0.2}$ is similar to that of Si, in that larger grain sizes are obtained by crystallization of an amorphous
Figure 6.11: Physical characterization of 0.1 μm-thick poly-Si₀.₈Ge₀.₂ film which was deposited at 475°C and ~0.3 torr, then annealed for 24 hours at 500°C: (a) plan-view TEM micrograph (b) X-ray diffraction data.

Figure 6.12: Physical characterization of 0.1 μm-thick poly-Si₀.₈Ge₀.₂ film which was deposited at 475°C and ~0.3 torr, then annealed for 24 hours at 550°C: (a) plan-view TEM micrograph (b) X-ray diffraction data. The average grain size is 0.2 μm.
Figure 6.13: Physical characterization of 0.1 μm-thick poly-Si$_{0.8}$Ge$_{0.2}$ film which was deposited at 550°C and ~0.2 torr: (a) plan-view TEM micrograph (b) X-ray diffraction data. The average grain size is 0.07 μm.

film (rather than directly by polycrystalline deposition) and by using lower deposition temperatures [134]. Grain sizes suitable for achieving good TFT characteristics can be obtained by 475°C deposition and 24-hour 550°C crystallization. However, a subsequent higher-temperature anneal (e.g. rapid thermal anneal) may be needed to reduce the density of intra-grain defects. For a 500°C crystallization process, an anneal time greater than 24 hours is required to completely crystallize a 100 nm-thick film.

6.2.2 Effect of Ge at the Si/SiO$_2$ Interface

The electrical effect of Ge at the Si/SiO$_2$ interface was studied by fabricating simple MOS capacitor structures on n-type Si wafers, with different areal densities of Ge located at the Si/SiO$_2$ interface. Ge was implanted into the starting substrates at an energy of 40 keV, to doses ranging from $1 \times 10^{11}$ to $1 \times 10^{14}$ cm$^{-2}$. The implanted
wafers were then oxidized at 900°C in steam to obtain a 0.14 μm-thick SiO$_2$ layer, thus entirely consuming the implanted region of the silicon and piling up the Ge at the SiO$_2$/Si interface [41]. Because the resulting concentrations of Ge at the SiO$_2$/Si interface are too low to be accurately detected by physical characterization methods, no physical characterizations were performed on these wafers. After the oxide was etched back (in 50:1 H$_2$O:HF) to a thickness of 0.05 μm, pure aluminum was sputtered onto the oxide and patterned to form gates for C-V measurements, and the wafers were annealed in forming gas at 400°C.

Measurements of the oxide fixed charge density ($Q_f$) and interface trap density ($D_{it}$) were obtained from high-frequency (100 kHz) and quasi-static (ramp rate = 10 mV/s) C-V measurements, and are shown in Figure 6.14. The presence of Ge at the SiO$_2$/Si interface was found to have no significant effect on the fixed charge: $N_f$ remains positive, does not vary significantly with Ge-implant dose, and is no higher for a Ge-implanted wafer than for a non-implanted wafer. However, the presence of Ge was found to affect the interface trap density: $D_{it}$ increases noticeably for Ge interface densities greater than 1×10$^{13}$ cm$^{-2}$, which corresponds to ~1 atomic percent Ge in Si at the oxide interface; at a Ge density of 1×10$^{14}$ cm$^{-2}$, which corresponds to ~10 atomic percent Ge, $D_{it}$ has increased to 1×10$^{11}$ cm$^{-2}$eV$^{-1}$. These findings show that the presence of Ge at the SiO$_2$/Si interface mainly affects the interface trap density, and not the fixed charge density. The increase in trap density may be attributed to unpassivated Ge bonds at the SiO$_2$/Si interface. This would partially account for the relatively high midgap state density shown in Figure 6.10, if 275°C post-H$^+$-implant annealing is not sufficient for passivation of Ge-associated defects. These results indicate that it would be inadvisable to use a thermally grown oxide as the gate dielectric in a poly-Si$_{1-x}$Ge$_x$ TFT technology, since Ge tends to accumulate at the oxidizing interface.
Figure 6.14: Interface trap density and fixed charge density (determined from high-frequency and quasi-static \(C-V\) measurements) as a function of the implanted Ge dose. The gate oxide was thermally grown in steam at 900°C, to pile up all of the Ge at the Si/SiO\(_2\) interface.
6.2.3 Hydrogenation of Poly-$\text{Si}_{1-x}\text{Ge}_x$ TFTs

Hydrogenation by $\text{H}^+$ ion implantation and subsequent thermal annealing is an effective method for improving poly-$\text{Si}_{1-x}\text{Ge}_x$ TFT performance, as can be seen from the data presented in sections 6.1.1 and 6.1.2. The effect of post-implant annealing temperature was therefore studied in order to determine the optimal temperature for efficient defect passivation in poly-$\text{Si}_{1-x}\text{Ge}_x$ TFTs.

$P$-channel poly-$\text{Si}_{0.8}\text{Ge}_{0.2}$ TFTs fabricated using the high-temperature process described in section 6.1.1 (Table 6.5) were measured prior to hydrogenation and then implanted with $\text{H}^+$, to a dose of $1\times10^{16}$ cm$^{-2}$. The devices were then annealed in forming gas at temperatures ranging from 250°C up to 375°C. Typical values of TFT mobility, leakage, subthreshold slope, and $I_{\text{ON}}/I_{\text{OFF}}$ ratio measured after each successive anneal are plotted in Figures 6.15 and 6.16. The data show that although the higher post-implant annealing temperatures (350°C and 375°C) result in the highest mobilities, a slightly lower temperature of 325°C is optimal because it yields the lowest leakage, steepest subthreshold slope, and highest $I_{\text{ON}}/I_{\text{OFF}}$ ratio. This temperature is lower than the optimal temperature of 375°C for $n$-channel poly-Si TFTs [135]. It should be noted that the optimal annealing temperature for $n$-channel devices may be different from that for $p$-channel devices; also, a two-step anneal (i.e. a high-temperature anneal followed by a low-temperature anneal) may ultimately be required for the optimization of this hydrogenation method, to effectively passivate Si-associated defects as well as Ge-associated defects.

6.3 Discussion

In this work, $p$-channel and $n$-channel TFTs have been successfully demonstrated in poly-$\text{Si}_{1-x}\text{Ge}_x$ films, and a low-temperature ($\leq 550^\circ\text{C}$) process has been shown to yield devices with well-behaved characteristics, proving that reduced thermal budgets can be used for Si$_{1-x}$Ge$_x$ technologies. It should be noted that the TFT fabrication processes used in this work were not optimized, and that superior device performance
Figure 6.15: Leakage and peak effective hole mobility for p-channel poly-Si$_{0.75}$Ge$_{0.25}$ TFTs. (Measurements were performed before hydrogenation, then after H$^+$ implantation, following each anneal at successively higher temperatures. The gate voltages were swept from 20 V to -30 V.)
Figure 6.16: Inverse subthreshold slope and $I_{ON}/I_{OFF}$ ratio for $p$-channel poly-Si$_{0.75}$Ge$_{0.25}$ TFTs. (Measurements were performed before hydrogenation, then after H$^+$ implantation, following each anneal at successively higher temperatures. The gate voltages were swept from 20 V to -30 V.)
should be achievable with process improvements which reduce the effective density of trap states in the poly-Si$_{1-x}$Ge$_x$ channel films.

The initial TFT studies have focused on poly-Si$_{1-x}$Ge$_x$ films with relatively low Ge content to avoid potential problems with high leakage currents associated with a much smaller energy band gap. The data presented in Section 4.3 indicate that Ge mole fractions greater than $\sim 0.15$ are sufficient for achieving substantial reductions in thermal-budget requirements for dopant activation. Experimentally, TFT leakage current has been found to be dependent on shallow trap states in the energy band gap of the channel film [128]. Therefore, the reduction of tail-state densities is of paramount importance in attaining low-leakage devices in poly-Si$_{1-x}$Ge$_x$ films. Considerable reductions from the levels seen in Figure 6.10 for the low-temperature-processed Si$_{1-x}$Ge$_x$ films used in this work should be achievable through improvements in the crystallization and defect-passivation processes, neither of which were optimized in this work. As noted in Section 6.1.2, the leakage current is also exponentially dependent upon the potential barrier height which exists at the source junction. Due to the smaller Si$_{1-x}$Ge$_x$ energy band gap, an undoped-channel poly-Si$_{1-x}$Ge$_x$ TFT may have a lower leakage activation energy in comparison to an undoped-channel poly-Si TFT, which may result in a higher leakage current (depending upon the nature of the tail-state traps). The channel region can be selectively doped (e.g. by masked ion implantation) to increase the channel-to-source barrier height and thereby reduce the leakage current. However, a trade-off for channel doping will exist between the leakage current and other TFT performance parameters such as the mobility, threshold voltage, and subthreshold slope.

An initial investigation of the crystallization behavior of Si$_{1-x}$Ge$_x$ showed that a lower deposition temperature yields larger final average grain size, which is beneficial to device performance, but that low-temperature ($\leq 550^\circ$C) crystallization results in microtwin defects, which are detrimental to device performance. Short-time, higher-temperature annealing (e.g. rapid thermal annealing for low-thermal-budget processing) may be required in order to achieve low intra-grain defect densities.
Chapter 6. Polycrystalline Si$_{1-x}$Ge$_x$ Thin-Film Transistors

The presence of Ge at the Si/SiO$_2$ interface was found to be correlated with an increase in the interface trap-density, possibly attributable to dangling Ge bonds; unpassivated interface traps would be manifest in the effective density-of-states distribution near midgap, which may partly account for the relatively high midgap-state densities observed in the poly-Si$_{1-x}$Ge$_x$ films in this work. Because Ge tends to pile up at the oxidizing interface during the oxidation of Si$_{1-x}$Ge$_x$ [42], problems with high densities of trap states will be exacerbated by the use of a thermally grown oxide as the gate dielectric for poly-Si$_{1-x}$Ge$_x$ TFTs.

The effect of post-H$^+$-implant annealing temperature on various TFT performance parameters was studied, and an optimal temperature of 325°C was found. A corresponding optimal H$^+$ implant dose was not determined, since the optimal dose is expected to change with variations in the TFT fabrication process which affect the grain structure of the channel poly-Si$_{1-x}$Ge$_x$ film (i.e., a true optimum dose does not exist).

The results of this initial work indicate that trap-state densities may inherently be somewhat higher in poly-Si$_{1-x}$Ge$_x$ films than in comparably processed poly-Si films, so that a commensurately higher dose of hydrogen may be required for poly-Si$_{1-x}$Ge$_x$ films in order to achieve device performance comparable to that achieved in poly-Si films. Since hydrogenation studies of poly-Si TFTs have found optimal H$^+$ implant doses to be in the mid-$10^{15}$ cm$^{-2}$ range [136, 135] this would suggest that very high H$^+$ implant doses ($\gg 10^{15}$ cm$^{-2}$) should be used for poly-Si$_{1-x}$Ge$_x$; such high doses are impractical, however. Alternative methods of hydrogenation such as high-density plasma hydrogenation [137, 138] may be more appropriate for efficient passivation of poly-Si$_{1-x}$Ge$_x$.

6.4 Conclusion

In summary, poly-Si$_{1-x}$Ge$_x$ is a promising material for CMOS integrated-circuit applications which require a low-temperature (< 600°C) TFT fabrication process, such
as active-matrix LCDs, linear image sensors, and three-dimensionally integrated electronics on low-cost glass substrates [54]. The fundamental properties of $Si_{1-x}Ge_x$ make it an attractive alternative to Si for applications in low-thermal-budget technologies, although some practical technological problems remain to be solved. Compared with a poly-Si TFT technology, a poly-$Si_{1-x}Ge_x$ TFT technology may ultimately be able to provide a lower-temperature, shorter-time processing capability at little or no expense to device performance. Although more work is needed to further develop and improve the fabrication process, the initial poly-$Si_{1-x}Ge_x$ devices show reasonable electrical characteristics. Upon optimization, a poly-$Si_{1-x}Ge_x$ TFT technology may open up a new domain of applications which were not accessible to Si TFT technologies.
Chapter 7

Conclusion

In this work, the physical and electrical properties of poly-Si$_{1-x}$Ge$_x$ films have been characterized, and their potential for application in MOS technologies has been assessed. As a result, a new variable-work-function gate material has been developed for use in submicrometer CMOS technologies and TFT technologies, and poly-Si$_{1-x}$Ge$_x$ TFT technologies have been successfully demonstrated for the first time.

7.1 Summary

Si$_{1-x}$Ge$_x$ alloy films can be routinely deposited in commercially available LPCVD equipment, and they can be etched using a standard flourine-based plasma-etch process. Practical deposition and etch rates are achieved, making the formation and patterning of poly-Si$_{1-x}$Ge$_x$ films very controllable processes. Films with Ge content up to 0.6 are not affected by various wet-chemical baths typically used in silicon-wafer processing. Si$_{1-x}$Ge$_x$ films are therefore compatible with conventional microelectronics fabrication techniques, and their use should not introduce significant additional process complexity into Si-based technologies.

Si$_{1-x}$Ge$_x$ has many properties which make it an attractive alternative to Si for MOS device applications:
Chapter 7. Conclusion

- Polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ films can be attained at significantly lower temperatures (down to $\sim 400^\circ\text{C}$) than polycrystalline Si films. For a given deposition temperature, the average grain size in a poly-$\text{Si}_{1-x}\text{Ge}_x$ film is larger than that in a poly-Si film, and it increases with Ge content.

- $\text{Si}_{1-x}\text{Ge}_x$ films can be heavily doped $p$-type to achieve resistivities significantly lower than that achievable in $p$-type Si films.

- Considerably lower annealing temperatures ($\sim 500^\circ\text{C}$) and lower boron implant doses can be used to obtain low resistivities in $\text{Si}_{1-x}\text{Ge}_x$ films, compared to Si films.

- The Hall hole mobility in poly-$\text{Si}_{1-x}\text{Ge}_x$ is higher than that in poly-Si, and increases with Ge content. The Hall electron mobility also increases with Ge content, for Ge content less than 35%.

- The work function of $p^+$ poly-$\text{Si}_{1-x}\text{Ge}_x$ can be modified by varying the Ge content. It is intermediate to the work functions of $n^+$ poly-Si and $p^+$ poly-Si, and decreases with increasing Ge content (by greater than 0.4 Volts from 0% Ge to 56% Ge).

$p^+$ poly-$\text{Si}_{1-x}\text{Ge}_x$ is a promising candidate for the gate material in CMOS technologies because of its lower resistivity (as compared with $p^+$ poly-Si) and its work function, which can be adjusted in order to achieve NMOS and PMOS devices which are more easily scalable to submicrometer dimensions. Because of its compatibility with low-temperature ($\leq 550^\circ\text{C}$) processing, $p^+$ poly-$\text{Si}_{1-x}\text{Ge}_x$ is also a good candidate for the gate material in TFT technologies which cannot afford large process thermal budgets, such as large-area electronics technologies (for sensors, displays, etc.).

$\text{Si}_{1-x}\text{Ge}_x$ TFTs are potentially advantageous for application in stacked-CMOS SRAM cells, because of their low thermal-budget requirement and their potentially high hole mobilities. The first poly-$\text{Si}_{1-x}\text{Ge}_x$ PMOS TFTs have been fabricated in
Chapter 7. Conclusion

this work, using either a high-temperature (950°C) or low-temperature (600°C) process. These devices exhibit good device characteristics, even though the fabrication processes were not optimized.

$Si_{1-x}Ge_x$ is an attractive alternative to Si especially for applications in technologies which have very limited thermal budgets, such as TFT AMLCD technologies. Compared with a poly-Si TFT technology, a poly-$Si_{1-x}Ge_x$ TFT technology should ultimately be able to provide a lower-temperature shorter-time processing capability at little or no expense to device performance. Poly-$Si_{1-x}Ge_x$ CMOS TFTs have been fabricated in this work using a maximum process temperature of 550°C, and these devices exhibit well-behaved electrical characteristics. Upon optimization, a poly-$Si_{1-x}Ge_x$ TFT technology should allow high-performance CMOS circuits to be realized on glass substrates, and thus aid the low-cost manufacturing of high-performance, high-density AMLCDs.

7.2 Recommendations for Future Work

This work constitutes an initial comprehensive investigation of poly-$Si_{1-x}Ge_x$ films. The deposition and properties of poly-$Si_{1-x}Ge_x$ need to be well understood before its potential for applications in MOS technologies can be fully realized. Therefore, further research is needed in the following areas:

1. **Deposition of poly-$Si_{1-x}Ge_x$ films:** The kinetics of the $Si_{1-x}Ge_x$ deposition process are not yet well understood. Several deposition models have been proposed by various researchers to describe the chemical vapor deposition of $Si_{1-x}Ge_x$ films, but none of these models satisfactorily predicts the low-temperature ($\leq 550^\circ C$) deposition behavior observed in this work; therefore, a more suitable deposition model needs to be developed. In addition, $Si_{1-x}Ge_x$ deposition using disilane ($Si_2H_6$) rather than silane as the silicon source gas should be investigated, since this process would provide higher deposition rates for improved throughput and diminish problems with oxygen incorporation. For applications
which require heavily doped films (e.g. MOS gate-electrode applications), the capability for in-situ doping can be useful and should thus be developed.

2. **Properties of poly-Si$_{1-x}$Ge$_x$ films:** The electrical properties of a polycrystalline film are dominated by its grain structure; therefore, the effects of deposition temperature, deposition pressure, and Ge content on Si$_{1-x}$Ge$_x$ crystal structure should be characterized. The crystallization (i.e. grain nucleation and grain growth) of amorphous Si$_{1-x}$Ge$_x$ films should also be studied in detail, since amorphous-phase deposition and subsequent crystallization is the preferred method for preparing high-quality films for TFT applications. An extensive study of dopant activation and segregation behavior, particularly for n-type dopants and for low annealing temperatures (< 600°C), should be conducted in order to completely assess the low-temperature process compatibility of poly-Si$_{1-x}$Ge$_x$ films.

3. **Poly-Si$_{1-x}$Ge$_x$ as a MOS gate material:** The electrical properties of poly-Si$_{1-x}$Ge$_x$ films can be expected to depend on strain, as is the case for single-crystalline Si$_{1-x}$Ge$_x$ films. Therefore, the effects of deposition temperature and deposition pressure on strain and hence on work function should be characterized as a function of Ge content, to facilitate the optimization of this gate material for various CMOS technologies. The oxidation behavior of poly-Si$_{1-x}$Ge$_x$ films should also be studied, since some oxidation of the gate electrode is typically needed to avoid gate-edge leakage problems resulting from source/drain ion implant damage. Finally, the diffusion of boron through poly-Si$_{1-x}$Ge$_x$ films into and through thin gate oxides should be investigated, to ascertain the severity of this problem (which results in MOSFET threshold-voltage shifts) for poly-Si$_{1-x}$Ge$_x$ gate technologies.

4. **Poly-Si$_{1-x}$Ge$_x$ TFT technology:** It is difficult to achieve a fair performance comparison between poly-Si$_{1-x}$Ge$_x$ TFTs and poly-Si TFTs at this time, because the fabrication processes used in this work were not optimized for Si$_{1-x}$Ge$_x$. 
Since TFT behavior is determined by the grain structure and perfection of the channel film, crystallization and defect-passivation processes which yield low-defect poly-Si$_{1-x}$Ge$_x$ films need to be developed in order to attain high-performance poly-Si$_{1-x}$Ge$_x$ devices. Alternative gate-dielectric materials may be better suited for poly-Si$_{1-x}$Ge$_x$ TFT technologies and should also be investigated. With optimized processes, TFT performance can be characterized as a function of Ge content, and the potential of poly-Si$_{1-x}$Ge$_x$ TFT technologies can be ascertained.
Bibliography


