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Department of Electrical Engineering and Computer Sciences
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EDUCATION

STANFORD UNIVERSITY, Palo Alto, California, USA

- 1994 Ph.D. in Electrical Engineering
Thesis: Applications of polycrystalline silicon-germanium thin films in metal-oxide-semiconductor technologies
Thesis Advisor: Professor Krishna C. Saraswat
- 1986 M.S. in Electrical Engineering
Coursework in integrated-circuit technology, semiconductor device physics, computer modelling of devices and fabrication processes, and solid-state physics
- 1984 B.S. in Electrical Engineering

EXPERIENCE

- 7/08 to present UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
Associate Dean for Research, College of Engineering
Overseeing operations of the Engineering Research Support Organization which provides research administration support to all research centers, departments, and affiliated organized research units in the UC Berkeley College of Engineering. Facilitating new research initiatives.
- 7/03 to present UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
Professor, Electrical Engineering and Computer Sciences
Research and instruction in the areas of nanometer-scale CMOS devices and technology, semiconductor memory devices, microelectromechanical systems technology, and large-area electronics.
- 8/06 to 6/08 UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
8/00 to 7/04 *Faculty Director*, UC Berkeley Microfabrication Laboratory (“Microlab”)
Responsible for overseeing lab operations and policies, setting new directions, and securing industrial support (in the form of grants and equipment, service, and cash donations) for this shared cleanroom research facility which supports a broad range of academic and industrial research. Liaison between Microlab and faculty as well as industry.
- 11/04 to 6/06 SYNOPSYS, INC., Mountain View, California, USA
Senior Director of Engineering, Advanced Technology Group
Development of new silicon technologies and associated intellectual property.
- 7/03 to 6/04 UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
Vice Chair for Graduate Matters, Electrical Engineering and Computer Sciences
Oversight and policy-setting for graduate admissions and the graduate study program.
- 5/00 to 10/04 PROGRESSANT TECHNOLOGIES, INC., Fremont, California, USA
Co-founder and President
Development and licensing of negative differential resistance transistor technology for low-cost, low-power integrated-circuit products. Negotiated sale of Progressant to Synopsys, Inc.
- 7/99 to 6/03 UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
Associate Professor, Electrical Engineering and Computer Sciences
Research and instruction in the areas of sub-100nm CMOS devices and technology, novel semiconductor memory devices, microelectromechanical systems technology, and maskless ion-beam lithography.

Resume of Tsu-Jae King Liu (UC Berkeley)

- 8/96 to 6/99 UNIVERSITY OF CALIFORNIA, Berkeley, California, USA
Assistant Professor, Electrical Engineering and Computer Sciences
Research and instruction in the areas of integrated-circuit devices and technology, thin-film transistor technology, and micro-electromechanical systems technology.
- 2/95 to 8/96 STANFORD UNIVERSITY, Palo Alto, California, USA
Consulting Assistant Professor, Electrical Engineering
Initiated and guided graduate-level research projects to explore applications of silicon-germanium ($\text{Si}_{1-x}\text{Ge}_x$) in large-area electronics technologies.
- 4/92 to 8/96 XEROX PALO ALTO RESEARCH CENTER, Palo Alto, California, USA
Member of Research Staff
Conducted research and development of polycrystalline Si (poly-Si) thin-film transistor (TFT) technologies for high-resolution, high-performance flat-panel display applications. Collaborated with researchers at various universities, national laboratories, and companies to develop materials, processing techniques, and tools for flat-panel display manufacture. Investigated novel applications of silicon-germanium ($\text{Si}_{1-x}\text{Ge}_x$) for TFT technologies. Participated in ARPA- and EPRI-sponsored workshops to support and provide guidance to university research programs pertaining to TFT technologies.
- 9/89 to 4/92 & 4/86 to 6/89 STANFORD UNIVERSITY, Palo Alto, California, USA
Research Assistant
Helped develop instructional semiconductor-particle-transport simulation program. Investigated gate-dielectric materials for germanium MOS transistors. Studied formation of epitaxial silicon-germanium ($\text{Si}_{1-x}\text{Ge}_x$) films on Si and the effects of Ge at the SiO_2/Si interface, for $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ heterojunction field-effect transistor applications. Modelled pyrometric temperature measurement. Developed a chemical vapor deposition technology for $\text{Si}_{1-x}\text{Ge}_x$ films. Characterized physical and electrical properties of polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ films. Investigated applications of $\text{Si}_{1-x}\text{Ge}_x$ in MOS technologies.
- 6/89 to 9/89 TEXAS INSTRUMENTS, INCORPORATED, Dallas, Texas, USA
Member of Technical Staff
Participated in development of real-time temperature sensor for single-wafer rapid-thermal-processing equipment.
- 9/85 to 4/86 & 9/84 to 6/85 STANFORD UNIVERSITY, Palo Alto, California, USA
Teaching Assistant and Student Undergraduate Advisor
Served as teaching assistant for courses in introductory electronics, linear systems, digital filters, signal processing, analog circuit laboratory, and semiconductor device physics. Duties included lecturing, supervision of laboratory sessions, individual tutoring, grading of problem sets and examinations, and providing curriculum counseling to undergraduate students.
- Summer 1985 HEWLETT-PACKARD COMPANY, Palo Alto, California, USA
Production Engineer
Wrote phase-linearity production test for the HP 8770A Arbitrary Waveform Synthesizer.
- Summer 1984 INTERNATIONAL BUSINESS MACHINES CORPORATION, San Jose, California, USA
Pre-Professional Engineer
Performed circuit simulations for microprocessor chip. Wrote computer programs for circuit analysis and product testing.
- Summer 1983 & Summer 1982 TEXAS INSTRUMENTS, INCORPORATED, Houston, Texas, USA
Engineering Aide
Performed circuit simulations for DRAM products. Wrote computer programs for data analysis and cost analysis.

PROFESSIONAL ACTIVITIES

Technical Program Committee Member, *2nd Int'l. Active Matrix Liquid Crystal Display Symposium* (1995)
Organizing Committee Member, *International Semiconductor Device Research Symposium* (1995, 1997, 1999)
Technical Program Committee Member, *Annual Device Research Conference* (1996, 1997, 1998)
Co-chair, *Active Matrix Liquid Crystal Displays Conference, IS&T/SPIE Symposium on Electronic Imaging Science and Technology* (1997)
Program Committee Member, *International Conference on Solid State Devices and Materials* (1997, 2002-2004)
Committee Member, *International Electron Devices Meeting, Subcommittee on Detectors, Sensors and Displays* (1998, 1999)
Int'l Technical Program Committee Member, *International SiGe Technology and Device Meeting* (2002, 2003, 2007)
Lead Organizer, *Symposium on CMOS Front-End Materials and Process Technology, 2003 MRS Spring Meeting*
Chair, Emerging Applications Committee, *Symposium on SiGe: Materials, Processing, and Devices, 2004 Fall ECS Meeting*
Organizer, *Symposium on Materials and Processes for Non-Volatile Memories, 2004 MRS Fall Meeting*
Committee Member, *2004 International Conference on Solid-State and Integrated-Circuit Technology*
Committee Member, *VLSI-Technology, Systems, and Applications Symposium* (2005, 2006, 2007)
Technical Committee Member, *Symposium on VLSI Technology* (2005, 2006, 2007, 2008, 2009, 2010)
Program Committee Member, *Silicon Nanoelectronics Workshop* (2005, 2006, 2007, 2008, 2009)
Technical Program Chair, *2010 Silicon Nanoelectronics Workshop*
Technical Committee Member, *2006 IEEE Nanotechnology Materials and Devices Conference*
Committee Member, *International Electron Devices Meeting, Subcommittee on CMOS Devices* (2007)
Committee Member, *International Electron Devices Meeting, Subcommittee on Solid-State Devices* (2008)
Member, *IEEE EDS VLSI Technology and Circuits Technical Committee* (2000-2001)
Member, *Emerging Research Devices Working Group, SIA Int'l Technology Roadmap for Semiconductors* (2002-present)
Member, *Process Integration, Devices, and Structures Working Group, SIA Int'l Technology Roadmap for Semiconductors* (2004-present)
Editor, *IEEE Electron Device Letters* (1999-2004)

INDUSTRIAL ACTIVITIES

Past and present technical consultant or advisory board member to various organizations including:

- Acorn Technologies, Inc. (Pacific Palisades, California)
- Advanced Process Development Group, Lawrence Livermore National Laboratory (Livermore, California), which spun out FlexICs (Milpitas, California)
- Advanced Technology Development Facility, SEMATECH (Austin, TX)
- Applied Materials (Santa Clara, CA)
- Rolltronics, Inc. (Menlo Park, California), 2000-2003
- Ronal Systems Corporation (Mountain View, California), 2003-2004
- SARIF (Vancouver, Washington)
- Silicon Clocks, Inc. (Berkeley, California)
- Symmorphix, Inc. (Sunnyvale, California)
- Transvision Microsystems (Milpitas, California)

HONORS AND AWARDS

Ross M. Tucker AIME Electronics Materials Award, 1992
NSF CAREER Award, 1998
DARPA Significant Technical Achievement Award (with Chenming Hu and Jeffrey Bokor), 2000
SRC Inventor Recognition Award, 2000, 2003, 2005
Outstanding Teaching Award (EE Division, EECS Department, UC Berkeley), 2003
MARCO/FCRP Inventor Recognition Award, 2006, 2007
IEEE Electron Devices Society Distinguished Lecturer, 2005-2008
National Academy of Engineering Lillian M. Gilbreth Lectureship, 2006
Conexant Systems Distinguished Professorship, 2009-present
IEEE Kiyo Tomiyasu Award, 2010

AFFILIATIONS

Member and past Faculty Advisor for CA-A Chapter, Tau Beta Pi
Fellow of the Institute of Electrical and Electronics Engineers
Member or past Member: Society for Information Display, Materials Research Society, Electrochemical Society

PERSONAL

U.S. citizen

PATENTS

1. U.S. Patent 5,250,818, "Low Temperature Germanium-Silicon on Insulator Thin-Film Transistor" (with K. C. Saraswat), October 5, 1993.
2. U. S. Patent 5,401,982, "Reducing Leakage Current in a Thin-Film Transistor with Charge Carrier Densities that Vary in Two Dimensions" (with M. G. Hack), March 28, 1995.
3. U. S. Patent 5,707,744, "Solid Phase Epitaxial Crystallization of Amorphous Silicon Films on Insulating Substrates" (with J. H. Ho), January 13, 1998.
4. U. S. Patent 5,893,949, "Solid Phase Epitaxial Crystallization of Amorphous Silicon Films on Insulating Substrates" (with J. H. Ho), April 13, 1999.
5. U. S. Patent 6,210,988, "Polycrystalline silicon germanium films for forming micro-electro-mechanical systems" (with A. Franke and R. T. Howe), April 3, 2001.
6. U.S. Patent 6,413,802, "FinFET transistor structures having a double gate channel extending vertically from a substrate and methods of manufacture" (with C. Hu, V. Subramanian, L. Chang, X. Huang, Y.-K. Choi, J. T. Kedzierski, N. Lindert, J. Bokor, and W.-C. Lee), July 2, 2002.
7. Taiwan Patent 154458, "Multiple-Thickness Gate Oxide Formed by Oxygen Implantation" (with Y.-C. King and C. Hu), August 16, 2002.
8. U.S. Patent 6,448,622, "Polycrystalline silicon-germanium films for micro-electromechanical systems application" (with A. Franke and R. T. Howe), September 10, 2002.
9. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode" (with D. K. Y. Liu), November 12, 2002.
10. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same" (with D. K. Y. Liu), January 28, 2003.
11. U.S. Patent 6,518,589, "Dual mode FET & logic circuit having negative differential resistance mode," February 11, 2003.
12. U.S. Patent 6,559,470, "Negative differential resistance field effect transistor (NDR-FET) and circuits using the same," May 6, 2003.
13. U.S. Patent 6,567,292, "Negative differential resistance (NDR) element and memory with reduced soft error rate," May 20, 2003.
14. U.S. Patent 6,594,193, "Charge pump for negative differential resistance transistor," July 15, 2003.
15. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device" (with D. K. Y. Liu), July 22, 2003.
16. U.S. Patent 6,664,601, Method of operating a dual mode FET & logic circuit having negative differential resistance mode," December 16, 2003.
17. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process" (with D. K. Y. Liu), January 20, 2004.
18. U.S. Patent 6,686,267, "Method for fabricating a dual mode FET and logic circuit having negative differential resistance mode," February 3, 2004.
19. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same" (with D. K. Y. Liu), February 3, 2004.
20. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR)

- characteristic" (with D. K. Y. Liu), February 17, 2004.
21. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold" (with D. K. Y. Liu), March 2, 2004.
 22. U.S. Patent 6,724,024, "Field effect transistor pull-up/load element," April 20, 2004.
 23. U.S. Patent 6,724,655, "Memory cell using negative differential resistance field effect transistors," April 20, 2004.
 24. U.S. Patent 6,727,548, "Negative differential resistance (NDR) element and memory with reduced soft error rate," April 27, 2004.
 25. U.S. Patent 6,753,229, "Multiple-thickness gate oxide formed by oxygen implantation" (with Y.-C. King and C. Hu), June 22, 2004.
 26. U.S. Patent 6,754,104, "Insulated-gate field-effect transistor integrated with negative differential resistance (NDR) FET," June 22, 2004.
 27. U.S. Patent 6,794,234, "Dual work function CMOS gate technology based on metal interdiffusion" (with I. Polishchuk, P. Ranade, and C. Hu), September 21, 2004.
 28. U.S. Patent, 6,795,337, "Negative differential resistance (NDR) elements and memory device using the same," September 21, 2004.
 29. U.S. Patent 6,806,117, "Methods of testing/stressing a charge trapping device," October 19, 2004.
 30. U.S. Patent 6,812,084, "Adaptive negative differential resistance device," November 2, 2004.
 31. U.S. Patent 6,847,562, "Enhanced read and write methods for negative differential resistance (NDR) based memory device," January 25, 2005.
 32. U.S. Patent 6,849,483, "Charge trapping device and method of forming the same," February 1, 2005.
 33. U.S. Patent 6,853,035, "Negative differential resistance (NDR) memory device with reduced soft error rate," February 8, 2005.
 34. U.S. Patent 6,855,994, "Multiple-thickness gate oxide formed by oxygen implantation" (with Y.-C. King and C. Hu), February 15, 2005.
 35. U.S. Patent 6,861,707, "Negative differential resistance (NDR) memory cell with reduced soft error rate," March 1, 2005.
 36. U.S. Patent 6,864,104, "Silicon on insulator (SOI) negative differential resistance (NDR) based memory device with reduced body effects," March 8, 2005.
 37. U.S. Patent 6,894,327, "Negative differential resistance pull-up element," May 17, 2005.
 38. U.S. Patent 6,912,151, "Negative differential resistance (NDR) based memory device with reduced body effects," June 28, 2005.
 39. U.S. Patent 6,933,548, "Negative differential resistance load element," August 23, 2005.
 40. U.S. Patent 6,956,262, "Charge trapping pull up element," October 15, 2005.
 41. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same" (with D. K. Y. Liu), November 29, 2005.
 42. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same" (with D. K. Y. Liu), December 6, 2005.
 43. U.S. Patent 6,979,580, "Process for controlling performance characteristics of a negative differential resistance (NDR) device," December 9, 2005.
 44. U.S. Patent 6,980,467, "Method of forming a negative differential resistance device," December 27, 2005.
 45. U.S. Patent 6,990,016, "Method of making memory cell utilizing negative differential resistance devices," January 24, 2006.
 46. U.S. Patent 7,005,711, "N-channel pull-up element and logic circuit," February 28, 2006.
 47. U.S. Patent 7,012,833, "Integrated circuit having negative differential resistance (NDR) devices with varied peak-to-valley ratios (PVRs)," March 14, 2006.
 48. U.S. Patent 7,012,842, "Enhanced read and write methods for negative differential resistance (NDR) based

- memory device,” March 14, 2006.
49. U.S. Patent 7,015,536, “Charge trapping device and method of forming the same,” March 21, 2006.
 50. U.S. Patent 7,016,224, “Two terminal silicon based negative differential resistance device,” March 21, 2006.
 51. U.S. Patent 7,060,524, “Methods of testing/stressing a charge trapping device,” June 13, 2006.
 52. U.S. Patent 7,067,873, “Charge trapping device” (with D. K. Y. Liu), June 27, 2006.
 53. U.S. Patent 7,084,407, “Ion beam extractor with counterbore” (with Q. Ji, K. Standiford, and K.-N. Leung), August 1, 2006.
 54. U.S. Patent 7,095,659, “Variable voltage supply bias and methods for negative differential resistance (NDR) based memory device,” August 22, 2006.
 55. U.S. Patent 7,098,472, “Negative differential resistance (NDR) elements and memory device using the same,” August 29, 2006.
 56. U.S. Patent 7,109,078, “CMOS compatible process for making a charge trapping device” (with D. K. Y. Liu), September 19, 2006.
 57. U.S. Patent 7,113,423, “Method of forming a negative differential resistance device,” September 26, 2006.
 58. U.S. Patent 7,141,858, “Dual work function CMOS gate technology based on metal interdiffusion” (with I. Polishchuk, P. Ranade, and C. Hu), November 28, 2006.
 59. U.S. Patent 7,186,619, “Insulated-gate field-effect transistor integrated with negative differential resistance (NDR) FET,” March 6, 2007.
 60. U.S. Patent 7,186,621, “Method of forming a negative differential resistance device,” March 6, 2007.
 61. U.S. Patent 7,187,028, “Silicon on insulator (SOI) negative differential resistance (NDR) based memory device with reduced body effects,” March 6, 2007.
 62. U.S. Patent 7,190,050, “Integrated circuit on corrugated substrate” (with V. Moroz), March 13, 2007.
 63. U.S. Patent 7,220,636, “Process for controlling performance characteristics of a negative differential resistance (NDR) device,” May 22, 2007.
 64. U.S. Patent 7,247,887, “Segmented channel MOS transistor” (with V. Moroz), July 24, 2007.
 65. U.S. Patent 7,254,050, “Method of making adaptive negative differential resistance device,” August 7, 2007.
 66. U.S. Patent 7,256,107, “Damascene process for use in fabricating semiconductor structures having micro/nano gaps” (with H. Takeuchi, E. P. Quevy, and R. T. Howe), August 14, 2007.
 67. U.S. Patent 7,265,008, “Method of IC production using corrugated substrate”(with V. Moroz), September 4, 2007.
 68. U.S. Patent 7,266,010, “Compact static memory cell with non-volatile storage capability,” September 4, 2007.
 69. U.S. Patent 7,453,083, “Negative differential resistance field effect transistor for implementing a pull up element in a memory cell,” November 18, 2008.
 70. U.S. Patent 7,494,933, “Method for achieving uniform etch depth using ion implantation and a timed etch,” February 24, 2009.
 71. U.S. Patent 7,508,031, "Enhanced segmented channel MOS transistor with narrowed base regions" (with Q. Lu), March 24, 2009.
 72. U.S. Patent 7,528,465, “Integrated circuit on corrugated substrate” (with V. Moroz), May 5, 2009.
 73. U.S. Patent 7,537,866, “Patterning a single integrated circuit layer using multiple masks and multiple masking layers,” May 26, 2009.
 74. U.S. Patent 7,557,009, "Process for controlling performance characteristics of a negative differential resistance (NDR) device," July 7, 2009.
 75. U.S. Patent 7,560,201, "Patterning a single integrated circuit layer using multiple masks and multiple masking layers," July 14, 2009.
 76. U.S. Patent 7,605,449, “Enhanced segmented channel MOS transistor with high-permittivity dielectric isolation material” (with Q. Lu), October 20, 2009.