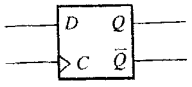
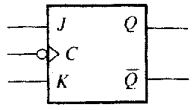


(a) Circuit symbol

C	D	Q_n
0	×	Q_{n-1}
1	×	Q_{n-1}
↑	0	0
↑	1	1

(b) Truth table
↑ indicates a transition from low to high

Figure 7.47 A positive-edge-triggered D flip-flop.



(a) Circuit symbol

C	J	K	Q_n	Comment
0	×	×	Q_{n-1}	Memory
1	×	×	Q_{n-1}	Memory
↓	0	0	Q_{n-1}	Memory
↓	0	1	0	Reset
↓	1	0	1	Set
↓	1	1	$\bar{Q}_{n-1}$	Toggle

(b) Truth table
↓ indicates a transition from low to high

Figure 7.50 Negative-edge-triggered JK flip-flop.

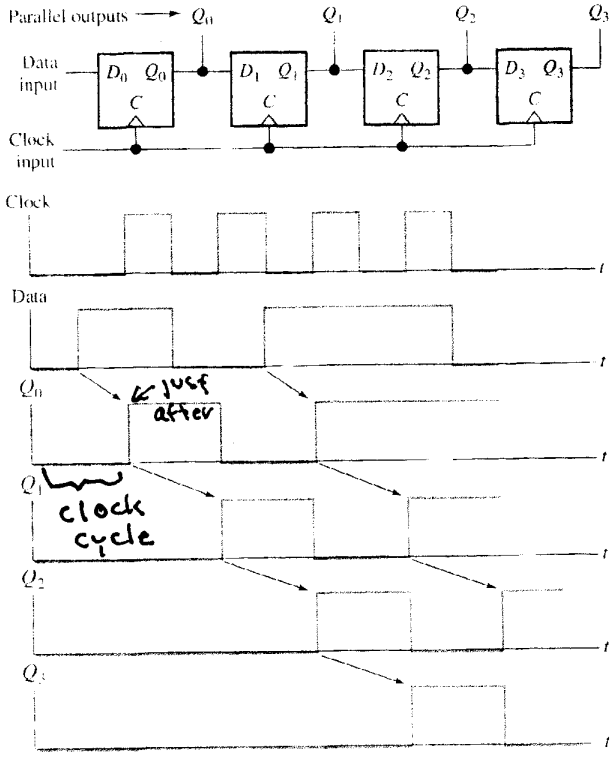


Figure 7.51 Serial-input parallel-output shift register.

Shift Register

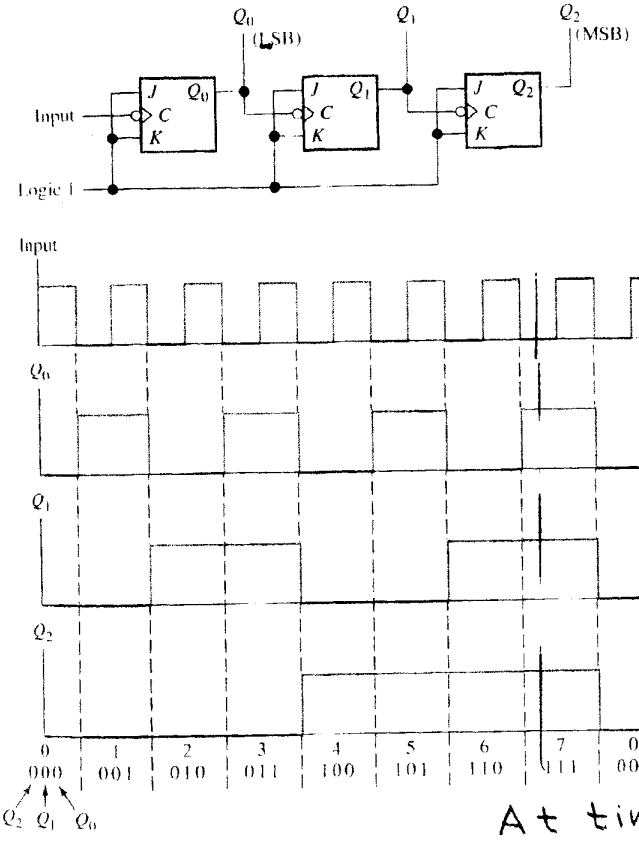


Figure 7.53 Ripple counter.

At time t 4+2+1 = 7 pulses

Ripple Counter