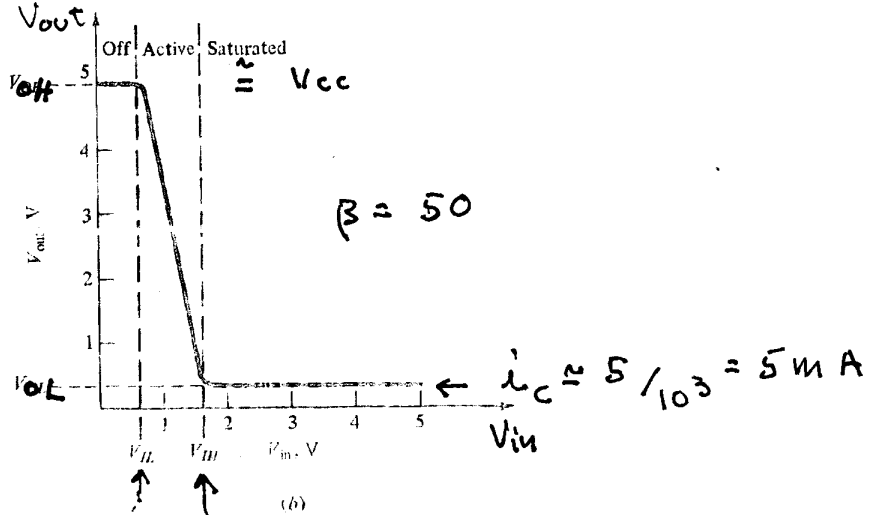
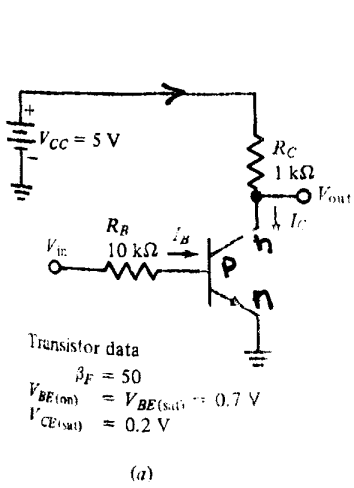
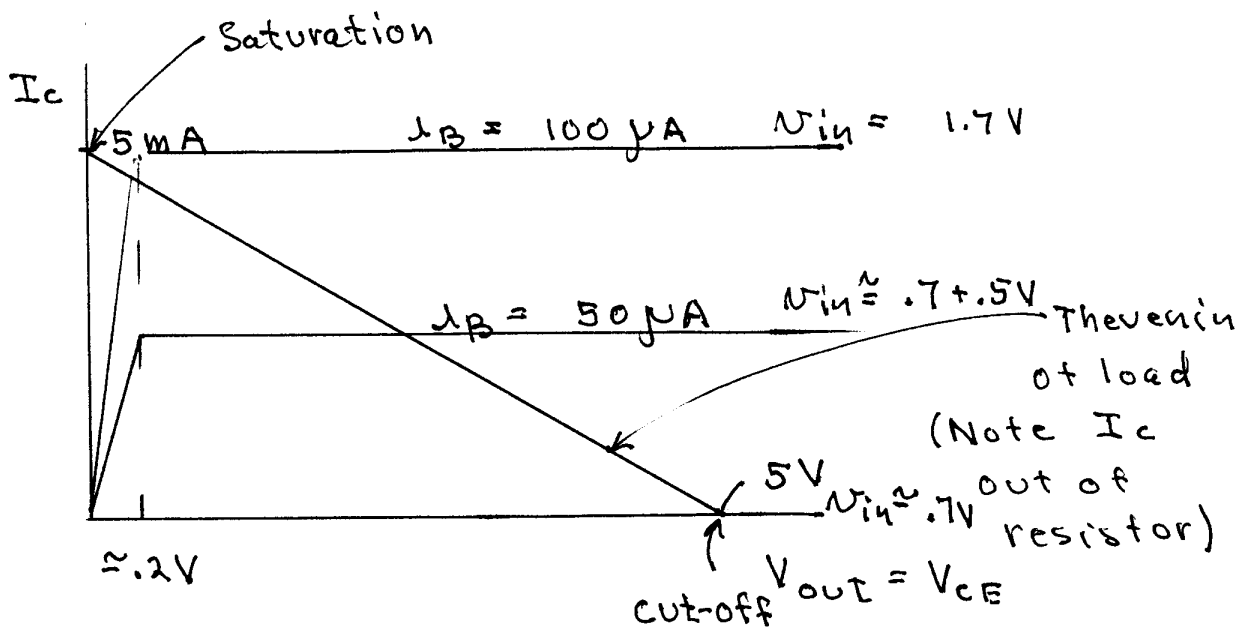


Transistor Inverter - Digital Application



$I_C \approx I_B = 0$
 base just barely on
 $\therefore V_{in} \approx 0.7 \text{ V}$

$I_C \approx 5 \text{ mA} = I_B \beta$
 $\therefore I_B \approx \frac{5 \text{ mA}}{50} = 100 \mu\text{A}$
 $V_{in} \approx 0.7 + 10 \text{ k}\Omega \times 100 \times 10^{-6}$
 $\approx 0.7 + 1 \approx 1.7 \text{ V}$



The NOR (or NAND) Gate

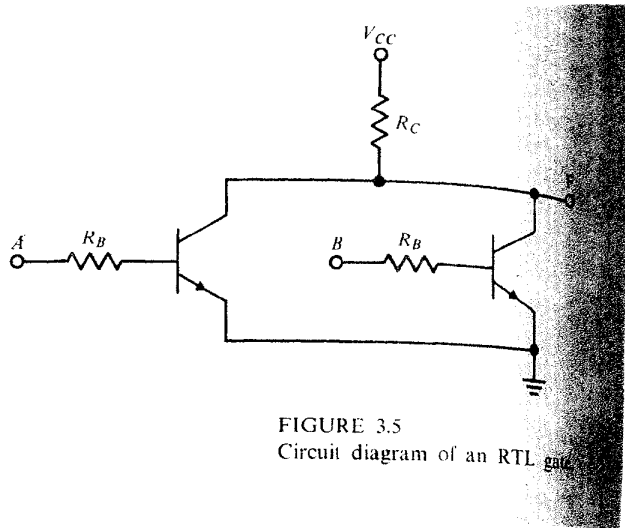


FIGURE 3.5
Circuit diagram of an RTL gate

Voltage level
HIGH = H
LOW = L

A	B	F
L	L	H
L	H	L
H	L	L
H	H	L

(a)

Positive logic
H = 1
L = 0

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

(b)

Negative logic
L = 1
H = 0

A	B	F
1	1	0
1	0	1
0	1	1
0	0	1

(c)

NOR

NAND

$$F = \overline{A + B}$$

$$F = \overline{A B}$$

By De Morgan's Th = $\overline{A} \overline{B}$

$$= \overline{A} + \overline{B}$$

Example $V_{BE(sat)} = 0.7V$
 $V_{CE(sat)} = 0.2V$

$$\beta_F = 50$$

$$R_B = 1k\Omega$$

$$V_{CC} = 3V$$

$$R_C = 2k\Omega$$

