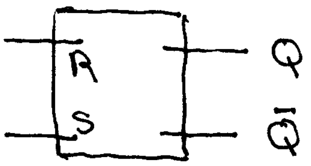
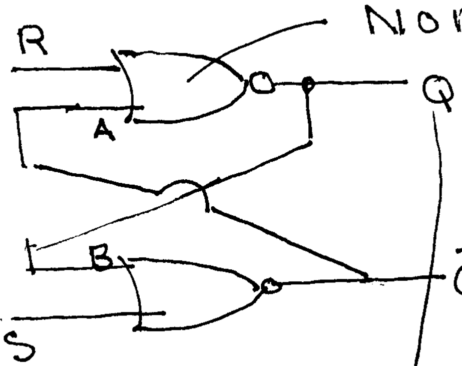
RS Flip-Flop → Simple Digital Design using NOR Gates



R	S	Q_{n+1}	$\bar{Q}_{n+1}$
0	0	Q_n	Q_n ← Doesn't change
1	0	low	high
0	1	high	low
1	1	↔ Avoid	

Simple Implementation

NOR Gate (Not OR)



$Q = \overline{R+A}$

$\bar{Q} = \overline{B+S}$

NOR Gate

R	A	Q
1	0	0
0	1	0
1	1	0
0	0	1

Input ; output of 2'nd

1st NOR $\quad Q = \overline{R + A} = \bar{R}\,\bar{A} = \bar{R}\,\bar{\bar{Q}} = \bar{R}\,(\overline{\overline{B+S}}) = \bar{R}\,(B+S)$

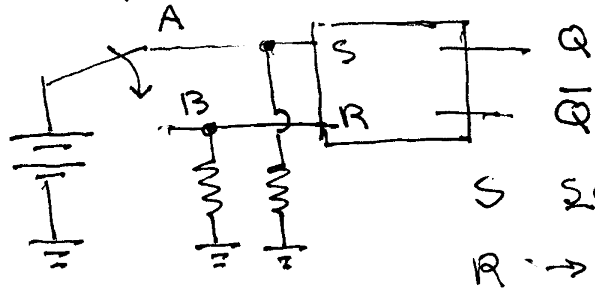
2nd NOR $\quad \bar{Q} = \bar{S}\,\bar{B} = \bar{S}\,\bar{Q} = \bar{S}\,(\overline{\overline{R+A}}) = \bar{S}\,(R+\bar{A})$

Input ; output of 1'st

R	S	Q	$\bar{Q}$
1	0	0	1
0	1	1	0
0	0	No Change	
1	1	Avoid	

Example Application

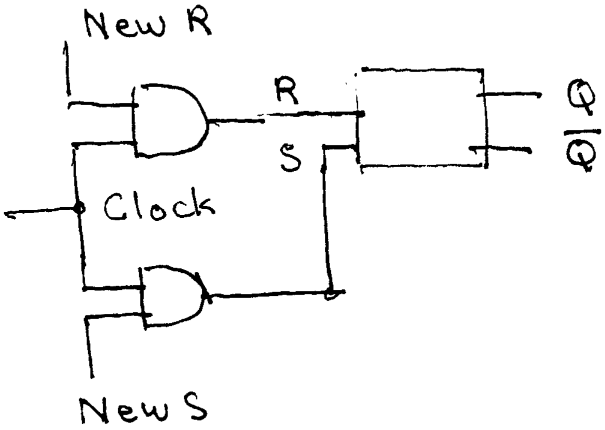
Simple De-Bouncer



S <u>Set</u> <u>goes</u> to 0 permanently

R → resets $\bar{Q}$ to 1 and Q to 0. Bounce at B does not matter since <u>0</u>, <u>0</u> does nothing

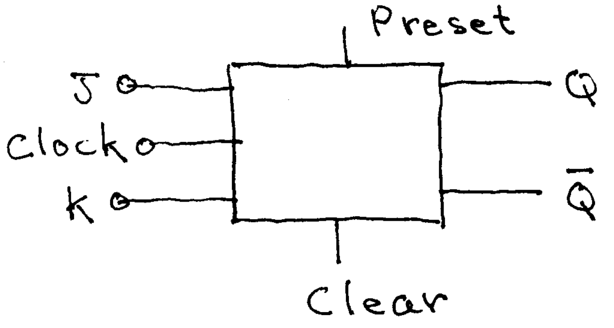
The Clocked RS Flip-Flop



Can also include a Clear and a Preset as inputs on NOR Gates of RS

Other types of Flip-Flops

JK Flip-Flop

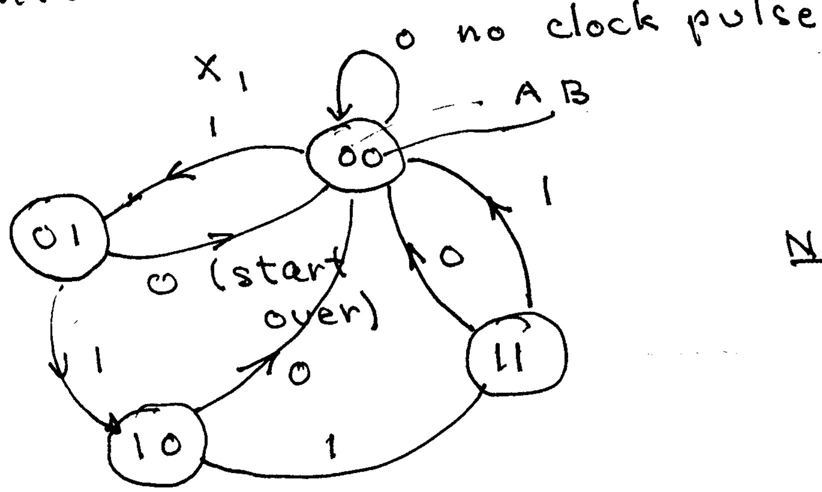


J	K	Q_n	After Pulse Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

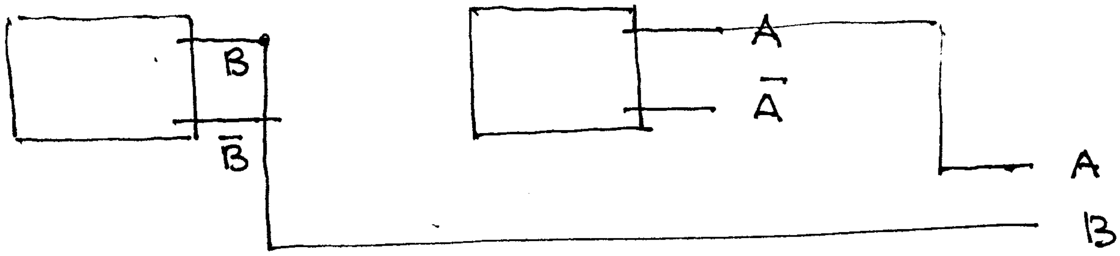
Applications: Frequency division
Ripple Counter.
Shift Registers.

State Diagrams - Example - 2 bit binary counter

State Diagram for the 2bit binary counter



Need 2 flip-flops



Excitation Table

Present State A	Present State B	X_1	Next State A	Next State B	J_A	K_A	J_B	K_B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	0	0	0	X	X	1
0	1	1	1	0	1	X	X	1
1	0	0	0	0	X	1	0	X
1	0	1	1	1	X	0	1	X
1	1	0	0	0	X	1	X	1
1	1	1	0	0	X	1	X	1

FF Inputs: J_A K_A J_B K_B

Now use Karnaugh Maps
for J_A and J_B, K_A & K_B

X_1 \ AB (present state)	00	01	11	10
0			X	X
1		1	X	X

$J_A = B X_1$

Similarly

$K_A = \bar{X}_1 + B = \overline{X_1 \bar{B}}$

$J_B = X_1$

$K_B = B$