The NOR (or NAND) Gate

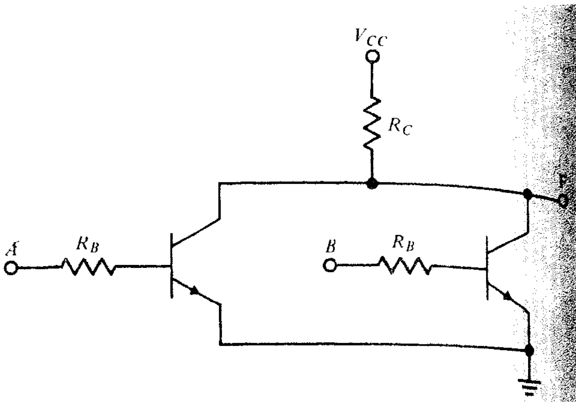

FIGURE 3.5
Circuit diagram of an RTL gate

Voltage level
HIGH = H
LOW = L

A	B	F
L	L	H
L	H	L
H	L	L
H	H	L

(a)

Positive logic
H = 1
L = 0

A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

(b)

NOR

Negative logic
L = 1
H = 0

A	B	F
1	1	0
1	0	1
0	1	1
0	0	1

(c)

NAND

$F = \overline{A + B}$ $\qquad$ $F = \overline{AB}$

By De Morgans Th $= \bar{A}\,\bar{B}$ $\qquad$ $= \bar{A} + \bar{B}$

Example $V_{BE(sat)} = .7V$ $\qquad$ $\beta_F = 50$

$V_{CE\,(sat)} = .2V$

$R_B = 1k\Omega$

$R_c = 2k\Omega$ $\qquad$ $V_{cc} = 3V$