

Problem Number One ) (Total 12: Logic Implementation)

a) 3/12 A logic implementation has four inputs, A, B, C, and D. The output is a logic 1 (high) when:

[ B is low AND (C is low OR D is low )] OR ( C is low AND A is low). All OR's refer to the inclusive OR function.

Write a Sum of Products expression for the output F.

$$F = \bar{B} (\bar{C} + \bar{D}) + \bar{C} \bar{A}$$

b) 3/12 Show the Karnaugh map for

$$\begin{aligned} G = \bar{B}\bar{C} + \bar{A}C + \bar{B} &= \bar{B}(\bar{C} + 1) + \bar{A}C \quad (1) \\ &= \bar{B} + \bar{A}C \end{aligned}$$

C \ AB	00	01	11	10
0	1	0	0	1
1	1	1	0	1

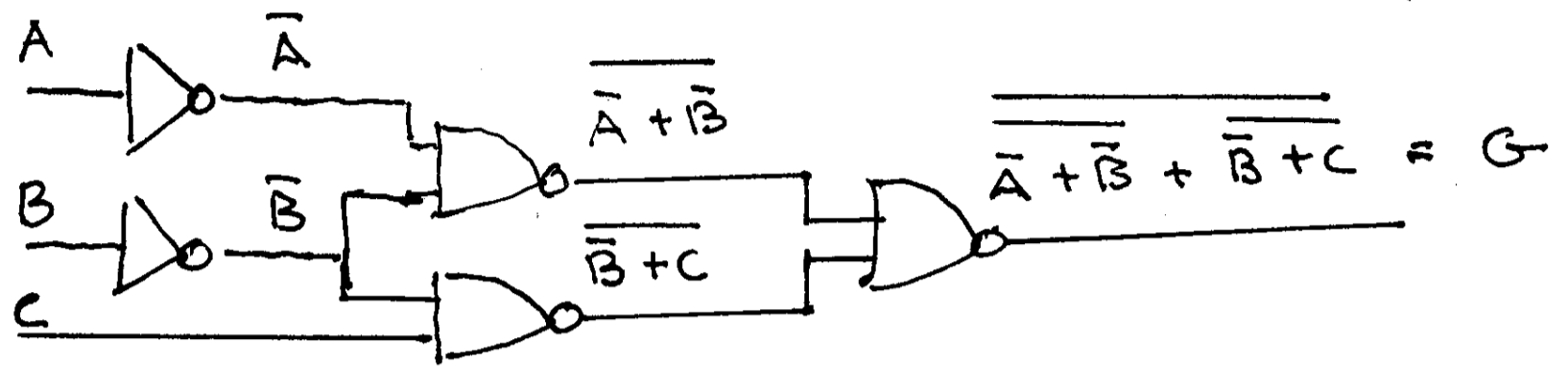
Handwritten annotations on the Karnaugh map:  
 - A circle around the '1' in the top-left cell (00, 0) is labeled  $\bar{B}$ .  
 - A circle around the '1' in the bottom-left cell (00, 1) is labeled  $\bar{A}C$ .  
 - A circle around the '1' in the bottom-middle cell (01, 1) is labeled  $\bar{A}C$ .  
 - A circle around the '1' in the bottom-right cell (10, 1) is labeled  $\bar{B}$ .

c) 3/12 Write down the product of sums implementation for G

$$\begin{aligned} \bar{G} &= AB + B\bar{C} \\ G &= \overline{AB + B\bar{C}} = \overline{AB} \overline{B\bar{C}} \\ &= (\bar{A} + \bar{B})(\bar{B} + C) \end{aligned}$$

$$G = \underline{(\bar{A} + \bar{B})(\bar{B} + C)}$$

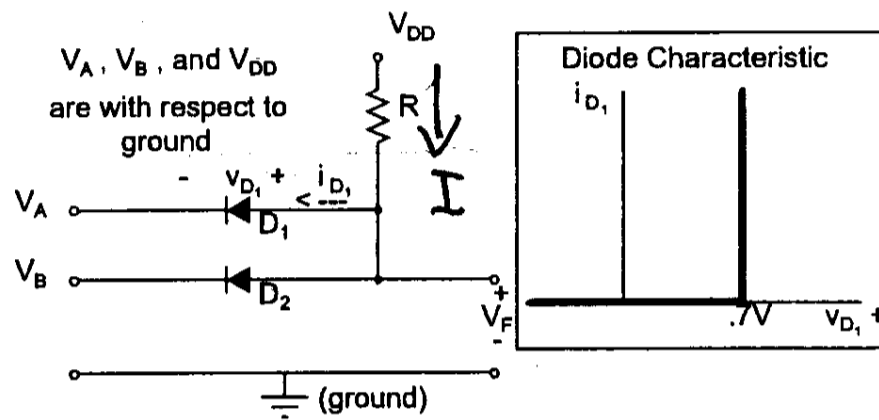
d) 3/12 Using only a minimum number of NOR gates (inverter included) implement the function G of part b)



$$\begin{aligned}
 \bar{G} &= \overline{A B + B \bar{C}} \\
 &= \overline{A B + B \bar{C}} \\
 &= \overline{A B} \overline{B \bar{C}} \\
 &= (\bar{A} + \bar{B})(\bar{B} + C) \quad \text{as in c)} \\
 &= \overline{\bar{A} + \bar{B}} \overline{\bar{B} + C} \\
 G &= \overline{\overline{\bar{A} + \bar{B}} + \overline{\bar{B} + C}}
 \end{aligned}$$

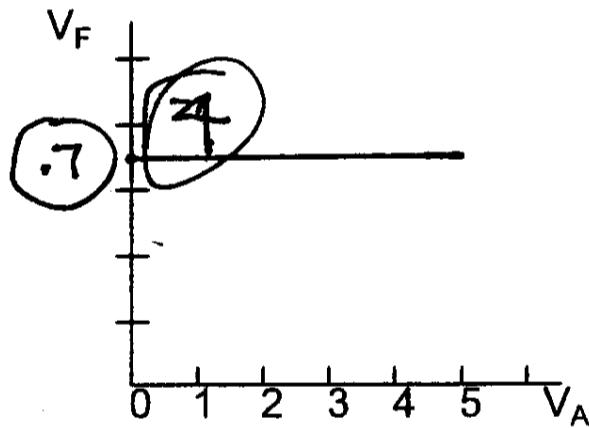
Problem Number Two ) (Total 12 Diode Logic Gate)

Given the circuit below along with the diode characteristic shown:



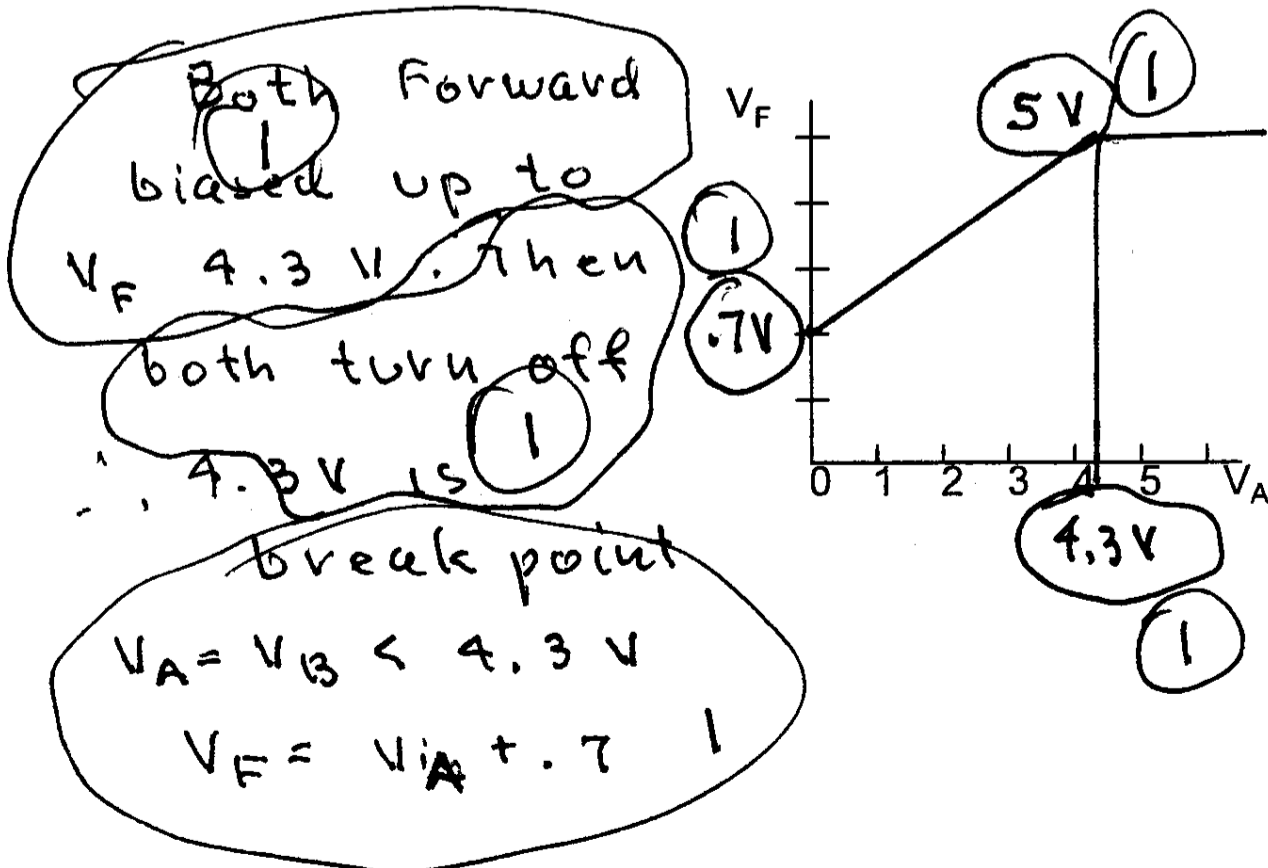
a) 4/12 Plot  $V_F$  versus  $V_A$  from 0 to five volts, with  $V_{DD} = 5$  Volts and  $V_B = 0$  Volts.

$V_B = 0$   
 $V_F = .7V$



$V_B = 0$   $D_2$  short <sup>(1)</sup>  
 $V_A > 0$   $D_1$  open <sup>(1)</sup>  
 Thus  $V_F = V_B + .7$  <sup>(1)</sup>  
 $= .7$  <sup>(1)</sup>  
 $I = \frac{V_{DD} - .7}{R}$  <sup>(1)</sup>

b) 4/12 Now let  $V_B = V_A$  and plot  $V_F$  versus  $V_A$  from 0 to five volts.



c) 4/12 Assuming positive logic, what type of gate is this?

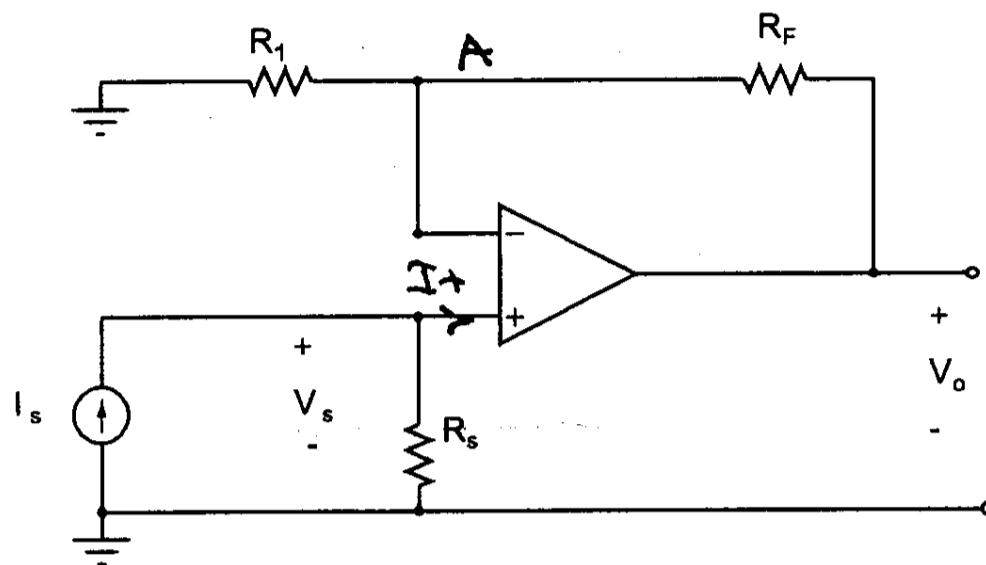
Truth <sup>2</sup> Table

$V_A$	$V_B$	$V_F$
0	0	0
0	1 <sup>2</sup>	0
1	0	0
1	1	1

It is a(n) = <sup>↑</sup> AND Gate

## Problem Number Three ) (Total 12 Operational Amplifier)

For the circuit shown below assume ideal operational amplifier conditions



a) 3/12 Find  $V_o/I_s$        $I_+ = 0 \quad \therefore V_s = I_s R_s$

$$V_A = V_s = I_s R_s$$

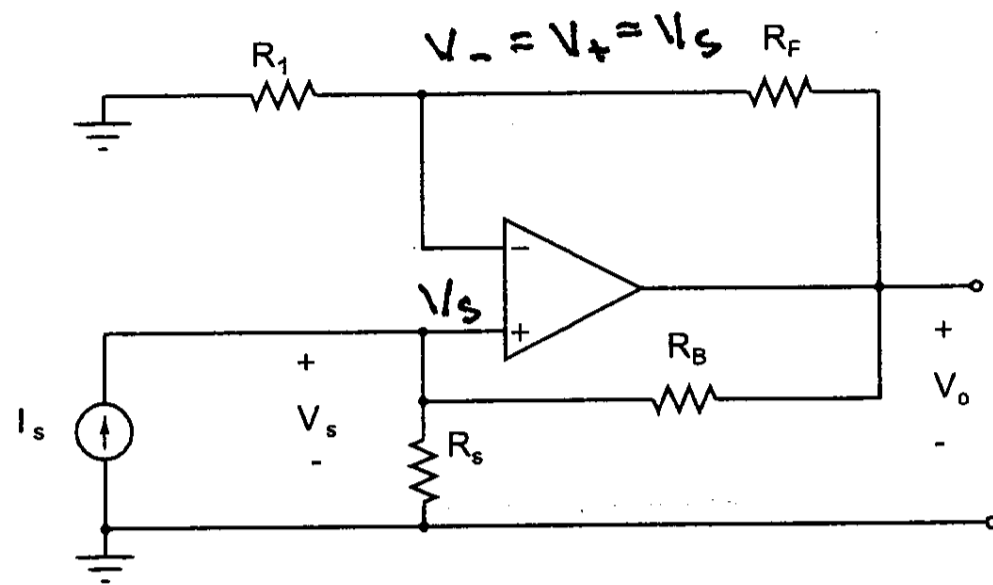
Node equation       $\frac{V_o - V_A}{R_F} = (V_A - 0)/R_1$

Thus  $V_o = I_s R_s R_F \left( \frac{1}{R_1} + \frac{1}{R_F} \right)$   
 $V_o/I_s = \frac{R_s}{R_1} (R_F + R_1)$

b) 3/12 What is the input resistance?

Input Resistance =            $R_s$

c)  $3/12$  A resistor is now added between the output and the + input.



Write the node equations at the positive and negative terminals of the operational amplifier in terms of  $I_s$ ,  $V_s$ ,  $V_o$ ,  $R_1$ ,  $R_f$ ,  $R_s$ , and  $R_b$

$$+ \text{ Node Eqn } \frac{V_s}{R_s} + \frac{V_s - V_o}{R_b} - I_s = 0 \quad \curvearrowright$$

$$- \text{ Node Eqn } \frac{V_o - V_s}{R_f} = V_s / R_1 \quad \textcircled{1}$$

$\textcircled{3}$

What is  $V_o/I_s$  including the added resistor?

Solve for  $V_s$  from (1)

$$\frac{V_o}{R_F} \approx V_s \left( \frac{1}{R_F} + \frac{1}{R_1} \right)$$

$$\text{Thus } V_s = \frac{R_1}{R_F + R_1} V_o$$

Sub in (2)

$$\left( \frac{1}{R_S} + \frac{1}{R_B} \right) \left( \frac{R_1}{R_F + R_1} \right) V_o - \frac{V_o}{R_B} - I_s = 0$$

$$\text{Thus } V_o/I_s = \frac{1}{\left( \frac{R_S + R_B}{R_S R_B} \frac{R_1}{R_F + R_1} - \frac{1}{R_B} \right)} = \frac{R_B}{\left( \frac{R_S + R_B}{R_F + R_1} \frac{R_1}{R_S} - 1 \right)}$$

d) 3/12 Does  $R_B$  provide negative or positive feedback? Why?

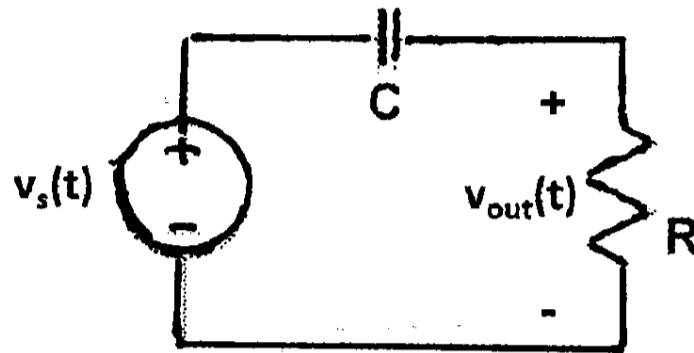
Feedback by  $R_B$  is = positive

Reason =  $\frac{V_o}{I_s}$  can  $\rightarrow \infty$

indicating that feed back  
is added in phase with  
input!

Problem Number Four) Steady State AC Analysis (Total 12)

For this entire, assume the circuits have been running for a long period of time, and all transient responses have died out. All voltages are specified in volts:



a) 2/12 Consider the circuit shown above. If  $v_s(t) = 1$  (DC), Determine  $v_{out}(t)$  in steady state?

$$v_{out}(t) = \underline{\quad 0 \quad}$$

b) 3/12 If  $v_s(t) = \cos(\omega t)$ , then  $v_{out}(t) = V_m \cos(\omega t + \theta)$ . Determine  $V_m$  and  $\theta$  as a function of  $R$ ,  $C$ , and  $\omega$ .

$$v_s = \frac{1}{2} e^{j\omega t}$$

$V_m$  is real

$$v_{out} = \frac{V_m}{2} e^{j(\omega t + \theta)}$$

$$v_{out} = \frac{R}{R + \frac{1}{j\omega C}} \times \frac{1}{2} e^{j\omega t} = \frac{V_m}{2} e^{j(\omega t + \theta)}$$

$$\frac{R}{(R^2 + (\frac{1}{\omega C})^2)^{1/2}} e^{-j \tan^{-1}(\frac{1}{\omega C R})} = V_m e^{j\theta}$$

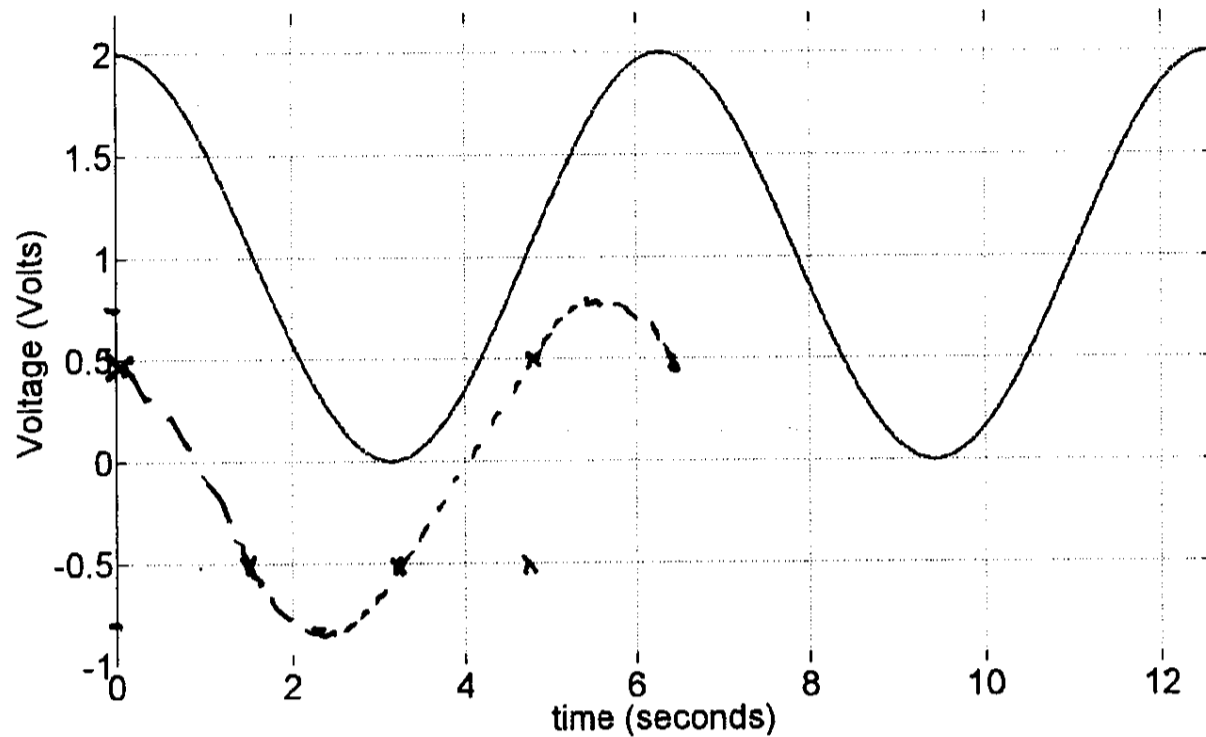
$$V_m = \underline{\quad \quad \quad}$$

$$\theta = \underline{\quad \tan^{-1}(\frac{1}{\omega C R}) \quad}$$

$$V_m = \frac{1}{(1 + (\frac{1}{\omega C R})^2)^{1/2}}$$



c) 3/12 A sketch of  $v_s(t)$  is shown below with  $v_s(t) = 1 + \cos(\omega t)$  and  $\omega = \frac{1}{RC} = 1 \text{ rad/s}$ . On the same axes, provide a sketch of  $v_{out}(t)$ , clearly indicating amplitude and phase.



$t$	$v_{out}$
$t = \frac{\pi}{2}$	$\frac{1}{\sqrt{2}} \cos \frac{3\pi}{4}$
	$= -\frac{1}{2}$
$t = \pi$	$\frac{1}{\sqrt{2}} \cos(\frac{5\pi}{4})$
	$= -\frac{1}{2}$
$t = \frac{3\pi}{2}$	$\frac{1}{\sqrt{2}} \cos(\frac{7\pi}{4})$
$= 4.71$	$= +\frac{1}{2}$
peak =	$\frac{1}{\sqrt{2}} = .708$

$$\omega RC = 1 \quad \theta = \tan^{-1} 1 = \frac{\pi}{4}$$

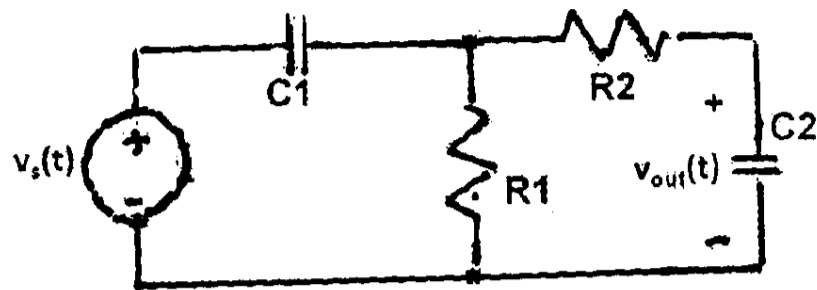
$$V_m = \frac{1}{(1+1)^{1/2}} = \frac{1}{\sqrt{2}}$$

$$v_{out} = \frac{1}{\sqrt{2}} \text{Re}(e^{j\pi/4 + j\omega t}) = \frac{1}{\sqrt{2}} \cos(\omega t + \frac{\pi}{4})$$

$$\begin{aligned} T &= 2\pi = 6.28 \\ T/2 &= \pi = 3.14 \\ T/4 &= \pi/2 = 1.58 \\ &1 \text{ rad/sec} \end{aligned}$$

d) 2/12 Of the three choices below, circle the one that best describes this circuit. (Hint: Look at your expression for  $V_m$  from Part b.)

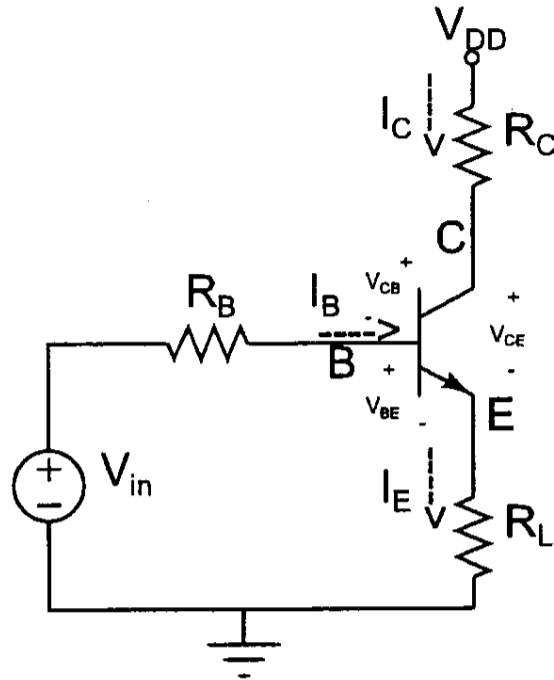
- Low pass filter - This circuit attenuates high frequencies and allows low frequencies to pass with minimal attenuation.
- High pass filter - This circuit attenuates low frequencies and allows high frequencies to pass with minimal attenuation.
- Band pass filter - This circuit attenuates both low and high frequencies and allows a band of frequencies to pass with minimal attenuation.



e) 2/12 Now consider the slightly modified circuit shown above. Of the three choices below, circle the one that best describes this circuit. (Hint: Very little math is needed for this problem! Use your intuition about the behavior of this circuit at very low frequencies and very high frequencies)

- Low pass filter - This circuit attenuates high frequencies and allows low frequencies to pass with minimal attenuation.
- High pass filter - This circuit attenuates low frequencies and allows high frequencies to pass with minimal attenuation.
- Band pass filter - This circuit attenuates both low and high frequencies and allows a band of frequencies to pass with minimal attenuation.

Problem Number 5 (Total 12 Bipolar Transistor)  
For the circuit shown below  $v_{in} = 4.6$  V.



a) 2/12 Use KVL to relate the voltages  $V_{CE}$ ,  $V_{BE}$ , and  $V_{CB}$  and KCL to relate the currents  $I_C$ ,  $I_B$ , and  $I_E$ .

Voltage relationship  $V_{CB} = V_{CE} - V_{BE}$

Current relationship  $I_B + I_C = I_E$

b) 3/12 Given  $V_{DD} = 5$  V,  $R_C = 1$  k $\Omega$ ,  $R_L = .5$  k $\Omega$ , and  $\beta = 40$  find  $I_C$  so that the transistor is biased such that  $V_{BE} = .7$  V and  $V_{CE} = .2$  V. (Hint: A KVL equation that includes  $I_C$  might help!)

KVL in collector circuit  $V_{DD} = I_C R_C + V_{CE} + I_E R_L$  for KVL

$\beta = 40 = \frac{\alpha}{1-\alpha} \therefore \alpha = \frac{\beta}{\beta+1} = \frac{40}{41}$

$\therefore V_{DD} = I_C + V_{CE} + I_C \left( \frac{1}{40} \times \frac{1}{2} \right)$  For  $I_E = I_C / \alpha$

$\therefore I_C = \frac{4.8}{\left(1 + \frac{41}{80}\right)} = \frac{4.8}{1.5125} I_C$  regardless of  $\alpha$   $I_C = 3.17$  mA

c) 2/12 Is the situation in b) the edge of saturation ( transistor acting like a short circuit ) or is it the edge of cut-off ( acting like an open circuit )?

Circuit is at edge of 2 Saturation

d) 3/12 Using the same parameters as given in b) (including  $V_{BE}$  and  $V_{CE}$ ) and also given that  $V_{in} = 4.5V$  determine the value of  $R_B$  (You may leave the answer in terms of  $I_C$  if you wish)

KVL in base loop (base-collector loop)

$$R_B I_B = V_{in} + V_{CE} + R_C I_C - V_{DD} \text{ from b) } \textcircled{1} \text{ For KVL}$$

$$\therefore R_B = \frac{(V_{in} - V_{BE} + V_{CE} + R_C (3.17 \text{ mA}))}{I_B} \textcircled{1} \text{ substituting for } I_B$$

$$= \frac{(4.5 - 0.7 + 0.2 + 3.17)}{3.17} \beta \text{ [k}\Omega\text{]} - \text{obtaining expression for } R_B \textcircled{1}$$

$$R_B = \underline{27.4 \text{ k}\Omega}$$

e) 2/12 What is the voltage  $V_E$  across  $R_L$ . Once again you may leave the answer in terms of  $I_C$  if you wish.

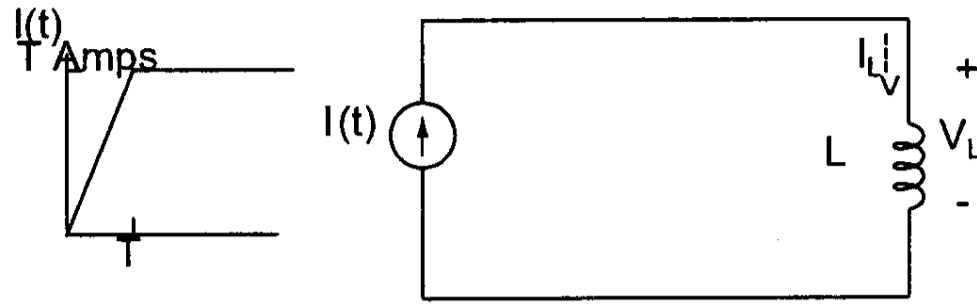
$$V_E = I_E R_L = \frac{I_C}{\beta} R_L = 3.17 \frac{41}{40} \times \frac{1}{2}$$

$$= 1.62 \text{ V}$$

$$V_E = \underline{1.62 \text{ V}}$$

Problem Number Six) (Transient RL problem)

For the following circuit



the current source is  $I(t) = t$  for  $0 \leq t \leq T$  and constant thereafter, as shown. Just before it is turned on ( $t = 0^-$ ) the current in the coil is zero.

a) 3/12 What are the current through and voltage across the coil for  $0^+ \leq t \leq T$ . Justify your result.

$$\begin{aligned}
 i_L(t) &= \frac{I}{L} = t \\
 v_L(t) &= L \frac{di_L}{dt} = L \cdot 1 = L
 \end{aligned}$$

KCL

b) 3/12 What are the current through and voltage across the coil for  $t \geq T$

$$\begin{aligned}
 i_L(t) &= T \\
 v_L(t) &= L \frac{di_L}{dt} = 0
 \end{aligned}$$

KCL

c) 3/12 A resistor, R, is added in parallel with the inductor. Give the current in the inductor and the voltage across the inductor for  $0^+ \leq t \leq T$ . (The following reference sheet gives the natural response and a complementary solution form for a first order D.E should you need them.)

$I_L = \frac{1}{\frac{1}{pL} + \frac{1}{R}} I(t)$   
voltage Divider

$= \frac{1}{1 + pLR} I(t)$

$\therefore \frac{dI_L}{dt} + \frac{R}{L} I_L = \frac{R}{L} I(t)$

$\frac{d}{dt}(I_L e^{R/L t}) = \frac{R}{L} I(t) e^{R/L t}$

Max 3

$I_L(t) e^{R/L t} - I_L(0^+) = \frac{R}{L} \int_0^t I(t') e^{R/L t'} dt'$

Integrate by parts  $\rightarrow \frac{1}{R} \frac{d}{dt} \left[ \frac{1}{R} e^{R/L t} \right]$  Solving D.E

$I_L(t) = \frac{R}{L} e^{-R/L t} \left[ \frac{1}{R} (t e^{R/L t}) - \frac{1}{R} \int e^{R/L t} dt \right]$

$i_L(t) = \frac{[t - L/R (1 - e^{-tR/L})]}{L}$

$v_L(t) = L \frac{di_L}{dt} = L [1 - e^{-tR/L}]$  ← Nat. Sol<sup>n</sup>

d) 3/12 For case a) and c) above, what are the inductor voltage and current after a long time?

$$i_L(t \rightarrow \infty) = \frac{T}{L} \text{ (2)}$$

$$v_L(t \rightarrow \infty) = 0 \text{ (1)}$$

## Useful Equations

### Complex Exponentials

$$\cos x = \frac{e^{jx} + e^{-jx}}{2} \quad \sin x = \frac{e^{jx} - e^{-jx}}{2j} \quad e^{jx} = \cos x + j \sin x$$

### First Order Circuits:

Differential Equation:  $\frac{df(t)}{dt} + af(t) = x(t)$

Natural Solution (i.e. solution when  $x(t) = 0$ ):  $f_n(t) = ke^{-at}$

Particular Solution: If  $x(t) = At$ , the particular solution has the form  $f_p(t) = A(-\frac{1}{\alpha^2} + \frac{t}{\alpha})$ .

### Second Order Circuits:

Differential Equation:  $\frac{d^2f(t)}{dt^2} + a\frac{df(t)}{dt} + bf(t) = x(t)$

Natural Solutions (i.e. solutions when  $x(t) = 0$ ):

$$f_n(t) = k_1e^{s_1t} + k_2e^{s_2t} \text{ (Overdamped)}$$

$$f_n(t) = k_1e^{s_1t} + k_2te^{s_1t} \text{ (Critically Damped)}$$

$$f_n(t) = e^{-\alpha t}(k_1 \cos(\omega_d t) + k_2 \sin(\omega_d t)) \text{ with } s_{1,2} = -\alpha \pm j\omega_d \text{ (Underdamped)}$$

### N-Channel MOSFET Transistors

Cutoff:  $i_d = 0$  for  $v_{GS} \leq V_{to}$

Triode:  $i_d = K[2(v_{GS} - V_{to})v_{DS} - v_{DS}^2]$  for  $v_{GS} \geq V_{to}$  and  $v_{DS} < v_{GS} - V_{to}$

Saturation:  $i_d = K(v_{GS} - V_{to})^2$  for  $v_{GS} \geq V_{to}$  and  $v_{DS} \geq v_{GS} - V_{to}$

### NPN Bipolar Junction Transistor

Active Region:  $i_C = \beta i_B$ ,  $i_C = \alpha i_E$ , and  $\beta = \frac{\alpha}{1-\alpha}$

UNIVERSITY OF CALIFORNIA  
College of Engineering  
Department of Electrical Engineering  
and Computer Sciences  
EECS 100/42  
Final Examination Fall 2009

T.K. Gustafson  
Dec 18 2009

**PRINT YOUR NAME:**

S.I.D. :

SIGNATURE:

Do your work on the exam.  
If you do need to use extra sheets  
attach these to the exam  
so that these are considered as well.

Make your methods clear so that partial credits is possible.

There are six problems  
THE PROBLEMS ARE EACH WORTH 12

Problem No	Score
One	
Two	
Three	
Four	
Five	
Six	
<b>TOTAL</b>	