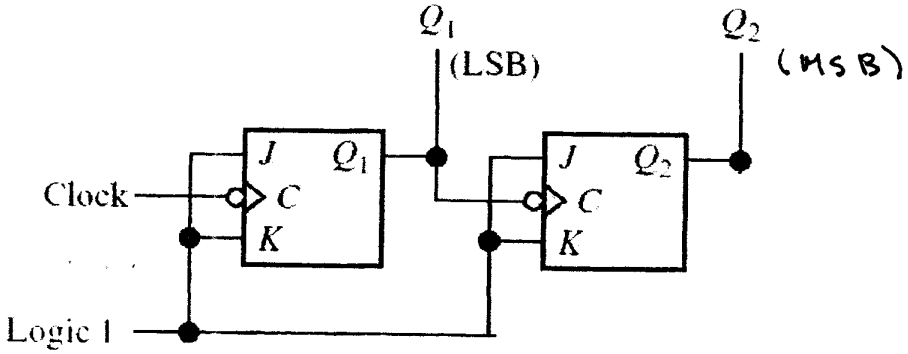
Problem Set 6
Solutions.

Problem No 1 Hambley 7.88

(a) There are four diodes and to make one revolution in two seconds each diode must be on for 0.5 s. Thus, the frequency of the clock is 2 Hz.

Since we need 4 states we need two Flip Flops (J K)

b) For the counting can just use a a ripple counter (page 383). The modulo 4 counter is



(c) The truth table

S	Q_2	Q_1	D_1	D_2	D_3	D_4
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1
1	0	0	1	0	0	0
1	0	1	0	0	0	1
1	1	0	0	0	1	0
1	1	1	0	1	0	0

The minimimal SOP expressions are:

$D_1 = \overline{Q_1}\overline{Q_2}$ $D_2 = Q_1\overline{Q_2}\,\overline{S} + Q_1Q_2S$ $D_3 = \overline{Q_1}Q_2$ $D_4 = Q_1Q_2\,\overline{S} + Q_1\overline{Q_2}S$

These are found fro Karnaugh maps.

Example D_1

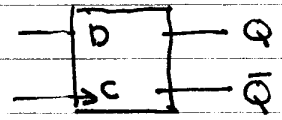
Q_2Q_1 / S	00	01	11	10
0	(1	0	0	0
1	1)	0	0	0

$D_1 = \overline{Q}_2\overline{Q}_1$

Hambley 7.81

Truth Table for D-Flip Flop (page

C	D	Q_n
↑	0	0
↑	1	1



From Logic Diagram

$D_0 = Q_2 \oplus D_2$

$D_2 = Q_1$

$D_1 = Q_0$

Also $Q_0 = D_0$, $Q_1 = D_1$, $Q_2 = D_2$ } on clock transition

Given

	Q_0	Q_1	Q_2	D_0	D_1	D_2
①	1	0	0	0	1	0
②	0	1	0	1	0	1
③	1	0	1	1	1	0
④	1	1	0	1	1	1
⑤	1	1	1	0	1	1
⑥	0	1	1	0	0	1
⑦	0	0	1	0	0	0
	0	0	0			

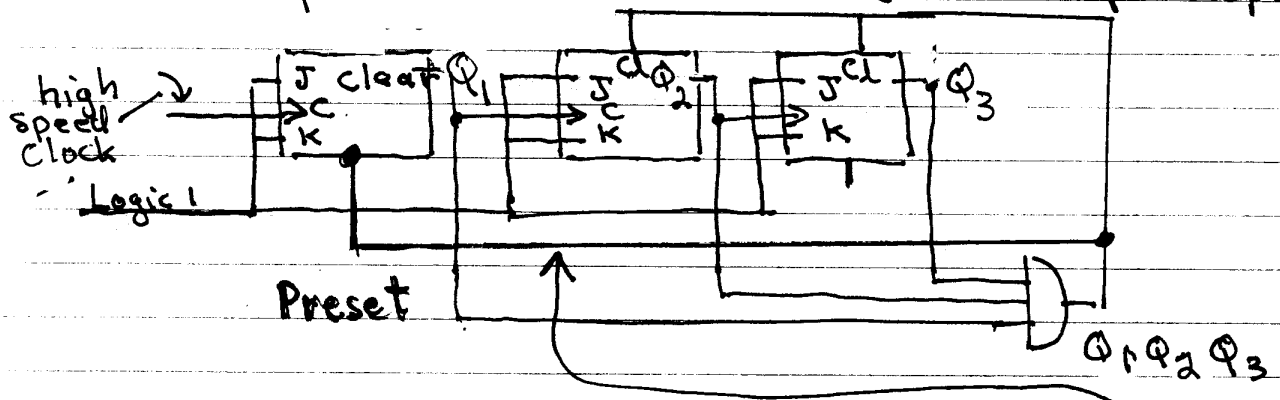
so register is empty after 7 clock cycles.

Problem No. 2 The counter using preset and clear

7.57

a) Use the ripple counter of Fig 7.53 with slight modification. We want it to clear when 111 is obtained (6) and want to set it to 000.

This can be done by using an adder to combine $Q_0 Q_1 Q_2$ and send it to the clear input of the three J-K flip-flops.

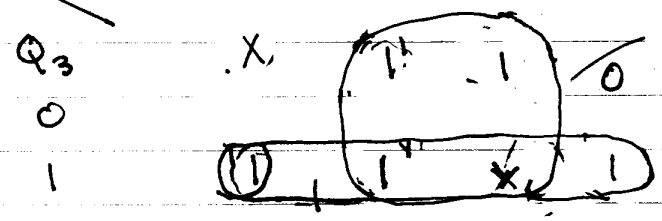


(b) The truth table for the encoder is:

	Q_3	Q_2	Q_1	D_1	D_2	D_3	D_4	D_5	D_6	D_7
"can't occur" → 0	~~0~~	~~0~~	~~0~~	x	x	x	x	x	x	x
1	0	0	1	0	0	0	1	0	0	0
2	0	1	0	1	0	0	0	0	0	1
3	0	1	1	1	0	0	1	0	0	1
4	1	0	0	1	1	0	0	0	1	1
5	1	0	1	1	1	0	1	0	1	1
6	1	1	0	1	1	1	0	1	1	1
7	1	1	1	X	X	X	X	X	X	X

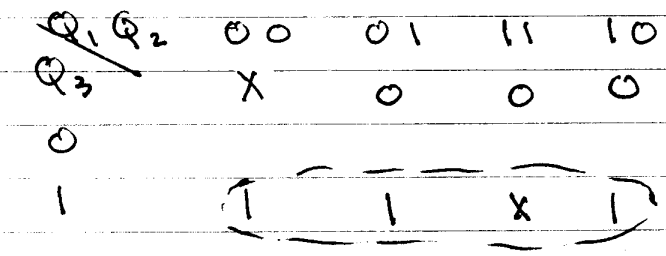
→ Haubley's Answer. However I really want these to be "can't occur"

Karnaugh Map for D_1



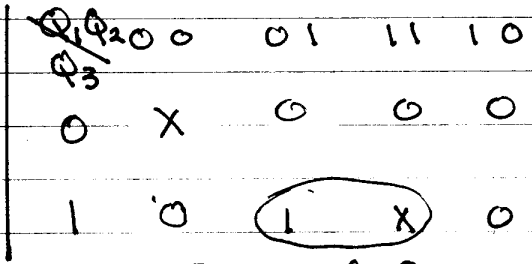
$D_1 = Q_3 + Q_2$

Karnaugh Map for D_2



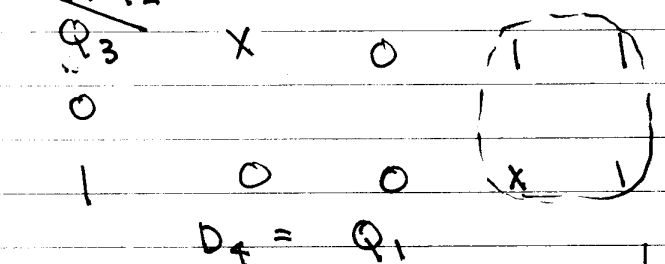
$D_2 = Q_3$

Map for D_3



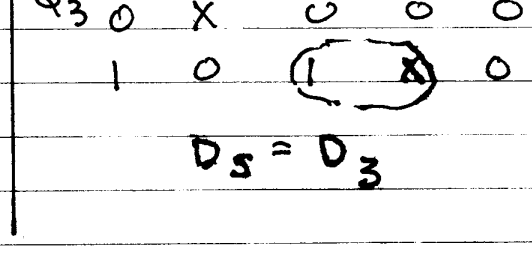
$D_3 = Q_2 Q_3$

Map for D_4



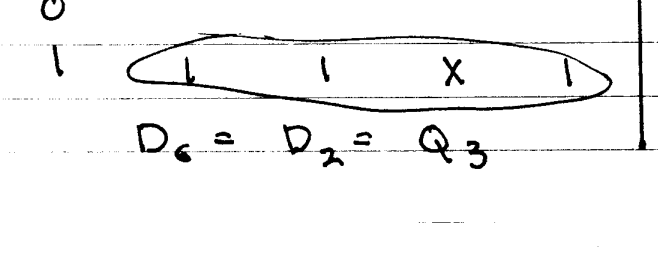
$D_4 = Q_1$

Map for D_5



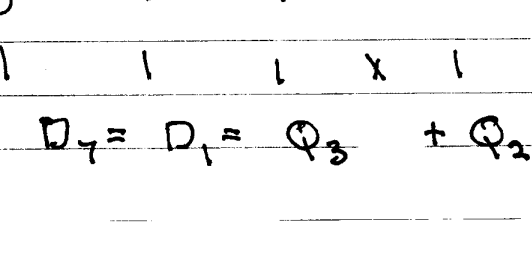
$D_5 = D_3$

Map for D_6



$D_6 = D_2 = Q_3$

Map for D_7



$D_7 = D_1 = Q_3 + Q_2$

Problem No. 3,

a) $i_{ds} = k (v_{gs} - V_T)^2$

$v_{gs} = V_{gs} + \Delta v_{gs}$; $i_{ds} = I_{ds} + \Delta i_{ds}$

(1) $I_{ds} + \Delta i_{ds} = k (V_{GS} + \Delta v_{gs} - V_T)^2$

$\simeq k ((V_{GS} - V_T)^2 + 2 \Delta v_{gs} (V_{GS} - V_T) + (\Delta v_{gs})^2)$

neglect (small)

Now $I_{ds} = k (V_{GS} - V_T)^2$ ——— (2)

This gives d.c. operating point

For d.c. capacitor is open

so $V_{GS} = 3$ V as previous.

so $I_{ds} = .5 (3-1)^2 = .5 \times 4 = 2$ mA

Use (2) in (1) to eliminate I_{ds}. Then

$\Delta i_{ds} = 2k (V_{GS} - V_T) \Delta v_{gs}$

$= 1 (2) \Delta v_{gs}$ mA

Now. $v_{ds} = 20 - i_{ds} \times 2k\Omega$

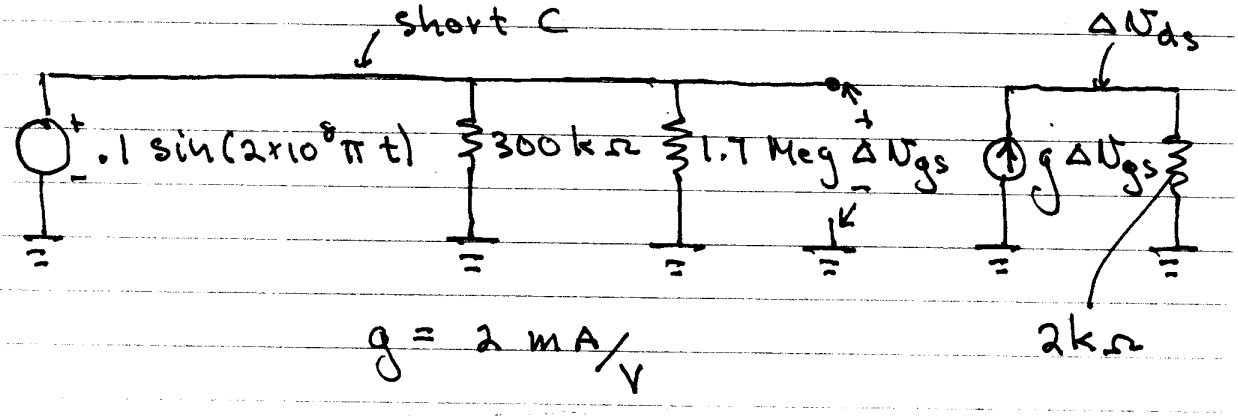
$V_{ds} + \Delta v_{ds} = 20 - (I_{ds} + \Delta i_{ds}) 2k\Omega$

but $V_{ds} = 20 - I_{ds} \times 2k\Omega$ (d.c. analysis)

Thus $\Delta v_{ds} = - \Delta i_{ds} \times 2k\Omega$

$\boxed{\Delta v_{ds} = - 4 \Delta v_{gs}}$

c) Small-signal equivalent!



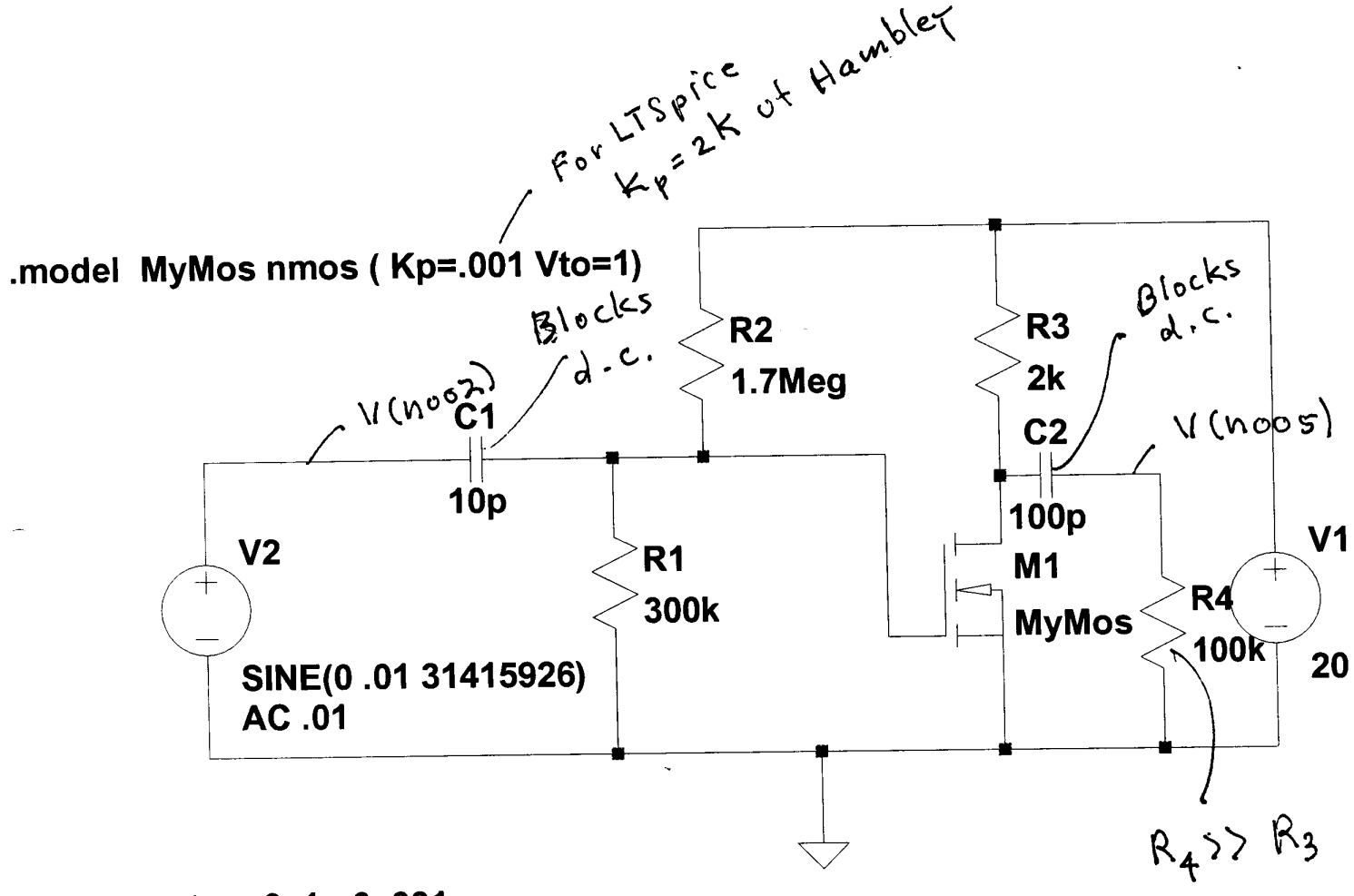
$g = 2\ mA/V$

d) The input resistance is

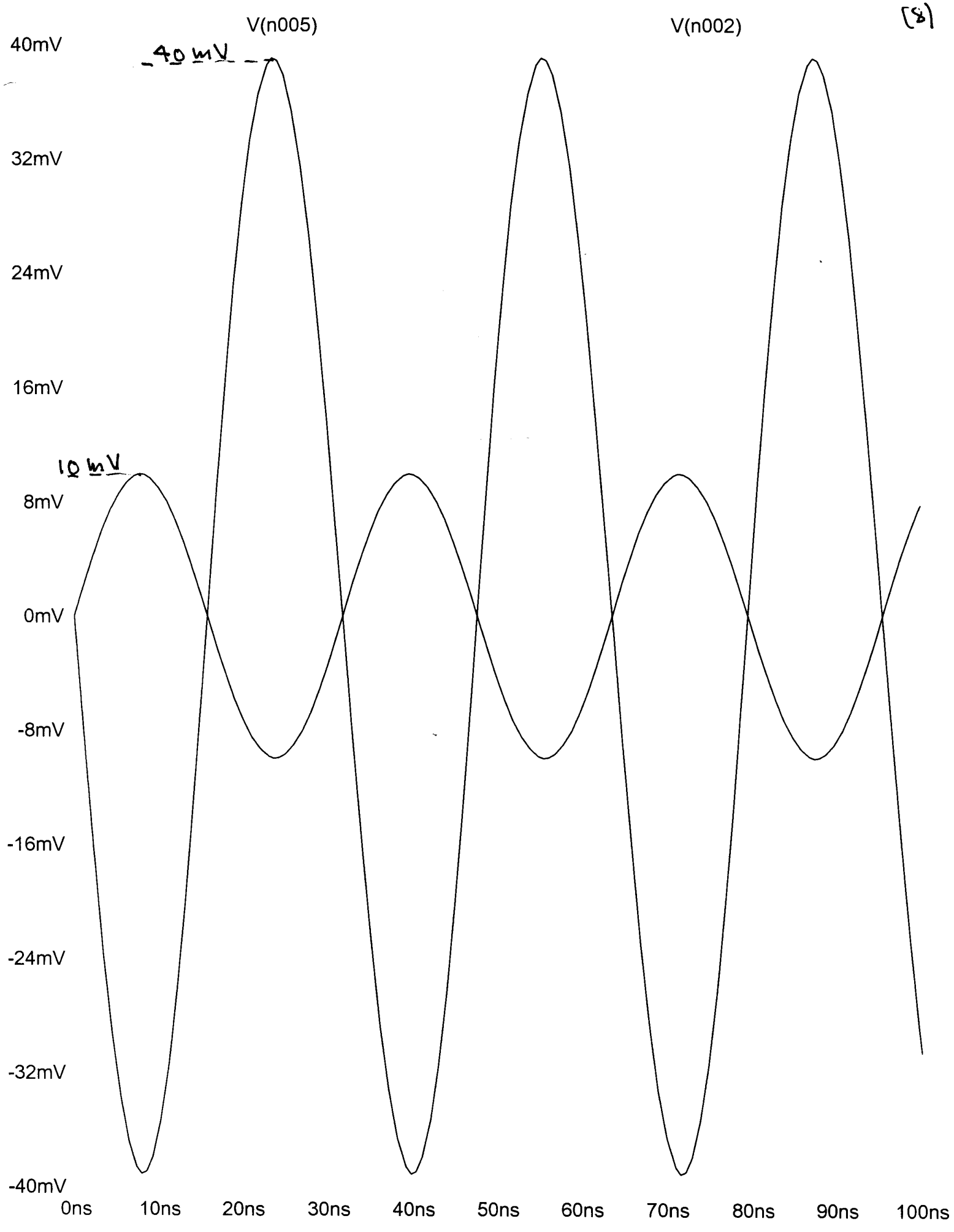
$R_i = (300k\Omega \,||\, 1.7\ Meg\Omega)$

$R_o = \infty$

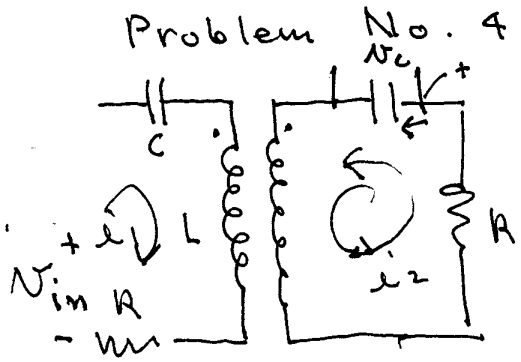
$R_L = 2k\Omega$ (generally not included in output R calculation)



.tran 0 .1u 0 .001u


V(n005)
V(n002)
40mV
32mV
24mV
16mV
8mV
0mV
-8mV
-16mV
-24mV
-32mV
-40mV
0ns
10ns
20ns
30ns
40ns
50ns
60ns
70ns
80ns
90ns
100ns
40 mV
10 mV

Problem No. 4



$$0 = L\frac{di_2}{dt} + M\frac{di_1}{dt} + \frac{1}{C}\int i_2\,dt = 0$$

$$v_{in} = L\frac{di_1}{dt} + M\frac{di_2}{dt} + \frac{1}{C}\int i_1\,dt$$

"phasors" $v_{in} = Re(V_1 e^{j\omega t})$, $i_1(t) = Re(I_1 e^{j\omega t})$

$v_c(t) = Re(V_c e^{j\omega t})$ $i_2(t) = Re(I_2 e^{j\omega t})$

$$0 = \left(Lj\omega + R + \frac{1}{j\omega C}\right) I_2 + j\omega M I_1 \quad --- (1)$$

$$V_1 = \left(j\omega L + R + \frac{1}{j\omega C}\right) I_1 + j\omega M I_2 + R I_1 \quad --(2)$$

$$0 = \left(j\omega L + \frac{1}{j\omega C} + R\right) I_2 + \frac{j\omega M(-j\omega M) I_2}{\left(j\omega L + \frac{1}{j\omega C} + R\right)}$$

$$+ \frac{j\omega M}{j\omega L + \frac{1}{j\omega C} + R} V_1$$

Multiply through by $(j\omega L + 1/j\omega C + R)$

$$-\left[\left(j\omega L + \frac{1}{j\omega C} + R\right)^2 + \omega^2 M^2\right] I_2 = -j\omega M V_1$$

Factoring!

$$\left[\left(j\omega L + \frac{1}{j\omega C} + R\right) - j\omega M\right]\left[\left(j\omega L + \frac{1}{j\omega C} + R\right) + j\omega M\right] I_2 = -j\omega M V_1$$

Thus

$$I_2 = \frac{-j\omega M V_1}{\left[\left(j\omega L + \frac{1}{j\omega C} + R\right) - j\omega M\right]\left[\left(j\omega L + \frac{1}{j\omega C} + R\right) + j\omega M\right]}$$

and

$$V_c = \frac{1}{j\omega C} I_2$$

we observe

a) if $M = 0$ there is a peak in $|V_c|$ near $\omega = \frac{1}{\sqrt{LC}}$; (R is small)

b) $j\omega L + \frac{1}{j\omega C} + R \pm j\omega M$

$$= \left[\left(\omega L - \frac{1}{\omega C} \pm \omega M\right)^2 + R^2\right]^{1/2} e^{j\tan^{-1}\left\{\frac{\left[\omega(L \pm M) - \frac{1}{\omega C}\right]}{R}\right\}}$$

So the magnitude of the denomenator is minimized for $\omega \simeq \frac{1}{\sqrt{C(L \pm M)}}$

Thus there are two peaks separated by $\frac{1}{\sqrt{C}}\left(\frac{-1}{\sqrt{L+M}} + \frac{1}{\sqrt{L-M}}\right) \simeq \frac{1}{\sqrt{LC}} \frac{M}{L}$ for M small

c) The width of the resonances is given by $\omega L - \frac{1}{\omega C} = R$ (neglecting a small M)

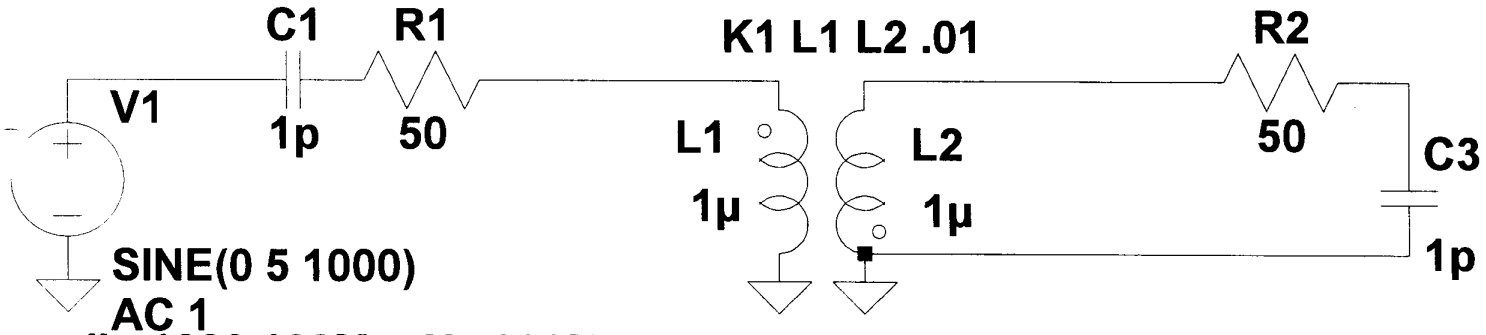
Let $\omega = \omega_0 + \Delta\omega$; $\omega_0 = \frac{1}{\sqrt{LC}}$

Thus $\omega_0 L + \Delta\omega L - \frac{1}{\omega_0 C} + \frac{\Delta\omega}{\omega_0}\frac{1}{\omega_0 C} = R$ ($\simeq \Delta\omega L$)

using $\frac{1}{\omega_0 + \Delta\omega} \simeq \frac{1}{\omega_0}\left(1 - \frac{\Delta\omega}{\omega_0}\right)$

Thus $\Delta\omega \simeq \frac{R}{L}$; This proportional to R

Thus unless M is large enough the separation between the peaks wont be observable (or decrase R)



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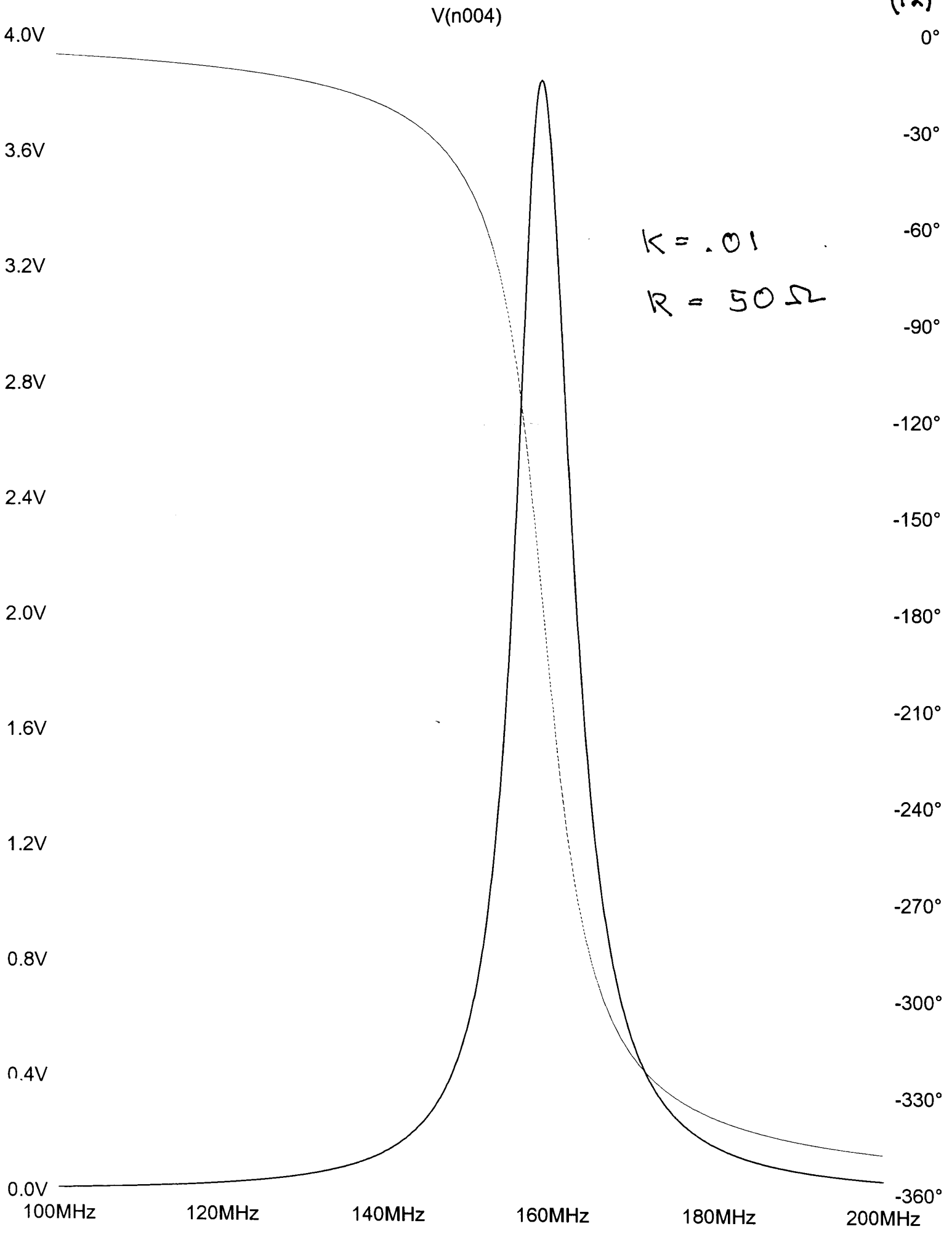
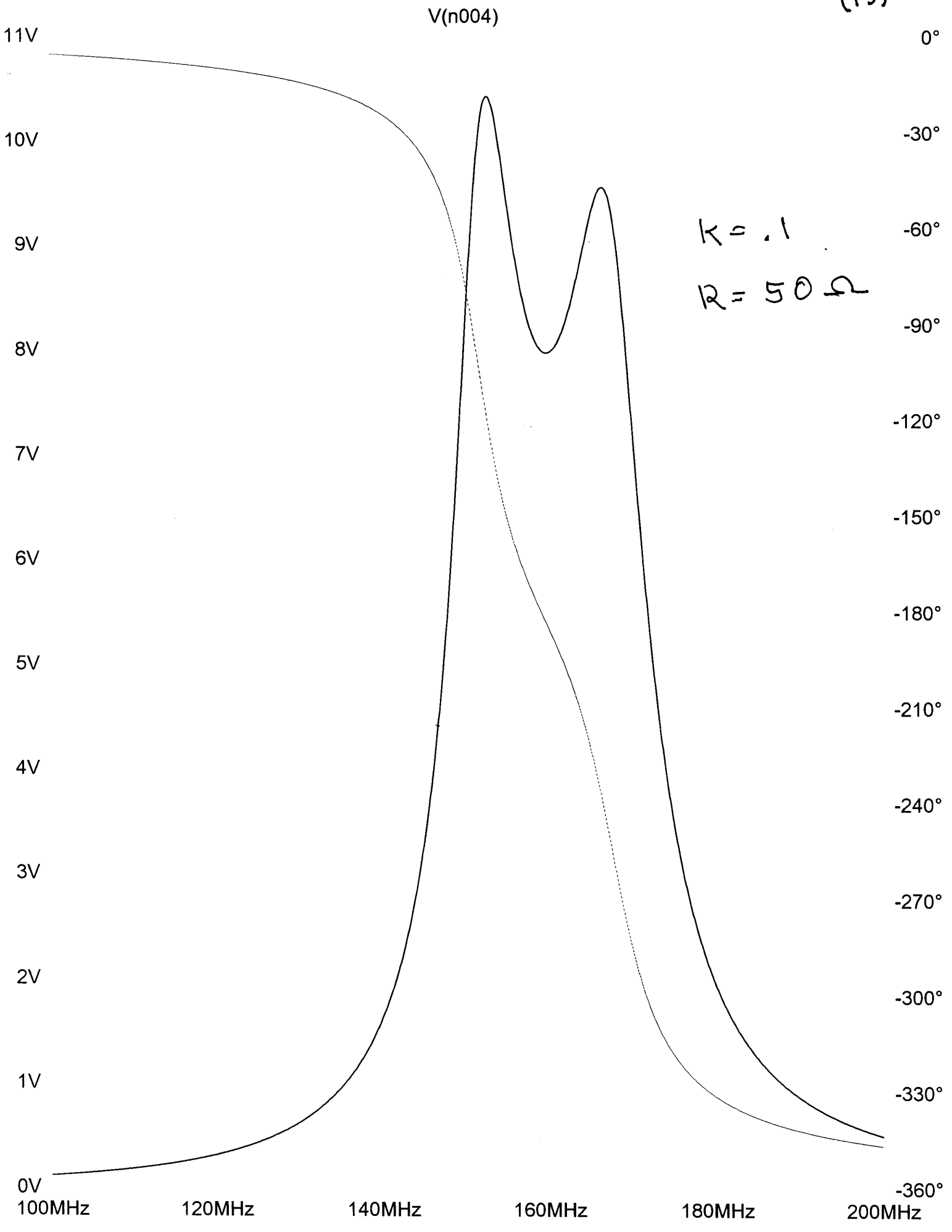
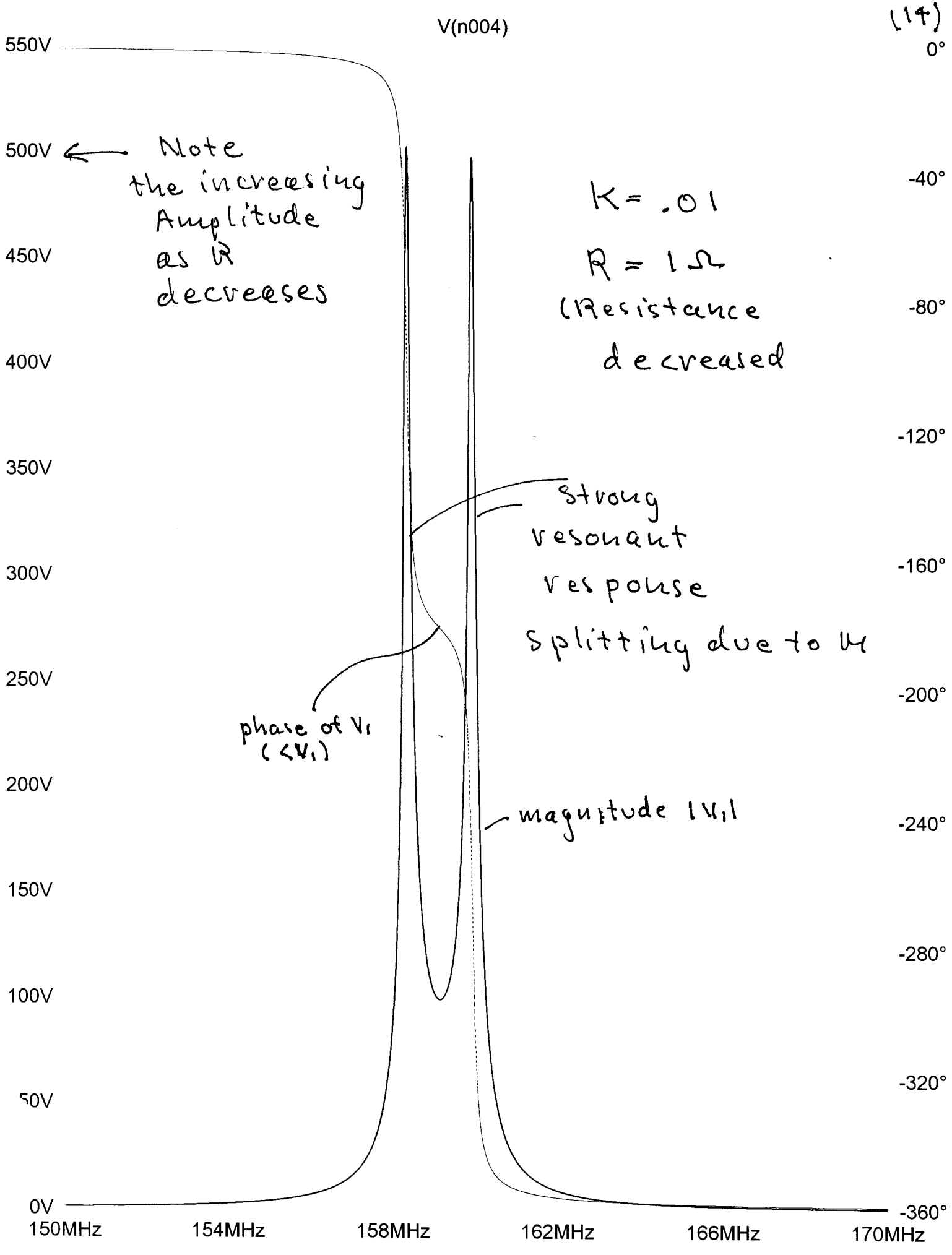
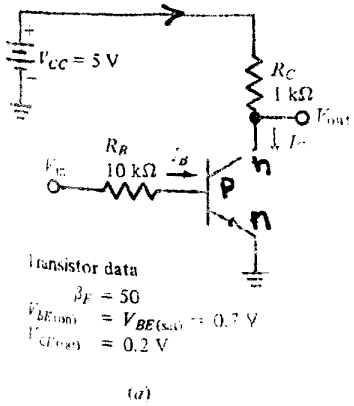

V(n004)
4.0V
3.6V
3.2V
2.8V
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0.0V
0°
-30°
-60°
-90°
-120°
-150°
-180°
-210°
-240°
-270°
-300°
-330°
-360°
100MHz
120MHz
140MHz
160MHz
180MHz
200MHz
K = .01
R = 50Ω

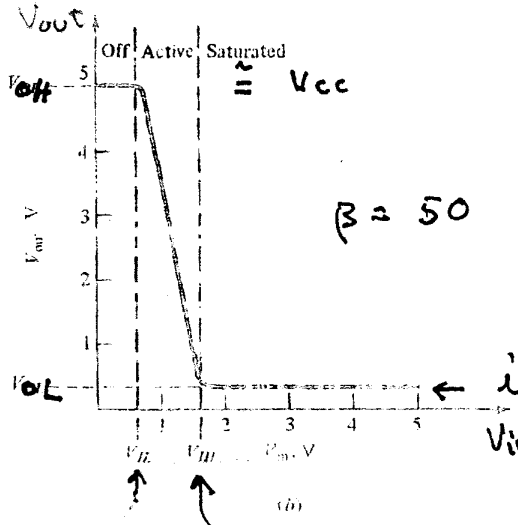

V(n004)
11V
10V
9V
8V
7V
6V
5V
4V
3V
2V
1V
0V
0°
-30°
-60°
-90°
-120°
-150°
-180°
-210°
-240°
-270°
-300°
-330°
-360°
100MHz
120MHz
140MHz
160MHz
180MHz
200MHz
K = .1
R = 50Ω


V(n004)
550V
500V
450V
400V
350V
300V
250V
200V
150V
100V
50V
0V
0°
-40°
-80°
-120°
-160°
-200°
-240°
-280°
-320°
-360°
150MHz
154MHz
158MHz
162MHz
166MHz
170MHz
Note the increasing Amplitude as R decreases
K = .01
R = 1Ω
(Resistance decreased
Strong resonant response
Splitting due to M
phase of V1 (<V1)
magnitude |V1|

Problem No. 5

Transistor Inverter - Digital Application





$\beta = 50$

$i_C \cong 5/10^3 = 5$ mA

$i_C \cong 5$mA $= i_B \beta$

$\therefore i_B \cong \frac{5\text{mA}}{50} = 100\,\mu\text{A}$

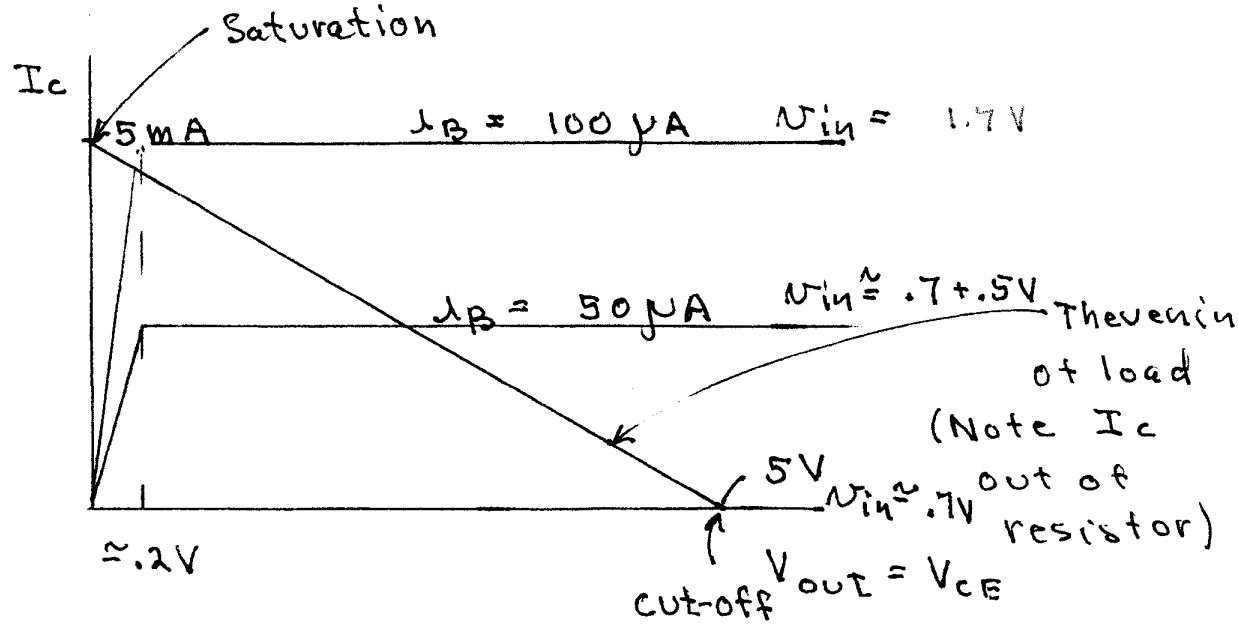
$V_{in} \cong .7 + 10\text{k}\Omega \times 100 \times 10^{-6}$

$\cong .7 + 1 \cong 1.7$ V

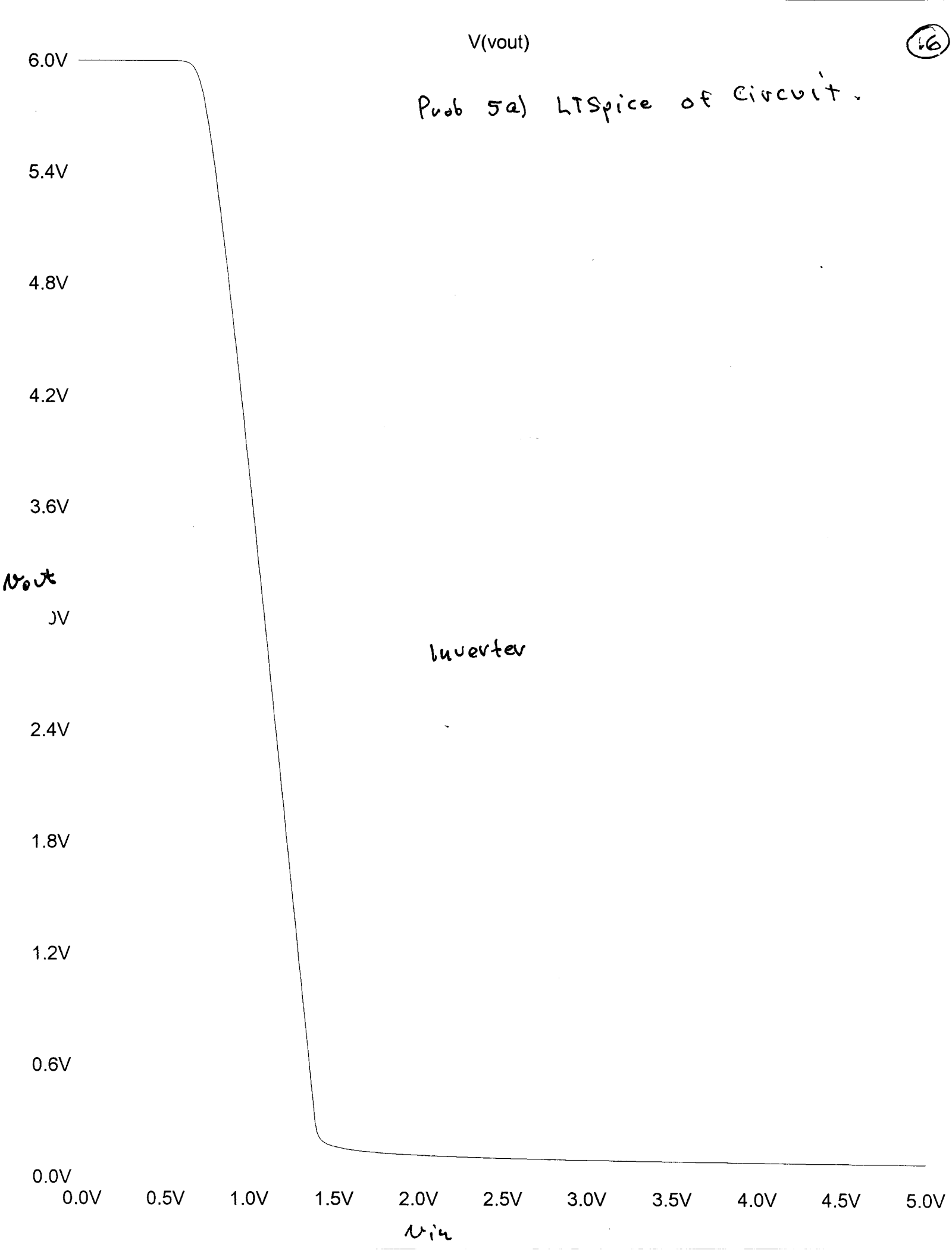
$i_C \cong i_B = 0$

base just barely on

$\therefore V_{in} \cong .7$V

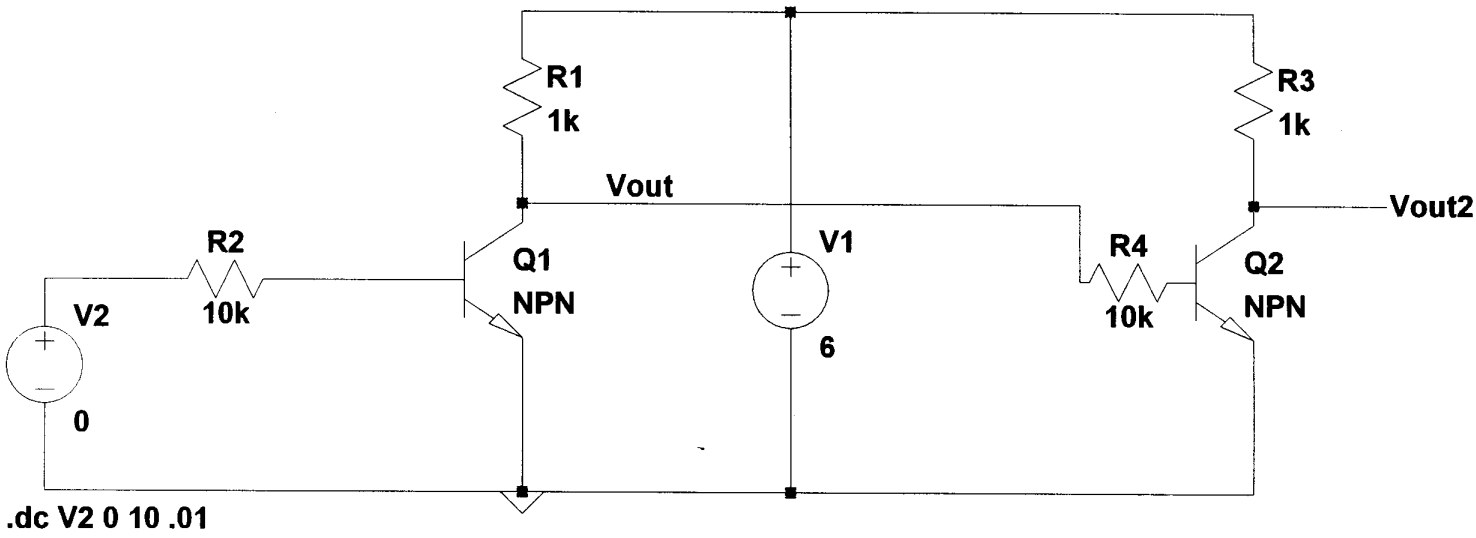


Prob 5a) LTSpice of Circuit.



Inverter

(5b)



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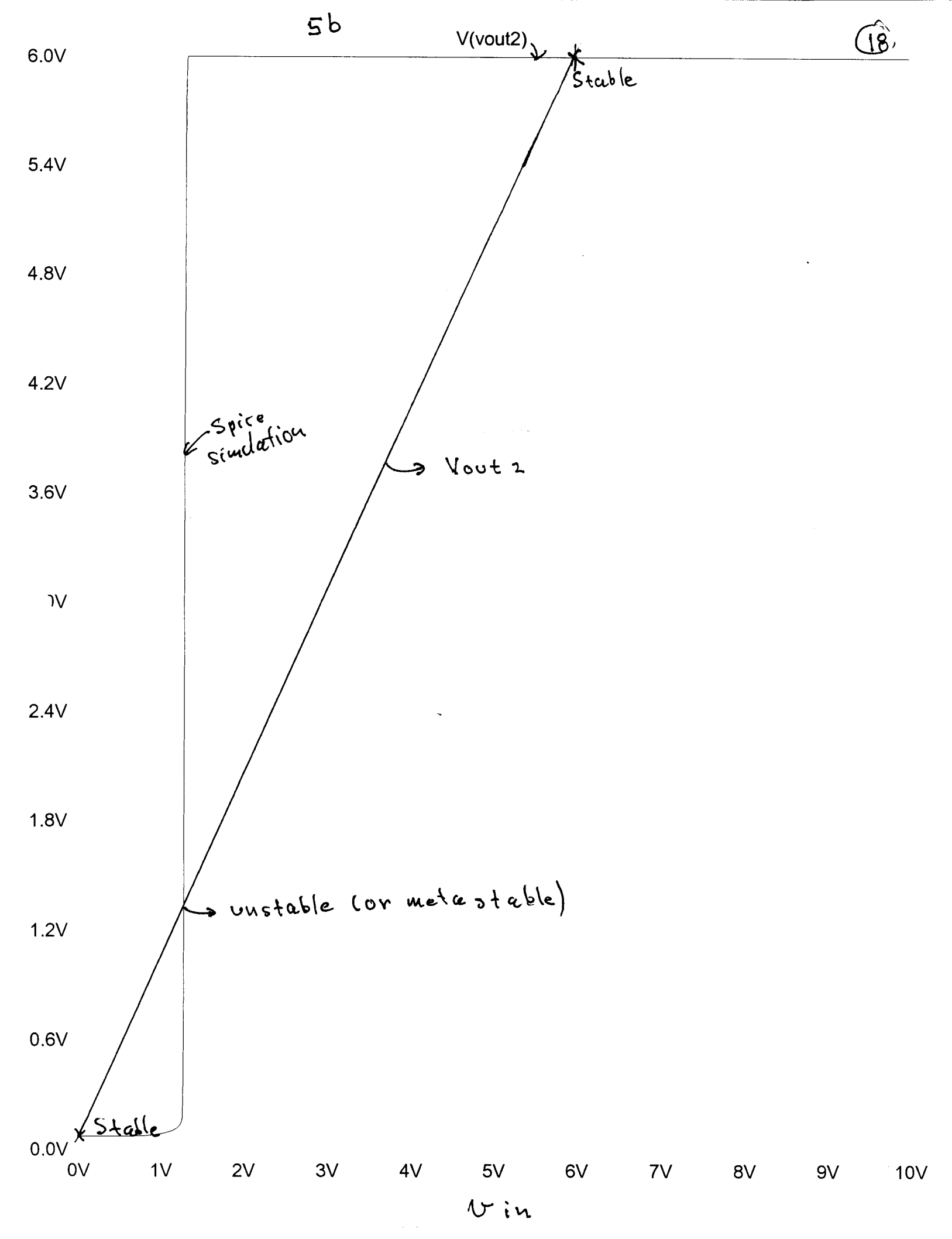
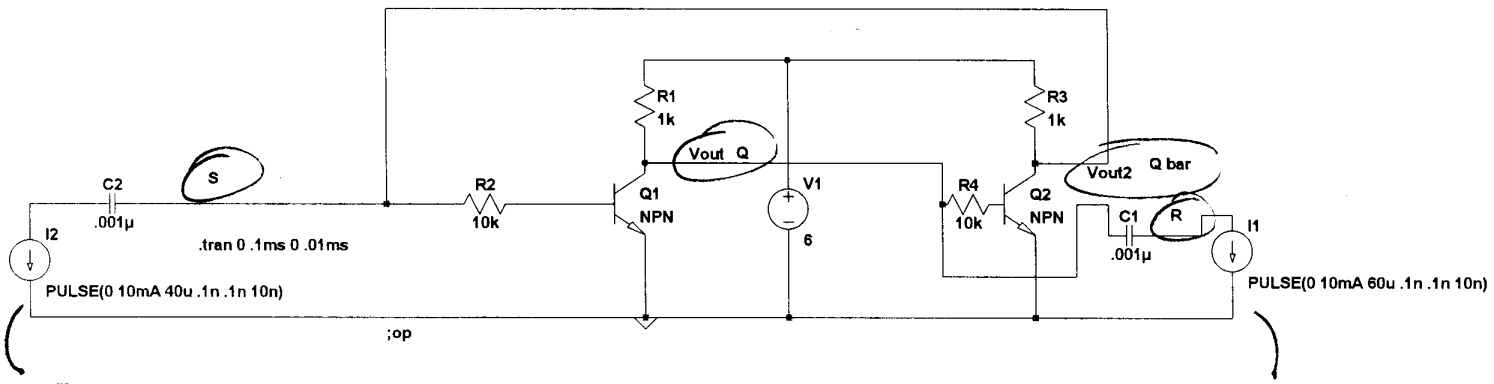
5b


V(vout2)
Stable
6.0V
5.4V
4.8V
4.2V
Spice simulation
Vout 2
3.6V
)V
2.4V
1.8V
unstable (or metastable)
1.2V
0.6V
Stable
0.0V
0V
1V
2V
3V
4V
5V
6V
7V
8V
9V
10V
v in

5c

R-S Flip Flop



Trigger

Trigger

Note pulses delayed by 20 µsec

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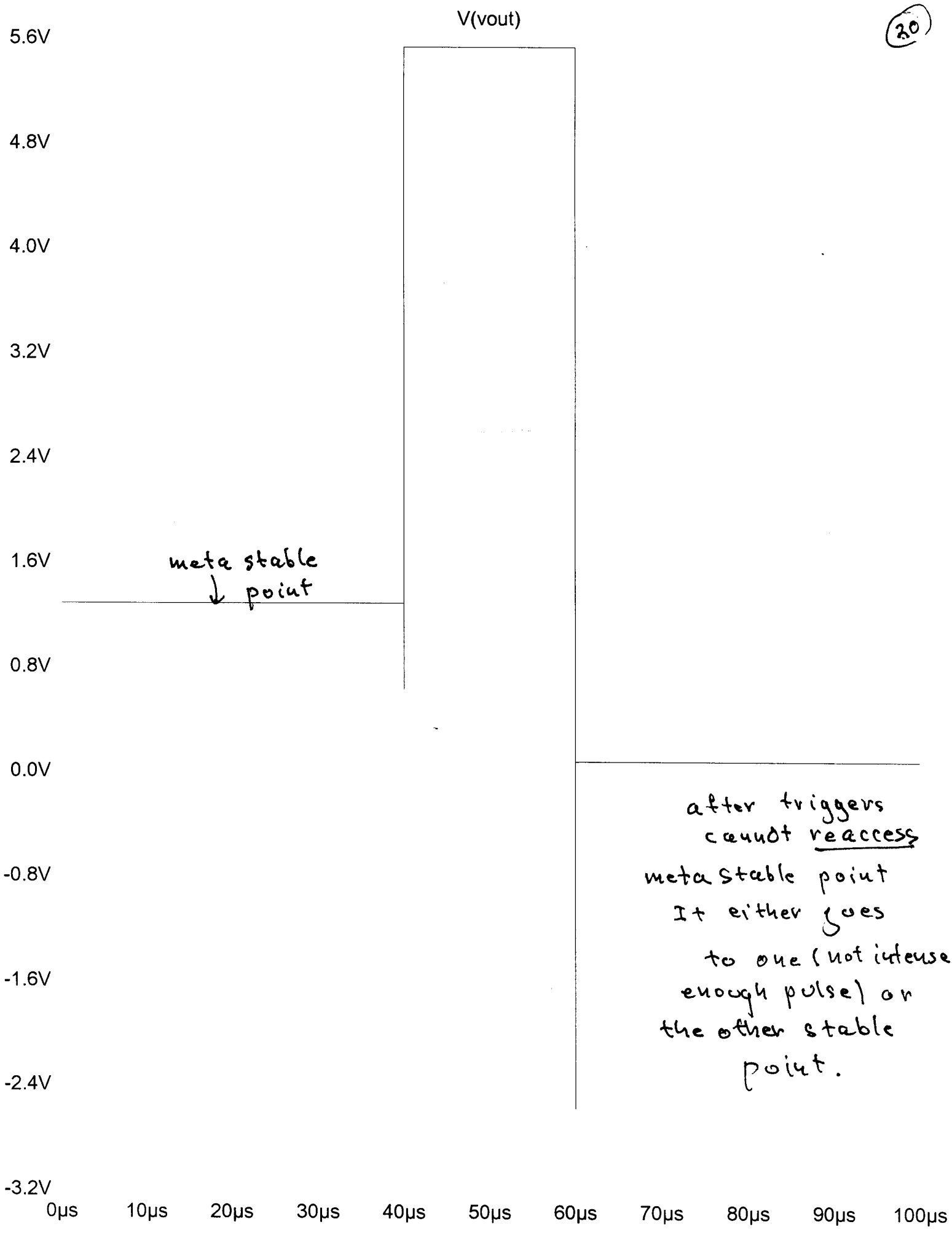
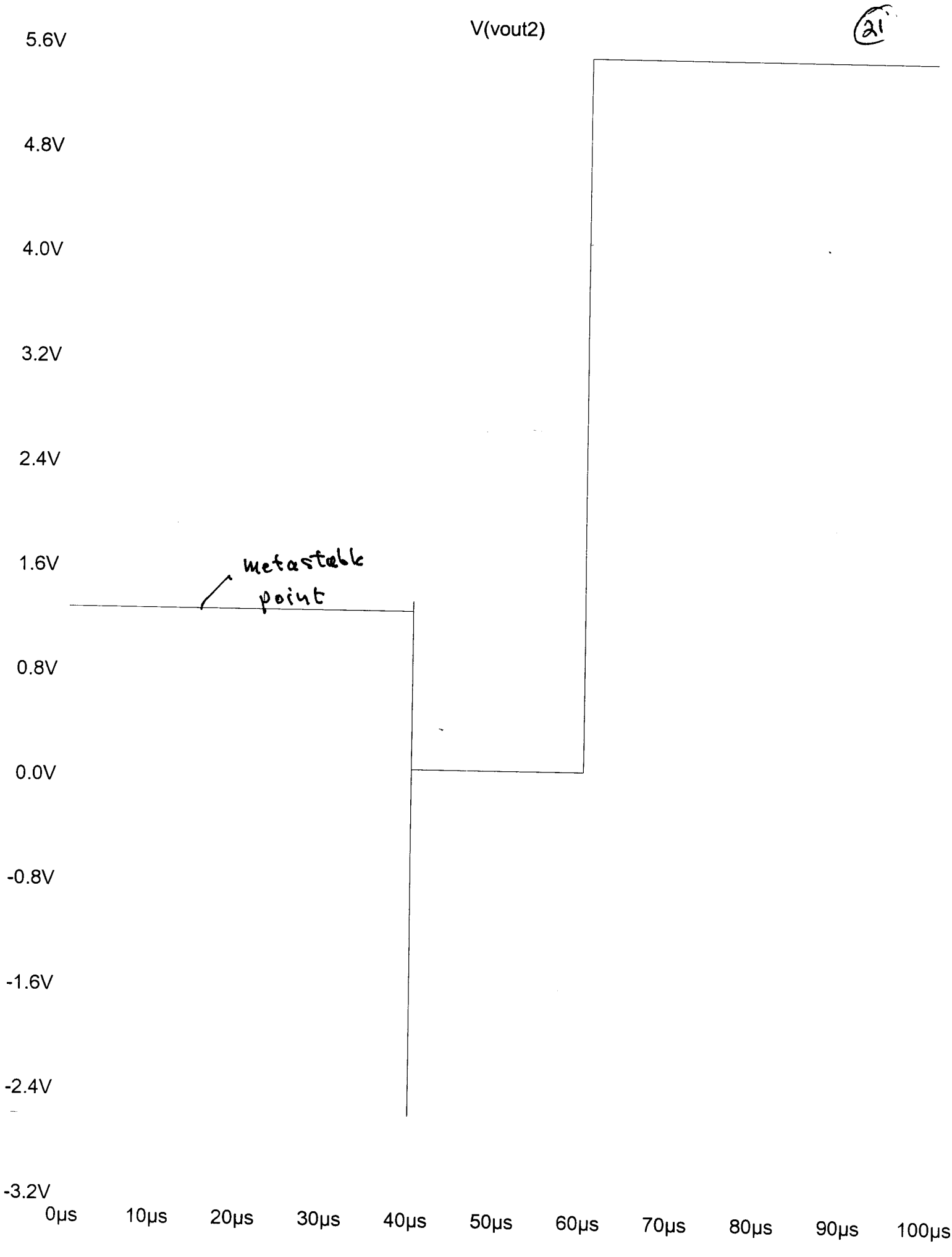
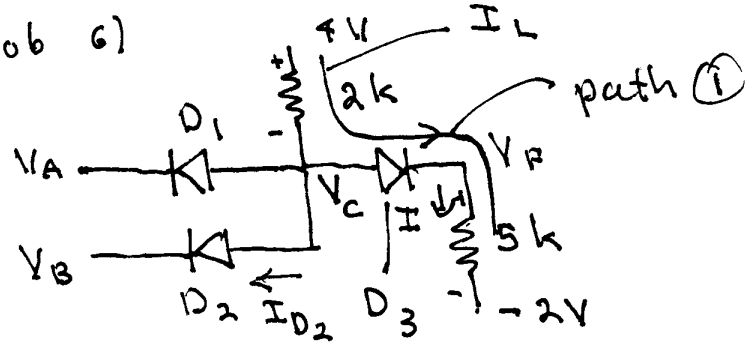

V(vout)
5.6V
4.8V
4.0V
3.2V
2.4V
1.6V
0.8V
0.0V
-0.8V
-1.6V
-2.4V
-3.2V
0µs
10µs
20µs
30µs
40µs
50µs
60µs
70µs
80µs
90µs
100µs
meta stable
point
after triggers
cannot reaccess
meta stable point
It either goes
to one (not intense
enough pulse) or
the other stable
point.


V(vout2)
5.6V
4.8V
4.0V
3.2V
2.4V
1.6V
0.8V
0.0V
-0.8V
-1.6V
-2.4V
-3.2V
metastable point
0µs
10µs
20µs
30µs
40µs
50µs
60µs
70µs
80µs
90µs
100µs

Prob 6)



$V_A = 5$ V. Thus D_1 is always reverse biased

$V_B = 4$ V D_2 = open since V_C would have to be 4.7 volts to foward bias it

Thus from KVL path ①

$$-4 + (2k)I + .7 + (5k)I - 2 = 0$$

(I in mA) $\therefore I = \frac{5.3}{7} = .757$ mA

Thus $V_F = -2 + 5(.757) = -2 + 3.785$

$= 1.785$ V.

As V_B is decreased, what is the voltage at which D_2 turns on? Ans: It is when $v_{D_2} = .7$ V and its current is zero!

$V_C = V_F + .7$; $V_B = V_C - .7 = V_F = 1.785$V

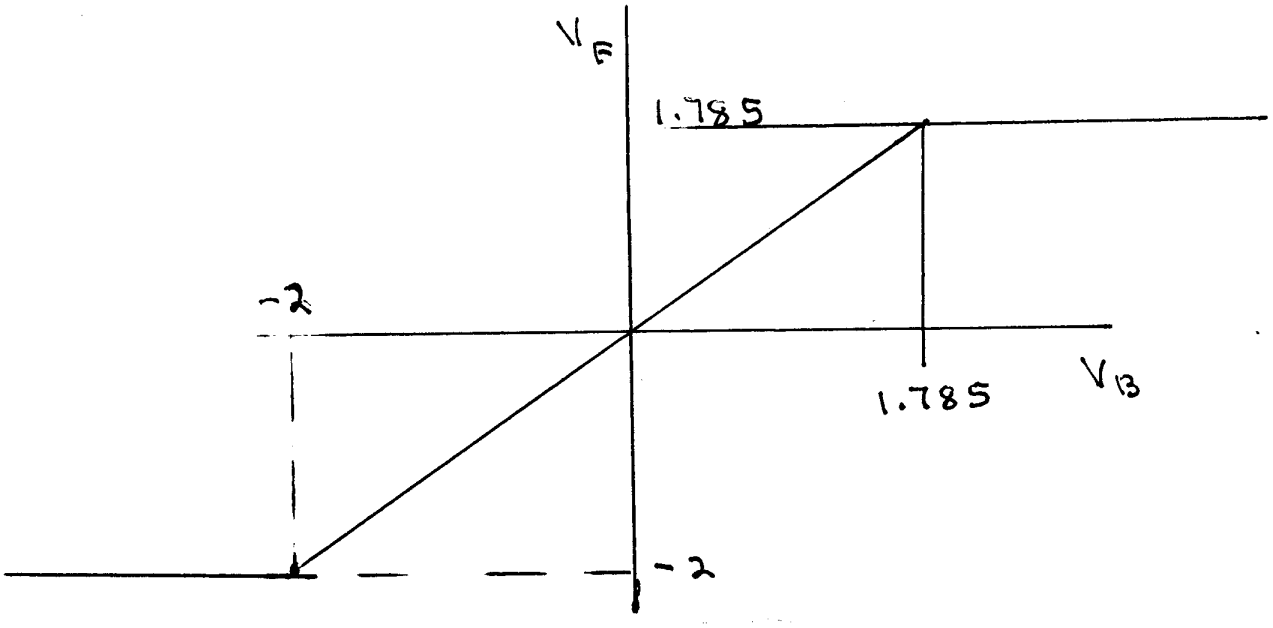
For $V_B < 1.785$ D_2 conducts. $V_C = V_B + .7$ and $V_F = V_B$

Finally, when does D_3 turn off. Ans $v_{D_3} = .7$V but $i_{D_3} = 0$. Then $I_L = I_{D_2}$ $(V_C + 2 - .7) + I5k = 0$

(V_C volts w.r.t. ground)

Thus $I = 0$ when $V_C = -2 + .7$, $V_B = V_C - .7 = -2$V

Then the out put voltage $= -2$V



Type of Gate

Truth Table (positive logic [high V → 1, low V → 0])

V_A	V_B	V_F	(V_A, V_B, V_F all > 0)
high	high	high	→ D_1 & D_2 off D_3 on
high	low	low	→ D_1 off D_2, D_3 on
low	high	low	→ D_2 off D_1, D_3 on
Low	low	low	→ D_1, D_2 on D_3 on

It is thus an and gate

Note that for negative logic (the reverse of the above, it is an OR Gate