Section 4.2: DC Steady State

P4.18. List the steps for dc steady-state analysis of *RLC* circuits.

P4.19. Explain why we replace capacitances with open circuits and inductances with short circuits in dc steady-state analysis.

***P4.20.** Solve for the steady-state values of i_1, i_2, and i_3 for the circuit shown in Figure P4.20.

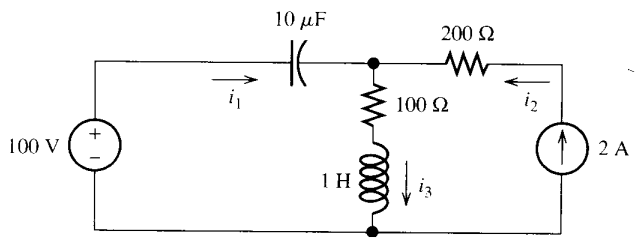


Figure P4.20

***P4.21.** Consider the circuit shown in Figure P4.21. What is the steady-state value of v_C after the switch opens? Determine how long it takes after the switch opens before v_C is within 1 percent of its steady-state value.

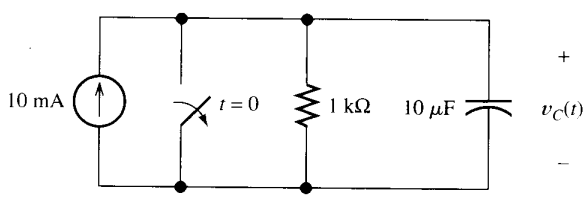


Figure P4.21

P4.22. Solve for the steady-state values of i_1, i_2, i_3, i_4, and v_C for the circuit shown in Figure P4.22, assuming that the switch has been closed for a long time.

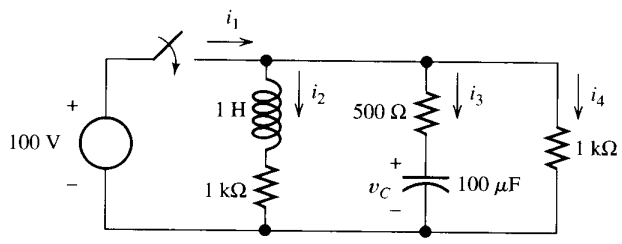


Figure P4.22

P4.23. The circuit shown in Figure P4.23 is operat in steady state. Determine the values of i_L, and v_C.

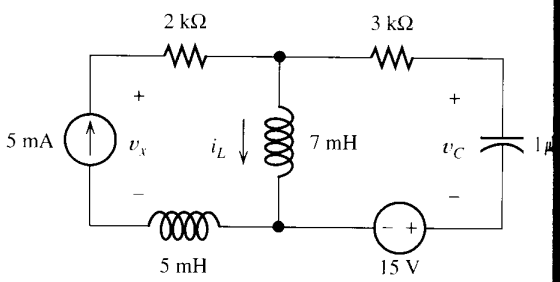


Figure P4.23

P4.24. The circuit shown in Figure P4.24 has been up for a long time prior to $t = 0$ with the sw closed. Find the value of v_C prior to $t = 0$. F the steady-state value of v_C after the switch been opened for a long time.

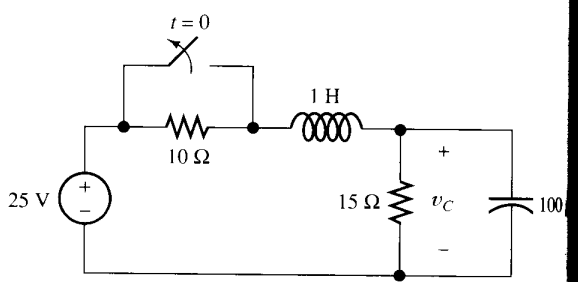


Figure P4.24

P4.25. Consider the circuit of Figure P4.25 in wh the switch has been closed for a long t prior to $t = 0$. Determine the values of v before $t = 0$ and a long time after $t = 0$. A determine the time constant after the sw opens and expressions for $v_C(t)$. Sketch v to scale versus time for $-0.2 \leq t \leq 1.0$ s.

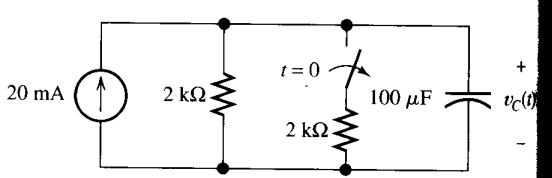


Figure P4.25

18. Draw the load lines on the i_D–v_{DS} axes for the circuit of Figure 12.10 on page 583 for

a. $R_D = 1\ \text{k}\Omega$ and $V_{DD} = 5\ \text{V}$

b. $R_D = 1\ \text{k}\Omega$ and $V_{DD} = 10\ \text{V}$

c. $R_D = 1\ \text{k}\Omega$ and $V_{DD} = 15\ \text{V}$

How does the position of the load line change as V_{DD} increases in value?

19. Consider the circuit shown in Figure 12.10 on page 583. The transistor characteristics are shown in Figure 12.11. Suppose that V_{GG} is changed to 0 V. Determine the values of V_{DSQ}, $V_{DS\text{min}}$, and $V_{DS\text{max}}$. Find the gain of the amplifier.

20. Consider the amplifier shown in Figure P12.20.

a. Find $v_{GS}(t)$, assuming that the coupling capacitor is a short circuit for the ac signal and an open circuit for dc. (*Hint:* Apply the superposition principle for the ac and dc sources.)

b. If the FET has $V_{to} = 1$ V and $K = 0.5\ \text{mA/V}^2$, sketch its drain characteristics to scale for $v_{GS} = 1, 2, 3$, and 4 V.

c. Draw the load line for the amplifier on the characteristics.

d. Find the values of V_{DSQ}, $V_{DS\text{min}}$, and $V_{DS\text{max}}$.

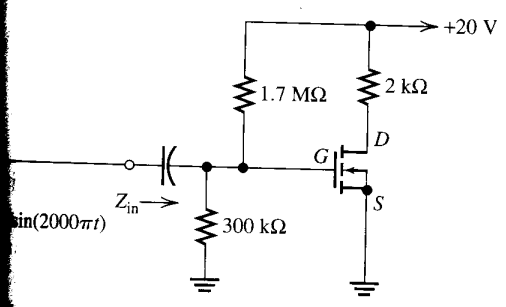


Figure P12.20

P12.22. Use a load-line analysis of the circuit shown in Figure P12.22 to determine the values of V_{DSQ}, $V_{DS\text{min}}$, and $V_{DS\text{max}}$. The characteristics of the FET are shown in Figure 12.21 on page 593. (*Hint*: First, replace the 15-V source and the resistances by their Thévenin equivalent circuit.)

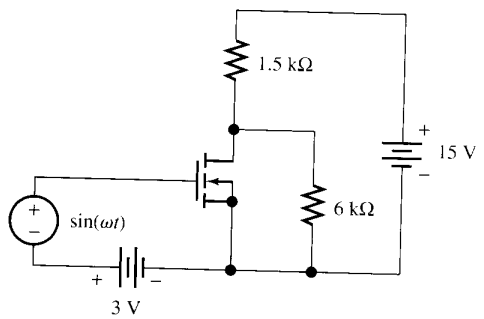
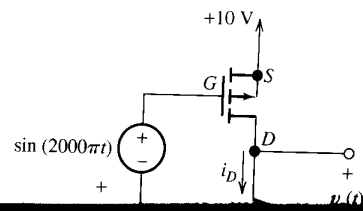


Figure P12.22

P12.23. Suppose that the resistance R_D in Figure 12.10 (page 583) is replaced with an unusual two-terminal nonlinear device for which $v = 0.1i_D^2$, where i_D is the current through the device in mA and v is the voltage across the device in volts (referenced positive at the end connected to V_{DD}). Carefully sketch the load line on Figure 12.11 (page 584). What shape is this load line?

P12.24. Use a load-line analysis for the PMOS amplifier shown in Figure P12.24 to determine the maximum, minimum, and Q-point values of $v_o(t)$. The characteristics of the transistor are shown in Figure 12.9 on page 582.



13.3: Load-Line Analysis of a Common-Emitter Amplifier

List several reasons that distortion occurs in BJT amplifiers.

Consider the circuit of Figure 13.7 on page 623. Given $V_{CC} = 10$ V and $R_C = 2$ kΩ, construct the load line on the i_C versus v_{CE} axes. Repeat for $V_{CC} = 15$ V. How does the slope of the load line change when V_{CC} changes?

Consider the circuit of Figure 13.7 on page 623. Assume that $V_{CC} = 20$ V, $V_{BB} = 0.8$ V, $R_B = 40$ kΩ, and $R_C = 2$ kΩ. The input signal is a 0.2-V-peak 1-kHz sinusoid given by $v_{in}(t) = 0.2\sin(2000\pi t)$. The common-emitter characteristics for the transistor are shown in Figure P13.19. Determine the maximum, minimum, and Q-point values for v_{CE}. What is the approximate voltage gain for this circuit?

Repeat Problem P13.24, with $V_{BB} = 0.3$ V. Why is the gain so small in magnitude?

Repeat Problem P13.24, with $R_C = 10$ kΩ. What can you say about the waveform for $v_{CE}(t)$? Why isn't voltage gain an appropriate concept in this case?

13.4: *pnp* Bipolar Junction Transistors

Draw the circuit symbol for a *pnp* BJT. Label the terminals and the currents. Choose reference directions that agree with the true current direction for operation in the active region.

A certain *pnp* silicon transistor has $\beta = 100$ and $i_B = 50\,\mu$A. Sketch i_C versus v_{CE}, for v_{CE} ranging from 0 to −5 V. Repeat for $\beta = 300$.

The circuit shown in Figure P13.29 has $i_s(t) = 10 + 5\sin(2000\pi t)\ \mu$A. The transistor has $\beta = 100$.

a. Sketch the output characteristics for $i_B = 0$, 5, 10, 15, 20, and 25 μA with v_{CE} ranging from zero to −20 V.

b. Draw the output load line on the characteristics sketched in part (a).

c. Determine the values for $I_{C\max}$, I_{CQ}, and $I_{C\min}$.

d. Sketch $v_{CE}(t)$ to scale versus time.

e. Repeat parts (c) and (d) for $i_s(t) = 20 + 5\sin(2000\pi t)\ \mu$A.

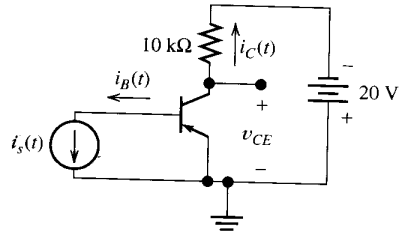


Figure P13.29

P13.30. Suppose we have a certain *pnp* BJT that has $V_{CE} = -5$ V, $I_C = 0.995$ mA, and $I_E = 1.000$ mA. Determine the values for α and β for this transistor.

P13.31. At a temperature of 30°C, a particular *pnp* transistor has $V_{BE} = -0.7$ V for $I_E = 2$ mA. Estimate V_{BE} for $I_E = 2$ mA at a temperature of 180°C.

P13.32. Figure P13.32 shows an *npn* transistor and a *pnp* transistor connected as a **Sziklai pair**, which is equivalent to a single *npn* transistor, as indicated. Find an expression for β_{eq} of the equivalent transistor in terms of β_1 and β_2.

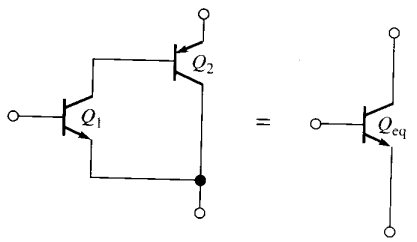


Figure P13.32 Sziklai pair.

Section 13.5: Large-Signal DC Circuit Models

P13.33. Draw the large-signal dc circuit model for a silicon *npn* transistor in the active region at room temperature. Include the constraints of currents and voltages that guarantee operation in the active region. Repeat for the saturation region. Repeat for the cutoff region.

P13.34. Repeat Problem P13.33 for a *pnp* transistor.

*P13.16. Two transistors Q_1 and Q_2 connected in parallel are equivalent to a single transistor, as indicated in Figure P13.16. If the individual transistors have $I_{ES1} = I_{ES2} = 10^{-13}$ A and $\beta_1 = \beta_2 = 100$, determine I_{ES} and β_{eq} for the equivalent transistor. Assume that all transistors have the same temperature.

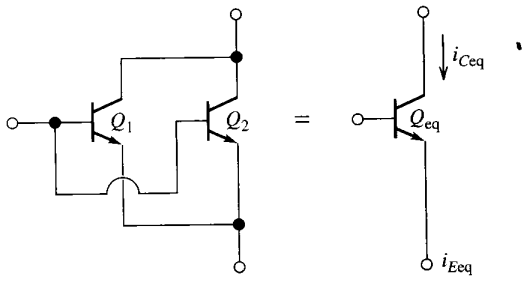


Figure P13.16

P13.17. The transistors Q_1 and Q_2 shown in Figure P13.17 are said to be **Darlington connected** and can be considered to be equivalent to a single transistor, as indicated. Find an expression for β_{eq} of the equivalent transistor in terms of β_1 and β_2.

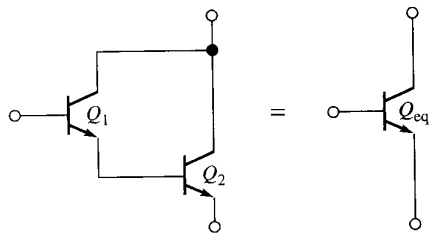
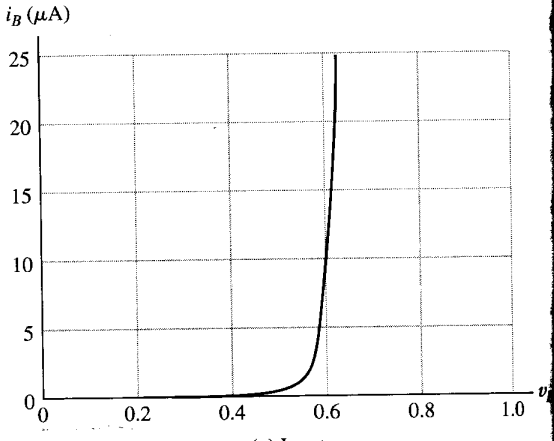


Figure P13.17 Darlington pair.

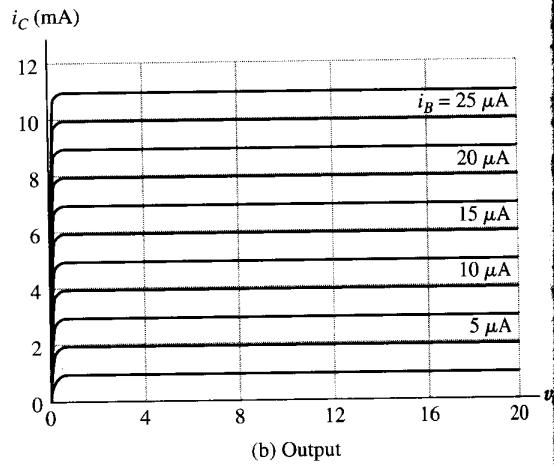
Section 13.2: Common-Emitter Characteristics

*P13.18. A certain *npn* silicon transistor has $v_{BE} = 0.7$ V for $i_B = 0.1$ mA at a temperature of 30°C. Sketch the input characteristic to scale at 30°C. What is the approximate value of v_{BE} for $i_B = 0.1$ mA at 180°C? (Use the rule of thumb that v_{BE} is reduced in magnitude by 2 mV per degree increase in temperature.) Sketch the input characteristic to scale at 180°C.

*P13.19. Determine the values of α and β for transistor whose characteristics are shown Figure P13.19.



(a) Input



(b) Output

Figure P13.19

P13.20. Consider an *npn* silicon transistor th $\beta = 100$ and $i_B = 0.1$ mA. Sketch i_C v_{CE}, for v_{CE} ranging from 0 to 5 V. R for $\beta = 300$.

P13.21. The transistor having the characte shown in Figure P13.19 is operatin $i_C = 8$ mA and $v_{CE} = 12$ V. Locate th of operation on both the input and characteristics.

Problems

Section 7.1: Basic Logic Circuit Concepts

*P7.1. State three advantages of digital technology compared with analog technology.

P7.2. Define these terms: *bit*, *byte*, and *nibble*.

P7.3. Explain the difference between positive logic and negative logic.

P7.4. What are noise margins? Why are they important?

P7.5. How is serial transmission of a digital word different from parallel transmission?

Section 7.2: Representation of Numerical Data in Binary Form

P7.6. Convert the following binary numbers to decimal form: **a.*** 101.101; **b.** 0111.11; **c.** 1010.01; **d.** 111.111; **e.** 1000.0101; **f.*** 10101.011.

P7.7. Express the following decimal numbers in binary form and in binary-coded-decimal form: **a.** 17; **b.** 8.5; **c.*** 9.75; **d.** 73.03125; **e.** 67.375.

P7.8. How many bits per word are needed to represent the decimal integers 0 through 100? 0 through 1000? 0 through 10^6?

P7.9. Add these pairs of binary numbers: **a.*** 1101.11 and 101.111; **b.** 1011 and 101; **c.** 10001.111 and 0101.001.

P7.10. Find the result (in BCD format) of adding the BCD numbers: **a.** * 10010011.0101 and 00110111.0001; **b.** 01011000.1000 and 10001001.1001.

P7.11. Express the following decimal numbers in binary, octal, and hexadecimal forms: **a.** 173; **b.** 299.5; **c.** 735.75; **d.*** 313.0625; **e.** 112.25.

P7.12. Write each of the following decimal numbers as an eight-bit signed two's-complement number: **a.** 19; **b.** −19; **c.*** 75; **d.*** −87; **e.** −95; **f.** 99.

P7.13. Express each of the following hexadecimal numbers in binary, octal, and decimal forms: **a.** $FA.F_{16}$; **b.** $2A.1_{16}$; **c.** 777.7_{16}.

P7.14. Express each of the following octa in binary, hexadecimal, and decim **a.** 777.7_8; **b.** 123.5_8; **c.** 24.4_8.

P7.15. What number follows 777 when co **a.** decimal; **b.** octal; **c.** hexadecimal?

P7.16. What range of decimal integers can sented by **a.** three-bit binary number digit octal numbers; **c.** three-digit he numbers?

*P7.17. Starting with the three-bit Gray cod Figure 7.9, construct a four-bit Gray what applications is a Gray code advan Why?

P7.18. Convert the following numbers to form: **a.** * $FA5.6_{16}$; **b.** * 725.3_8; **c.** **d.** 73.25_8; **e.** $FF.F0_{16}$.

P7.19. Find the one's and two's complemen binary numbers: **a.** * 11101000; **b.** 0 **c.** 10101010; **d.** 11111100; **e.** 11000000.

P7.20. Perform these operations by using 8-bi two's-complement arithmetic: **a.** 17_{10} **b.** $17_{10} - 15_{10}$; **c.*** $33_{10} - 37_{10}$; **d.** 15_{10} **e.** $49_{10} - 44_{10}$.

P7.21. Describe how to test whether overflow derflow has occurred in adding signed complement numbers.

Section 7.3: Combinatorial Logic Circuits

P7.22. What is a truth table?

*P7.23. State De Morgan's laws.

P7.24. Draw the circuit symbol and list the truth for the following: an AND gate, an OR an inverter, a NAND gate, a NOR gat an XOR gate. Assume two inputs for eac (except the inverter).

P7.25. Describe a method for proving the validi Boolean algebra identity.

---

* Denotes that answers can be found on the OrCAD CD and on the website www.myengineeringlab.com

...e truth table for each of these Boolean ...ions:

$= ABC + A\overline{B}$

$= AB + A\overline{B}C + \overline{C}D$

$= WX + \overline{(W + Y)}$

$= A + \overline{A}B + C$

$= \overline{(A + BC)}$

...a Boolean expression for the output of ...f the logic circuits shown in Figure P7.27.

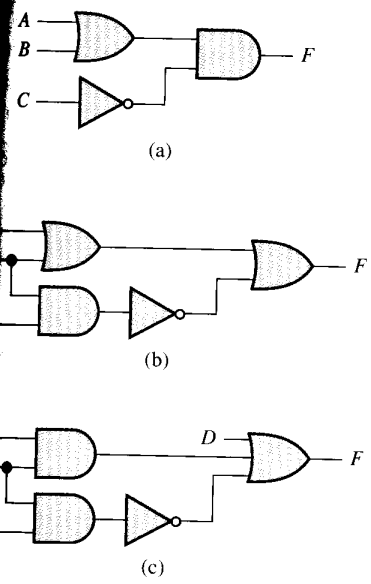


Figure P7.27

...a truth table to prove the identity

$$(A + B)(A + C) = A + BC$$

...a truth table to prove the identity

$$(A + B)(\overline{A} + AB) = B$$

...a truth table to prove the identity

$$A + \overline{A}B = A + B$$

...a truth table to prove the identity

$$ABC + AB\overline{C} + A\overline{B}\,\overline{C} + A\overline{B}C = A$$

P7.32. Draw a circuit to realize each of the following expressions using AND gates, OR gates, and inverters:

a. $F = A + \overline{B}C$

b. $F = A\overline{B}C + AB\overline{C} + \overline{A}BC$

c. * $F = (\overline{A} + \overline{B} + C)(A + B + \overline{C})(A + \overline{B} + C)$

P7.33. Replace the AND operations by ORs and vice versa by applying De Morgan's laws to each of these expressions:

a. $F = AB + (\overline{C} + A)\overline{D}$

b. $F = A(\overline{B} + C) + D$

c. $F = A\overline{B}C + A(B + C)$

d. * $F = (A + B + C)(A + \overline{B} + C)(\overline{A} + B + \overline{C})$

e. * $F = ABC + A\overline{B}C + \overline{A}B\overline{C}$

P7.34. Why are NAND gates said to be *sufficient* for combinatorial logic? What other type of gate is sufficient?

P7.35. Consider the circuit shown in Figure P7.35. The switches are controlled by logic variables such that, if A is high, switch A is closed, and if A is low, switch A is open. Conversely, if B is high, the switch labeled $\overline{B}$ is open, and if B is low, the switch labeled $\overline{B}$ is closed. The output variable is high if the output voltage is 5 V, and the output variable is low if the output voltage is zero. Write a logic expression for the output variable. Construct the truth table for the circuit.

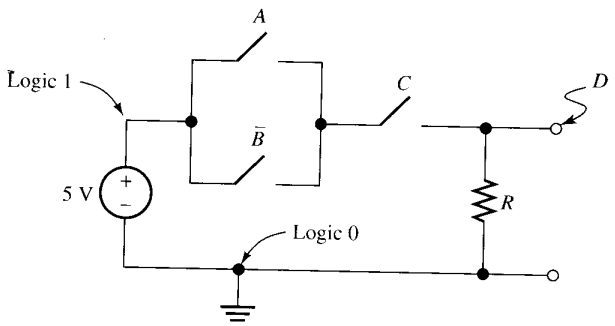


Figure P7.35

P7.36. Repeat Problem P7.35 for the circuit shown in Figure P7.36.

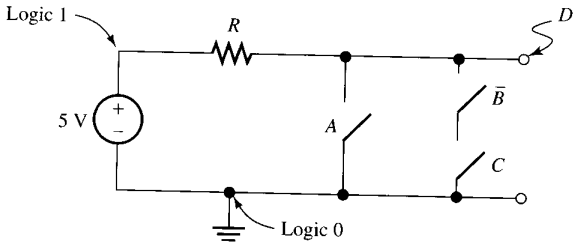


Figure P7.36

P7.37. Sometimes "bubbles" are used to indicate inverters on the input lines to a gate, as illustrated in Figure P7.37. What are the equivalent gates for those of Figure P7.37? Justify your answers.

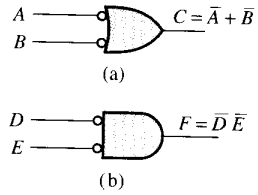


Figure P7.37

Section 7.4: Synthesis of Logic Circuits

P7.38. Using the sum-of-products approach, describe the synthesis of a logic expression from a truth table. Repeat for the product-of-sums approach.

P7.39. Give an example of a decoder.

*__P7.40.__ Consider Table P7.40. A, B, and C represent logic-variable input signals; F through K are outputs. Using the product-of-sums app write a Boolean expression for F in te the inputs. Repeat by using the sum-of-pr approach.

Table P7.40

A	B	C	F	G	H	I	J	K
0	0	0	1	1	1	0	0	1
0	0	1	0	0	1	0	1	1
0	1	0	1	0	1	0	0	0
0	1	1	0	1	0	1	1	0
1	0	0	0	0	1	0	0	0
1	0	1	1	0	1	0	1	0
1	1	0	0	0	1	1	1	1
1	1	1	1	0	1	1	1	1

P7.41. Repeat Problem P7.40 for G.

P7.42. Repeat Problem P7.40 for H.

P7.43. Repeat Problem P7.40 for I.

P7.44. Repeat Problem P7.40 for J.

P7.45. Repeat Problem P7.40 for K.

P7.46. Show how to implement the sum-of-pr circuit shown in Figure P7.46 by using NAND gates.

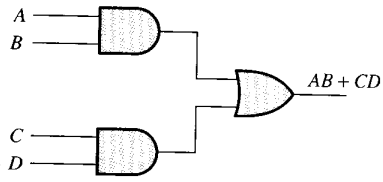


Figure P7.46

P7.47. Show how to implement the product-of circuit shown in Figure P7.47 by using NOR gates.

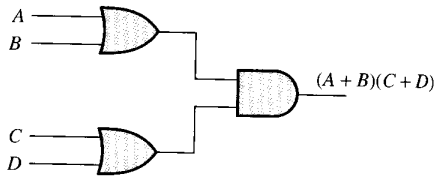


Figure P7.47

P7.48. Design a logic circuit to control electrical p to the engine ignition of a speed boat. Logic put I is to become high if ignition power is applied and is to remain low otherwise. C line fumes in the engine compartment pr a serious hazard of explosion. A sensor vides a logic input F that is high if fume present. Ignition power should not be ap if fumes are present. To help prevent accid ignition power should not be applied whil outdrive is in gear. Logic signal G is hi the outdrive is in gear and is low other

e signal B becomes high after the blower een in operation for five minutes. Finally, nergency override signal E is provided so the operator can choose to apply ignition er even if the blower has not operated for minutes and if the outdrive is in gear, but f gasoline fumes are present. **a.** Prepare a table listing all combinations of the input als B, E, F, and G. Also, show the desired e of I for each row in the table. **b.** Using sum-of-products approach, write a Boolean ression for I. **c.** Using the product-of-sums roach, write a Boolean expression for I. Try to manipulate the expressions of parts and (c) to obtain a logic circuit having the t number of gates and inverters. Use AND es, OR gates, and inverters.

only NAND gates to find a way to imple- nt the XOR function for two inputs, A and (*Hint:* The inputs of a two-input NAND can wired together to obtain an inverter. List truth table and write the SOP expression. en, apply De Morgan's laws to convert the operation to AND.)

e only two-input NOR gates to find a way to plement the XOR function for two inputs, A B. (*Hint:* The inputs of a two-input NOR be wired together to obtain an inverter. List truth table and write the POS expression. en, apply De Morgan's laws to convert the ND operation to OR.)

nsider the BCD-to-seven-segment decoder cussed in conjunction with Figure 7.26 on ge 369. Suppose that the BCD data are rep- ented by the logic variables B_8, B_4, B_2, and . For example, the decimal number 7 is rep- ented in BCD by the word 0111 in which the tmost bit is $B_8 = 0$, the second bit is $B_4 = 1$, d so forth. **a.** Find a logic circuit based on the oduct of maxterms having output A that is h only if segment A of the display is to be **b.** Repeat for segment B.

sign bit of the first number, S_2 is the sign bit of the second number, and S_T is the sign bit of the total. Suppose that we want a logic circuit with output E that is high if either overflow or underflow has occurred; otherwise, E is to remain low. **a.** Write the truth table. **b.** Find an SOP expression composed of minterms for E. **c.** Draw a circuit that yields E, using AND, OR, and NOT gates.

Section 7.5: Minimization of Logic Circuits

*P7.53. **a.** Construct a Karnaugh map for the logic function

$$F = \overline{A}BC\,\overline{D} + AB\overline{C}\,\overline{D} + \overline{A}B\overline{C}D + AB\overline{C}D + \overline{A}BC\overline{D} + \overline{A}\,\overline{B}C\overline{D}$$

b. Find the minimum SOP expression. **c.** Find the minimum POS expression.

P7.54. A logic circuit has inputs A, B, and C. The output of the circuit is given by

$$D = \sum m(0, 3, 4)$$

a. Construct the Karnaugh map for D.
b. Find the minimum SOP expression.
c. Find two equally good minimum POS expressions.

P7.55. A logic circuit has inputs A, B, and C. The output of the circuit is given by

$$D = \prod M(1, 3, 4, 6)$$

a. Construct the Karnaugh map for D.
b. Find the minimum SOP expression.
c. Find the minimum POS expression.

P7.56. **a.** Construct a Karnaugh map for the logic function

$$D = ABC + \overline{A}BC + AB\overline{C} + BC$$

b. Find the minimum SOP expression and realize the function, using AND, OR, and NOT gates.
c. Find the minimum POS expression and realize the function, using AND, OR, and NOT gates.

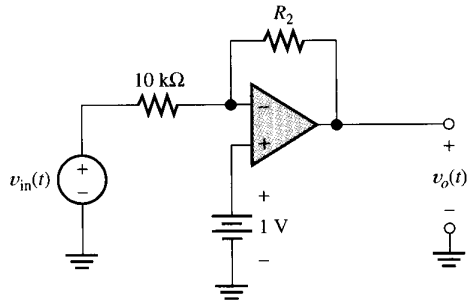
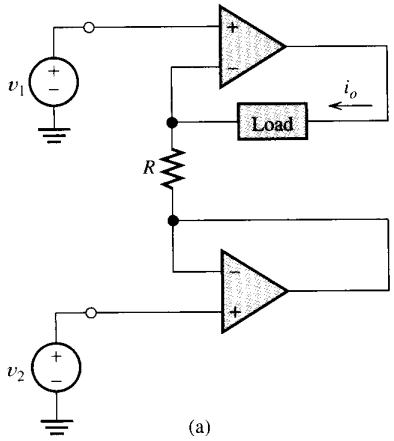
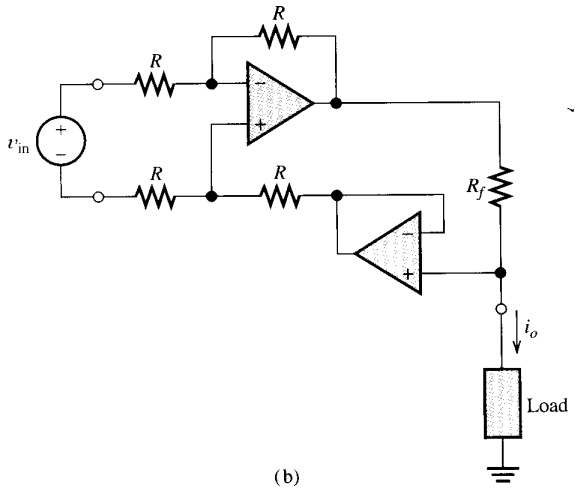


Figure P14.22

P14.23. Analyze each of the ideal-op-amp circuits shown in Figure P14.23 to find expressions for i_o. What is the value of the output impedan for each of these circuits? Why? [*Note:* T bottom end of the input voltage source is grounded in part (b) of the figure. Thus, say that this source is *floating*.]



(a)



(b)

Figure P14.23

***P14.24.** Consider the circuit shown in Figure P14. **a.** Find an expression for the output volt in terms of the source current and resistan values. **b.** What value is the output impedan of this circuit? **c.** What value is the in impedance of this circuit? **d.** This circuit be classified as an ideal amplifier. What the amplifier type? (See Section 11.6 fo discussion of various ideal-amplifier types.)

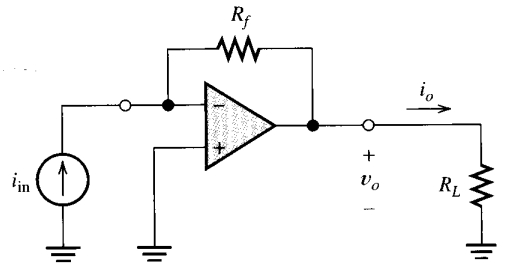


Figure P14.24

P14.25. Repeat Problem P14.24 for the circuit sho in Figure P14.25.

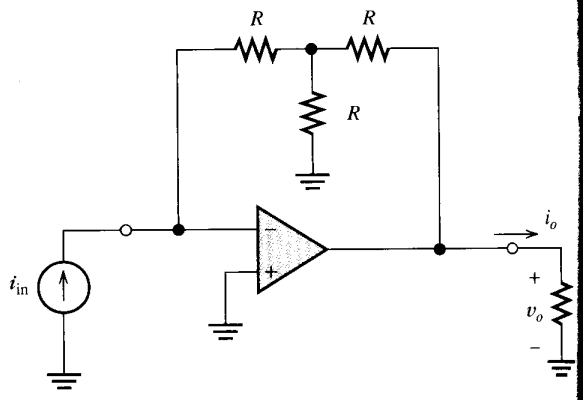


Figure P14.25

P14.26. Consider the circuit shown in Figure P14 **a.** Find an expression for the output curre

fer function of the filter can be determined. Compute the transfer function for each of these frequencies.

*P6.17. Consider a circuit for which the output voltage is the running-time integral of the input voltage, as illustrated in Figure P6.17. The input voltage is given by

$$v_{in}(t) = V_{max}\cos(2\pi f t)$$

Find an expression for the output voltage as a function of time. Then find an expression for the transfer function of the integrator. Plot the magnitude and phase of the transfer function versus frequency.

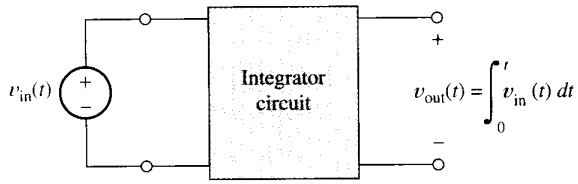


Figure P6.17

P6.18. Consider a circuit for which the output voltage is the time derivative of the input voltage, as illustrated in Figure P6.18. The input voltage is given by

$$v_{in}(t) = V_{max}\cos(2\pi f t)$$

Find an expression for the output voltage as a function of time. Then find an expression for the transfer function of the differentiator. Plot the magnitude and phase of the transfer function versus frequency.

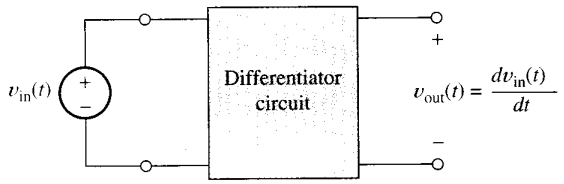


Figure P6.18

is

$$v_o(t) = v_{in}(t) + v_{in}(t - 10^{-3})$$

(The output equals the input plus the inp delayed by 1 ms.) The input voltage given by

$$v_{in}(t) = V_{max}\cos(2\pi f t)$$

Find an expression for the output voltage a function of time. Then find an expression for t transfer function of the system. Use a compu program of your choice to plot the magnitu of the transfer function versus frequency f the range from 0 to 2000 Hz. Comment on t result.

P6.20. Repeat Problem P6.19 for

$$v_o(t) = 1000\int_{t-10^{-3}}^{t} v_{in}(t)\,dt$$

Section 6.2: First-Order Lowpass Filters

P6.21. Draw the circuit diagram of a first-ord *RC* lowpass filter and give the expressio for the half-power frequency in terms the circuit components. Sketch the magn tude and phase of the transfer function versu frequency.

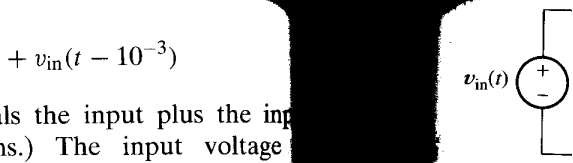
P6.22. Repeat Problem P6.21 for a first-order *RL* fi ter.

P6.23. Recall that in Chapter 4 we used the tim constant to characterize first-order *RC* circuit Find the relationship between the half-powe frequency and the time constant.

*P6.24. An input signal given by

$$v_{in}(t) = 5\cos(500\pi t) + 5\cos(1000\pi t) + 5\cos(2000\pi t)$$

is applied to the lowpass *RC* filter shown i Figure P6.24. Find an expression for the outpu signal.



25. The inp with a h by

$(t) = 4 + 2s$

Find an

26. Conside what fre shift equ

27. Suppose filter wi Determi that the

28. A first-o soidal st 2 kHz. U that the by 0.1 m the inpu the filter.

29. Suppose tains com 100 Hz t plitude o 100 by pa lowpass required compone passing th

30. A first-o signal

v_{in}

and the o

v_{out}(

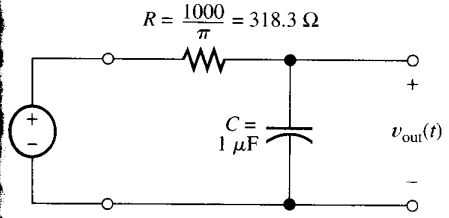


Figure P6.24

e input signal of a first-order lowpass filter th a half-power frequency of 500 Hz is given

$$4 + 2\sin(1000\pi t + 30°) + 5\cos(30 \times 10^3 \pi t)$$

nd an expression for the output voltage.

nsider a first-order RC lowpass filter. At at frequency (in terms of f_B) is the phase ift equal to $-1°$? $-10°$? $-89°$?

ppose that we need a first-order RC lowpass ter with a half-power frequency of 1 kHz. termine the value of the capacitance, given at the resistance is 1 kΩ.

first-order lowpass filter is operating in sinuidal steady-state conditions at a frequency of kHz. Using an oscilloscope, it is determined at the positive peak of the output is delayed 0.1 ms compared with the positive peak of e input. Determine the break frequency of e filter.

ppose that we have an input signal that conins components that range in frequency from 0 Hz to 10 kHz. We wish to reduce the amtude of the 10-kHz component by a factor of 0 by passing the signal through a first-order wpass filter. What half-power frequency is quired for the filter? By what factor is a mponent at 1 kHz changed in amplitude in ssing through this filter?

first-order RC lowpass filter has the input nal

$$v_{in}(t) = \cos(20 \times 10^3 \pi t)$$

d the output signal

$$v_{out}(t) = \cos(20 \times 10^3 \pi t - \theta)$$

Determine the break frequency of the filter and the value of θ.

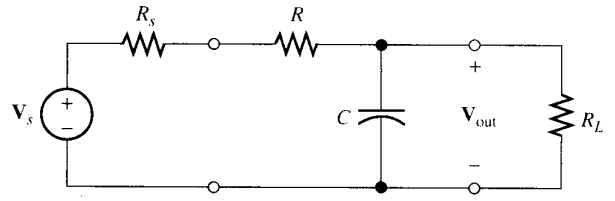
P6.31. Consider the circuit shown in Figure P6.31(a). This circuit consists of a source having an internal resistance of R_s, an RC lowpass filter, and a load resistance R_L. **a.** Show that the transfer function of this circuit is given by

$$H(f) = \frac{\mathbf{V}_{out}}{\mathbf{V}_s} = \frac{R_L}{R_s + R + R_L} \times \frac{1}{1 + j(f/f_B)}$$

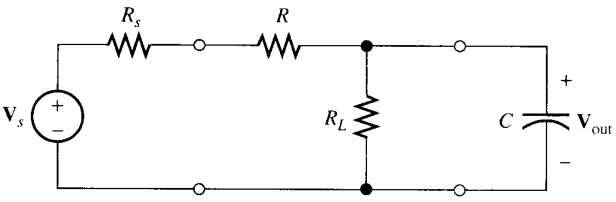
in which the half-power frequency f_B is given by

$$f_B = \frac{1}{2\pi R_t C} \quad \text{where} \quad R_t = \frac{R_L(R_s + R)}{R_L + R_s + R}$$

Notice that R_t is the parallel combination of R_L and $(R_s + R)$. [*Hint:* One way to make this problem easier is to rearrange the circuit as shown in Figure P6.31(b) and then to find the Thévenin equivalent for the source and resistances.] **b.** Given that $C = 1\ \mu F$, $R_s = 1$ kΩ, $R = 2$ kΩ, and $R_L = 3$ kΩ, sketch (or use a computer to plot) the magnitude of $H(f)$ to scale versus frequency up to $3f_B$.



(a)



Find Thévenin equivalent

(b)

Figure P6.31