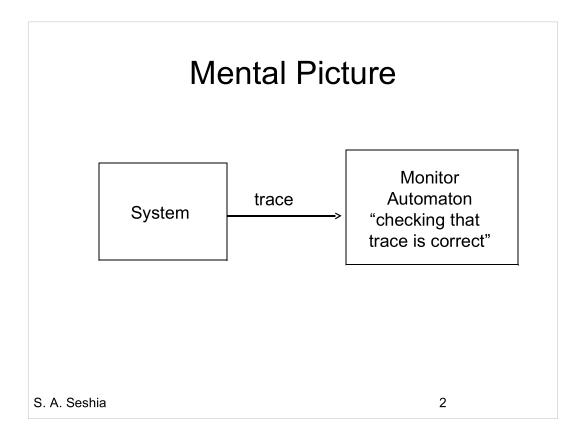
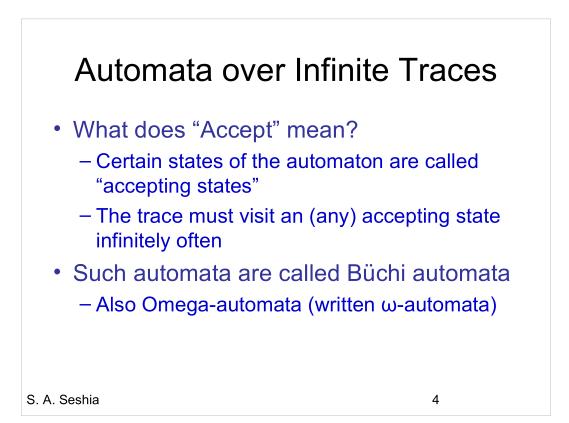
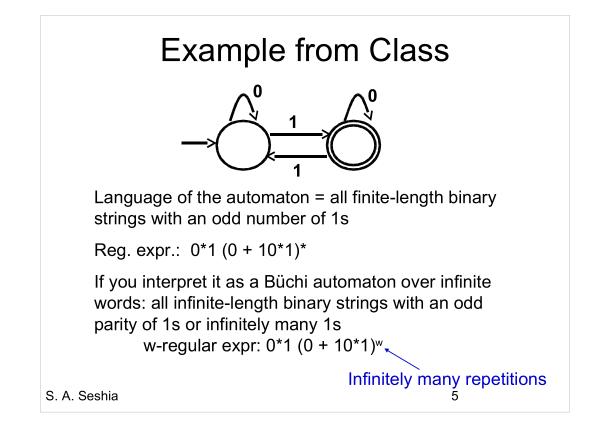
EECS 219C: Computer-Aided Verification Properties as Automata and Explicit-State Model Checking

> Sanjit A. Seshia EECS, UC Berkeley





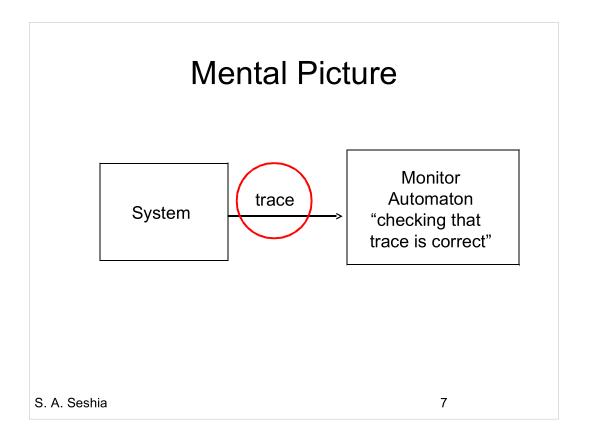


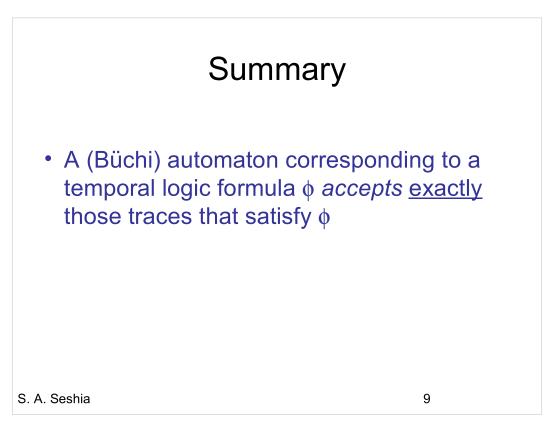


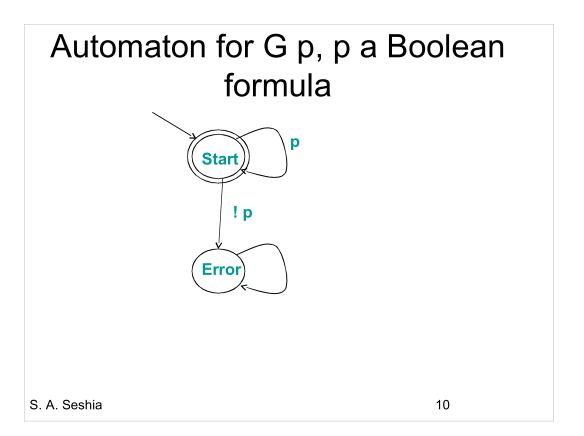
From Temporal Logic to Monitors

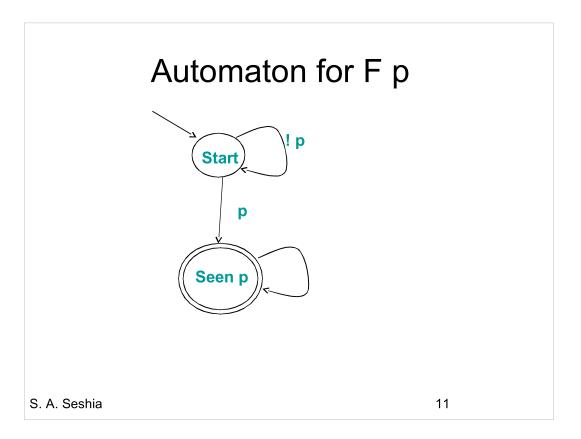
- A monitor for a temporal logic formula
 - is a finite automaton
 - Accepts exactly those behaviors that satisfy the temporal logic formula
 - "Accepts" means that an accepting state is visited infinitely often
- Properties are often specified as automata

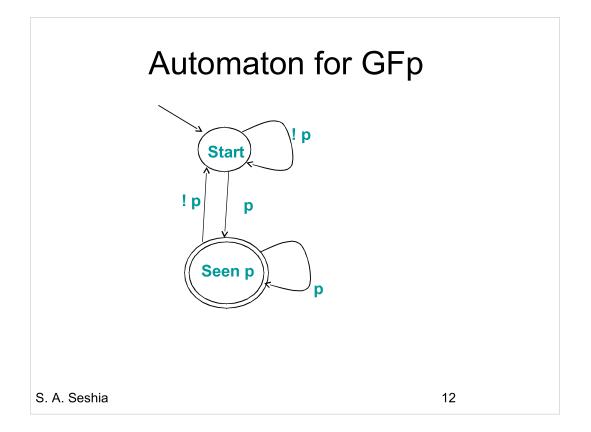
S. A. Seshia



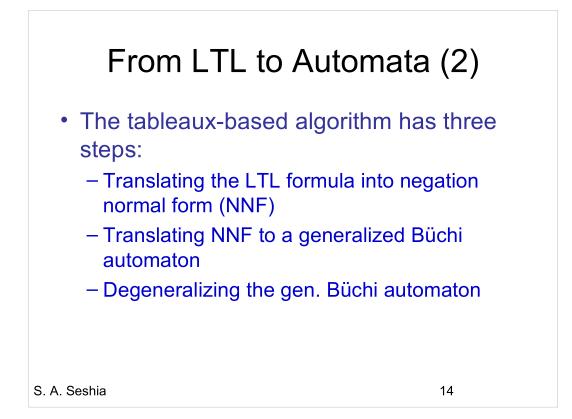


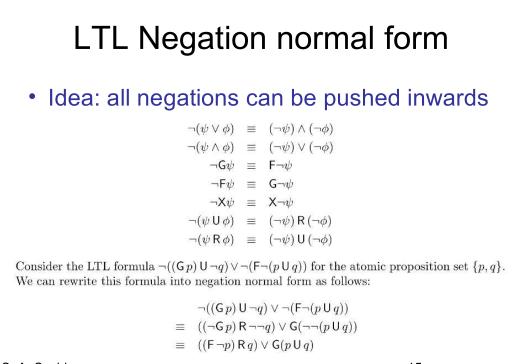






From LTL to Automata (1) Any LTL formula can be translated to a corresponding automaton There are many translation algorithms We discus the classical tableaux-based one Reference: Rob Gerth, Doron Peled, Moshe Y, Vardi, Pierre Wolper: Simple on-the-fly automatic verification of linear temporal logic. PSTV 1995: 3-18





S. A. Seshia

