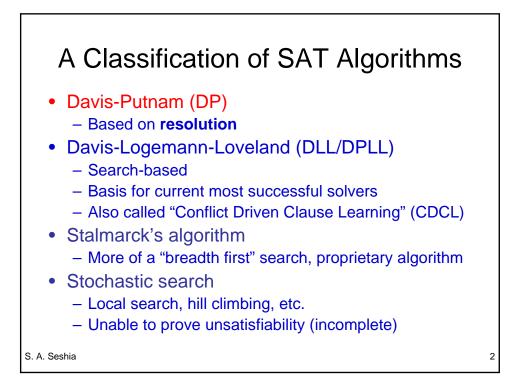
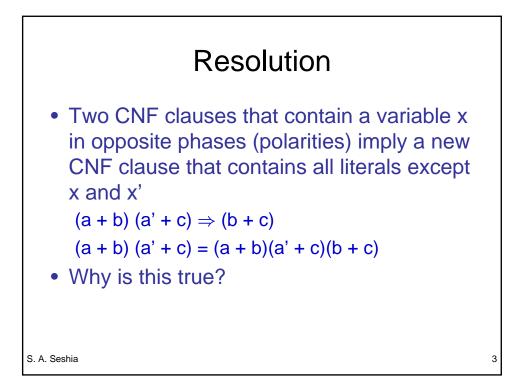
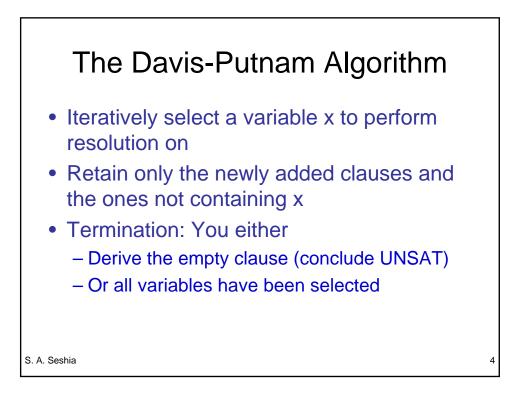
EECS 219C: Computer-Aided Verification Boolean Satisfiability Solving Part II: DPLL-based (CDCL) Solvers

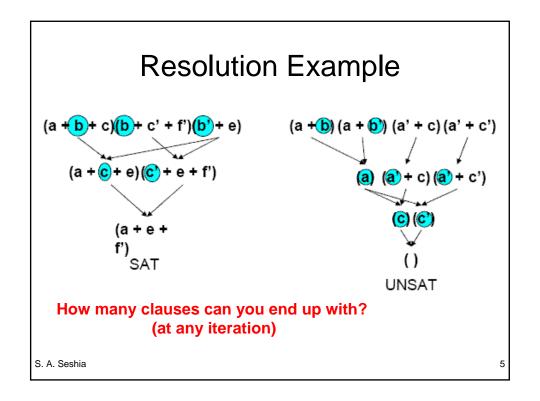
> Sanjit A. Seshia EECS, UC Berkeley

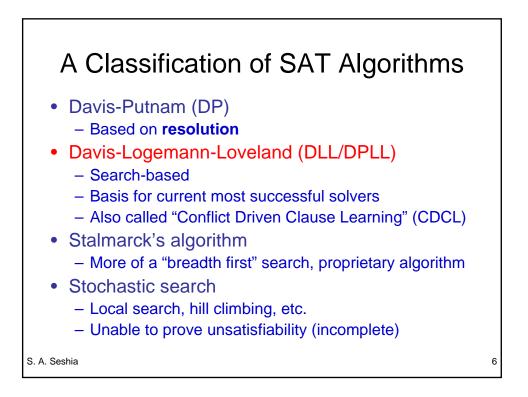
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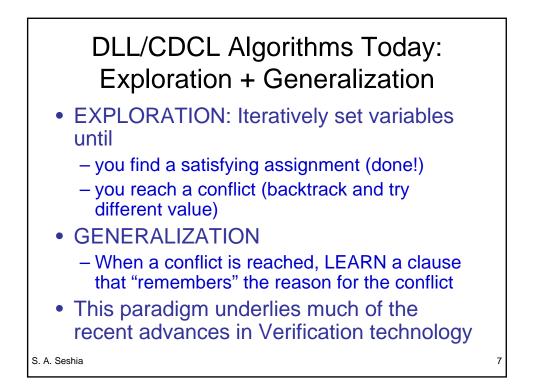


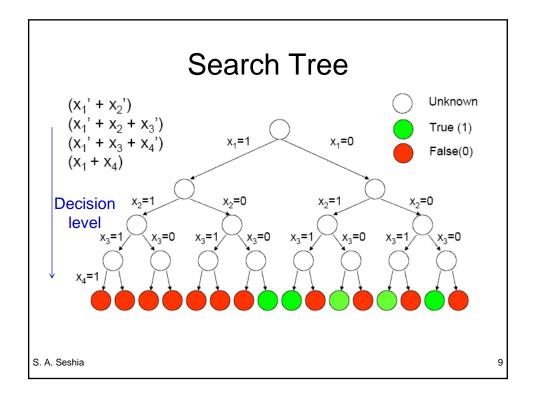


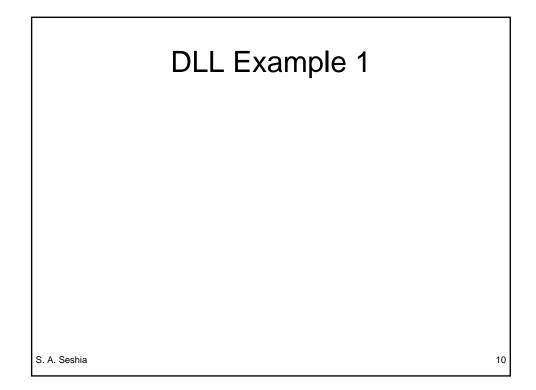


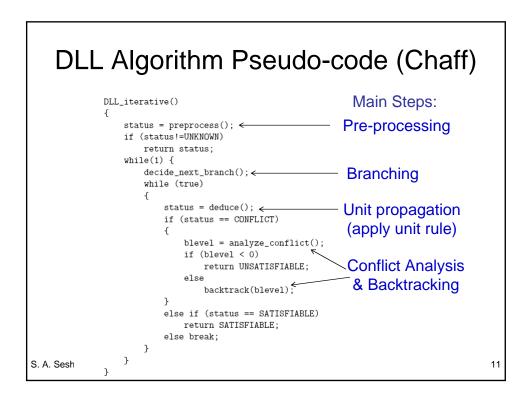


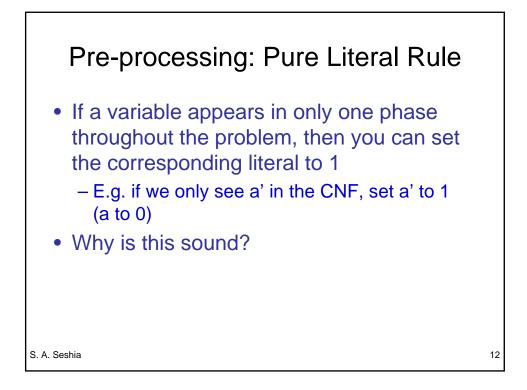


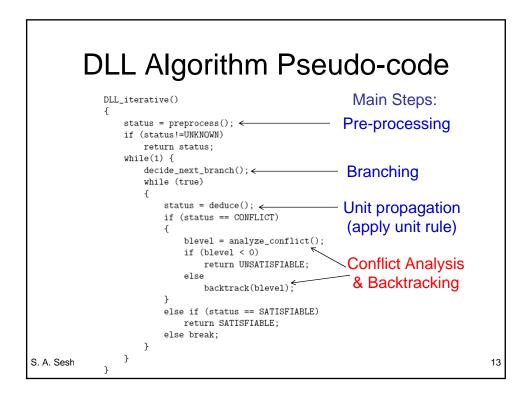


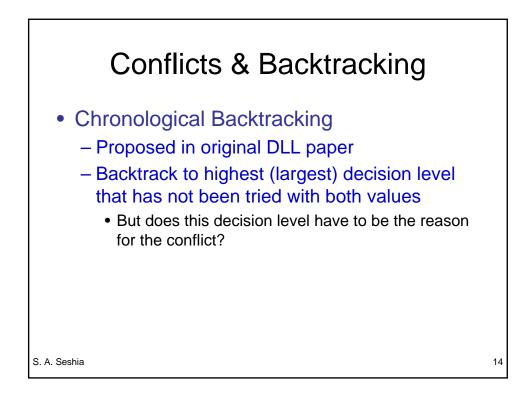


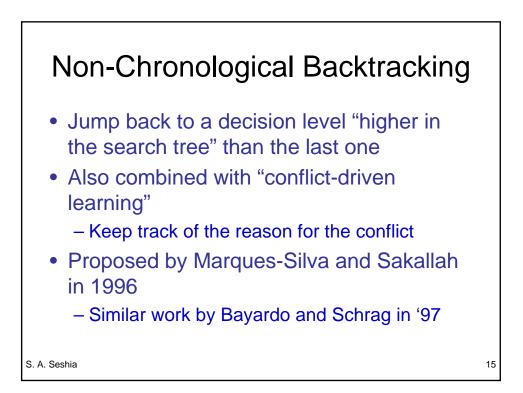


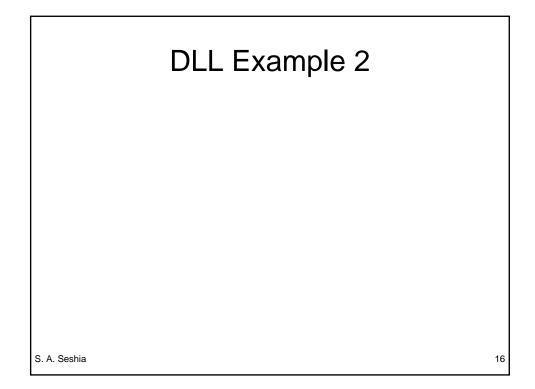


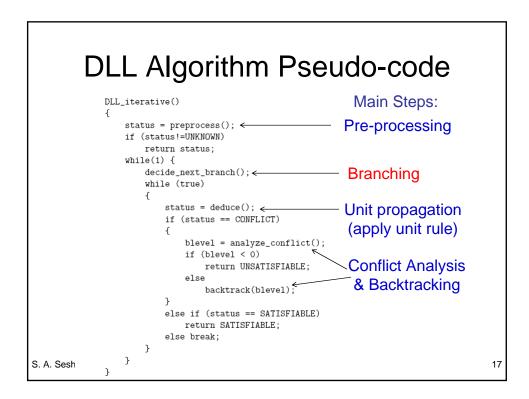


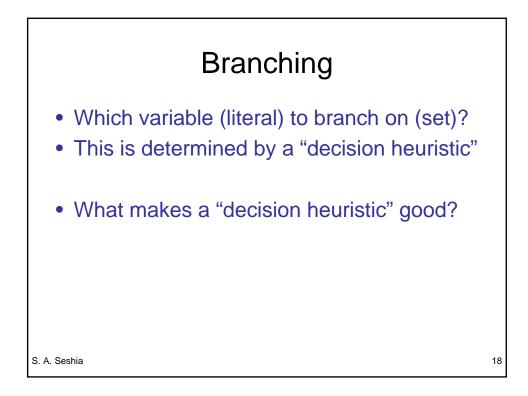


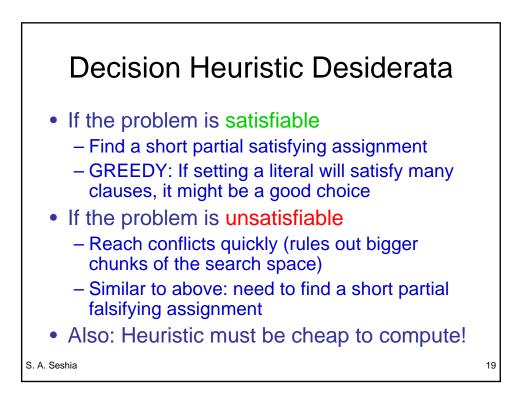


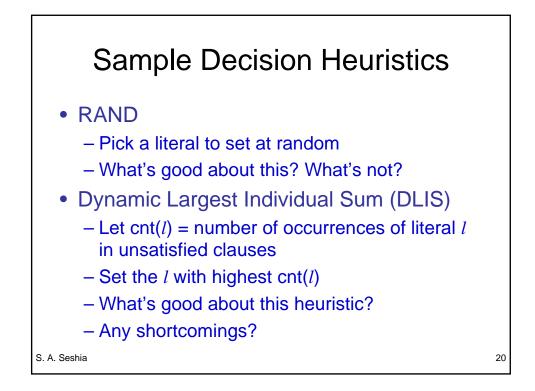


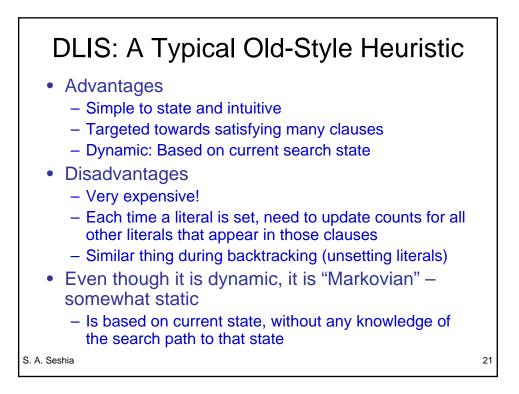


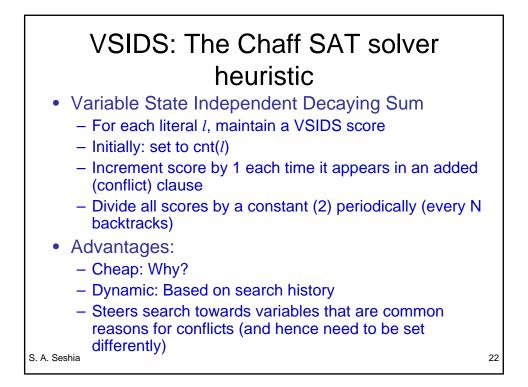


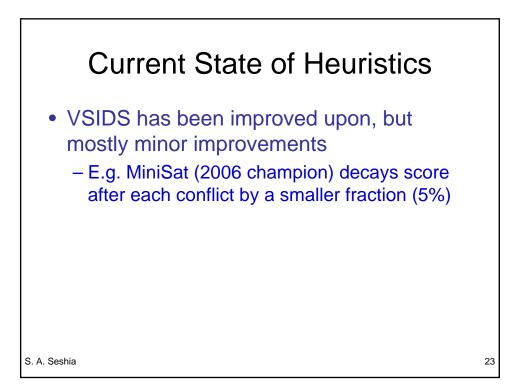


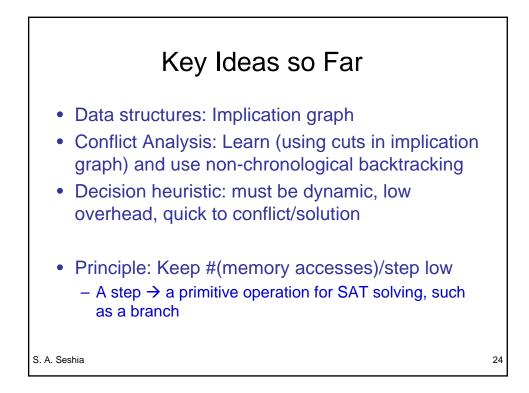


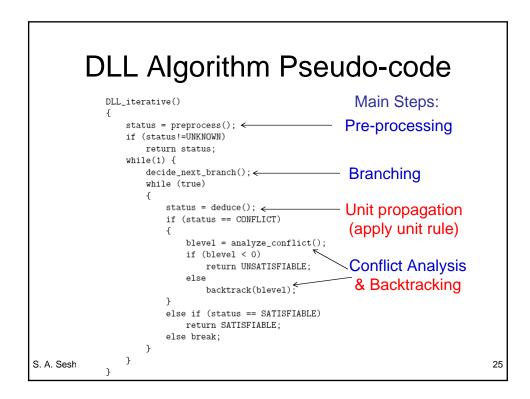


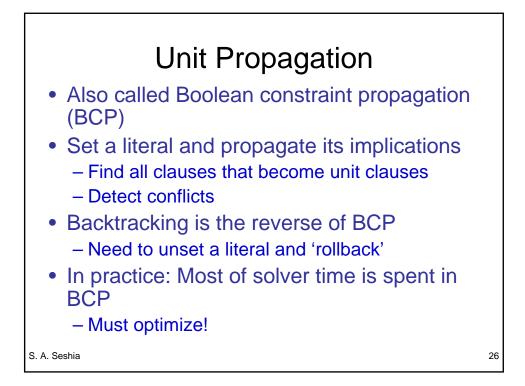


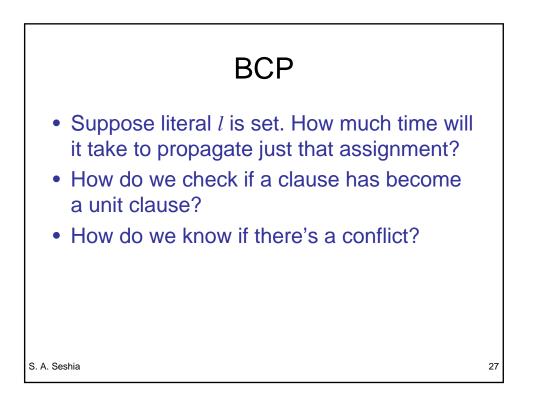


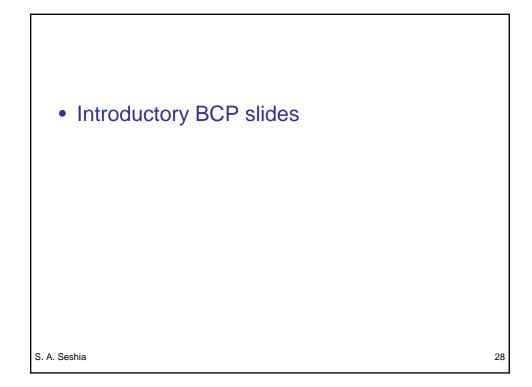


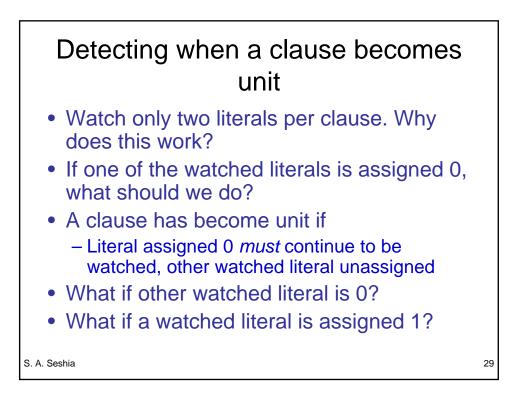


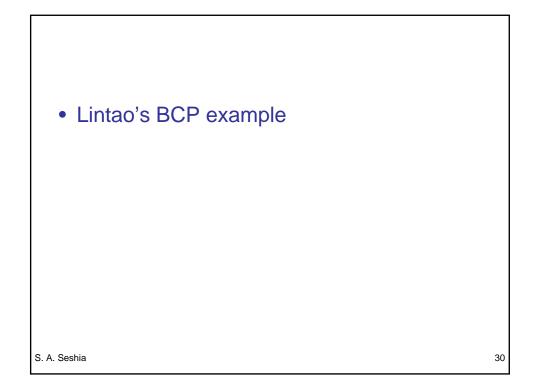


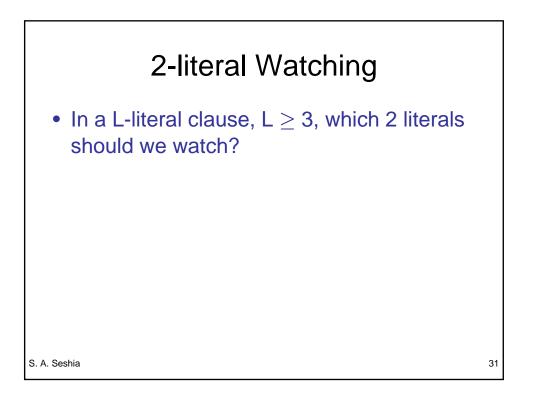


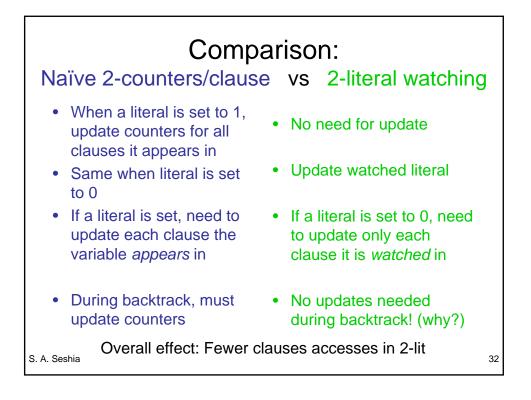


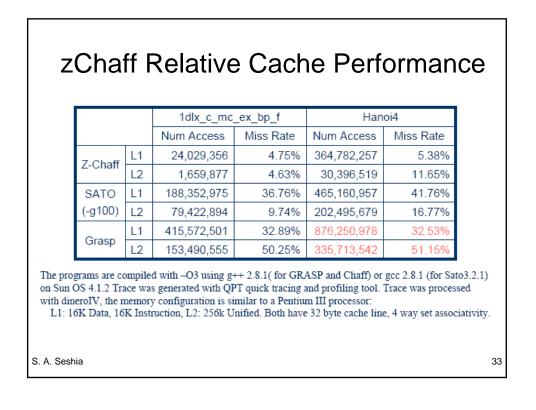








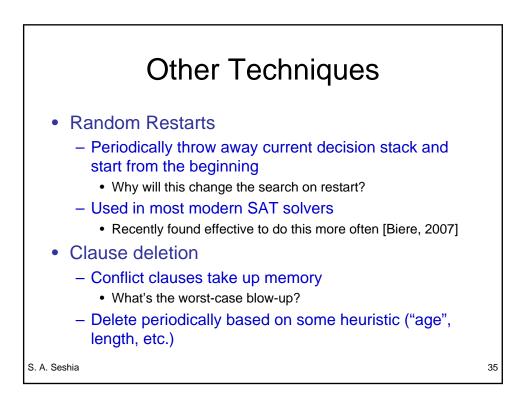




## Key Ideas in Modern DLL SAT Solving

- Data structures: Implication graph
- Conflict Analysis: Learn (using cuts in implication graph) and use non-chronological backtracking
- Decision heuristic: must be dynamic, low overhead, quick to conflict/solution
- Unit propagation (BCP): 2-literal watching helps keep memory accesses down
- Principle: Keep #(memory accesses)/step low
  A step → a primitive operation for SAT solving, such as a branch

S. A. Seshia



34

