

# Rajesh Nishtala

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## Objective

Conduct leading research in the areas of Computer Systems and Parallel Computing in an industrial research lab.

## Education

8/03 – current UC Berkeley Berkeley, CA  
**Working towards a PhD in Computer Science from UC Berkeley with an emphasis in Computer Systems and Parallel Computing**

5/06 UC Berkeley Berkeley, CA  
**Obtained a Master of Science in Computer Science emphasizing in Computer Systems and Parallel Computing**

5/06 UC Berkeley Berkeley, CA  
**Obtained a Management of Technology Certificate from the UC Berkeley Haas School of Business**

8/99 – 5/03 UC Berkeley Berkeley, CA  
**Graduated with Honors with a Bachelors of Science in Electrical Engineering and Computer Science emphasizing in Computer Systems**  
**IBM PhD Fellowship (2008-2009)**

## Honors

**UC Berkeley Outstanding Graduate Student Instructor Award for CS162 (Operating Systems) (March 2006)**

**UC Berkeley Unsung Hero Award for Undergraduate Research Mentoring (November 2005)**

**Siebel Scholar Class of 2005**

## Research Experience

6/03 - current Parallel Computing Laboratory, UC Berkeley Berkeley, CA  
Berkeley UPC Group at Lawrence Berkeley Nat'l Labs Berkeley, CA  
**Graduate Student Researcher**

- Working under Professor Katherine Yelick and Professor James Demmel on automatic performance optimization of communication algorithms on multicore systems and large clusters of Multicore systems.
- Analyze scalability of large parallel applications on a variety of modern multicore architectures and system interconnects
- Wrote the IBM BlueGene/P port of the Berkeley UPC compiler
- Work with novel parallel programming models and languages to aid in programmer productivity and application scalability.
- Work closely with parallel architecture and parallel operating systems groups to identify key challenges in parallel programming and work to create new parallel constructs (at all levels of the software hierarchy) to aid in parallel programming.

6/07 – 8/07 IBM TJ Watson Research Laboratory Yorktown Heights, NY  
**Summer Research Intern**

- Worked with Gheorghe Almasi and Calin Cascaval on programming systems to aid productivity and scalability of large applications across thousands of processors on the BlueGene/L
- Using new language features on 16,384 processors on BlueGene/L and developed multi-dimensional Fast Fourier Transforms that achieved over 2 TeraFlop/s and Dense Linear Algebra Kernels that achieved over 28 TeraFlop/s in less than 20 lines of code.

10/01-5/03 BeBop Group at UC Berkeley Berkeley, CA  
**Undergraduate Research Assistant**

- Working under Professor Katherine Yelick and Professor James Demmel in performance modeling of sparse matrix multiplication, including analysis of cache misses and TLB miss behavior on a variety of modern architectures.

**Teaching  
Experience**

1/06 – 5/06 UC Berkeley Berkeley, CA  
**Graduate Student Instructor (CS267, Professor James Demmel)**  
• Teaching a graduate course in The Applications of Parallel Computing. Responsibility included leading class recitations and overseeing student projects

8/05 - 12/05 UC Berkeley Berkeley, CA  
**Graduate Student Instructor (CS162, Professor John Kubiawicz)**  
• Taught undergraduate course in Operating Systems. Responsibility included leading class recitations, holding office hours, leading review sessions, writing detailed notes, creating exams, and overseeing student projects

**Publications  
and Talks**

**Scaling Communication Intensive Applications on BlueGene/P Using One-Sided Communication and Overlap** (*International Parallel and Distributed Processing Symposium, Rome, Italy, May 2009*) Rajesh Nishtala, Paul Hargrove, Dan Bonachea, Katherine Yelick

**Optimizing Collective Communication on Multicores** (*HotPar 2009, Berkeley, CA, USA, March 2009*) Rajesh Nishtala and Katherine Yelick

**Performance without Pain=Productivity, Data layouts and Collectives in UPC** (*Principles and Practices of Parallel Programming (PPoPP) 2008, Salt Lake City, USA, February 2008*) Rajesh Nishtala, George Almasi, Calin Cascaval

**Productivity and Performance Using Partitioned Global Address Space Languages** (*Invited Talk, Parallel Symbolic Computation, London, Canada, July 2007*), Katherine Yelick, Dan Bonachea, Wei-Yu Chen, Phillip Colella, Kaushik Datta, Jason Duell, Susan L. Graham, Paul Hargrove, Paul Hilfinger, Parry Husbands, Costin Iancu, Amir Kamil, Rajesh Nishtala, Jimmy Su, Michael Welcome, and Tong Wen

**Poster on Optimized Collectives for PGAS Languages with One-Sided Communication** (*Supercomputing, Tampa Bay, USA, November 2006*) Dan O. Bonachea, Rajesh Nishtala, Paul Hargrove, Mike Welcome, Kathy Yelick

**Talk on Efficient Point-to-point Synchronization in UPC** (*Partitioned Global Address Space Programming Models, Washington DC, USA, October 2006*) Dan Bonachea, Rajesh Nishtala, Paul Hargrove, Katherine Yelick

**Masters Report: Architectural Probes for Measuring Communication Overlap Potential** (submitted May 19th, 2006 for Master of Science Degree) Rajesh Nishtala

**Optimizing Bandwidth Limited Problems Using One-Sided Communication and Overlap** (*International Parallel and Distributed Processing Symposium, Rhodes, Greece, April 2006*) Christian Bell, Dan Bonachea, Rajesh Nishtala, Katherine Yelick

**Poster on The Performance and Productivity Benefits of Global Address Space Languages** (*Supercomputing, Seattle, USA, November 2005*) Dan O. Bonachea, Christian Bell, Rajesh Nishtala, Kaushik Datta, Parry Husbands, Paul Hargrove, Katherine Yelick

**When Cache Blocking Sparse Matrix Vector Multiply Works and Why** (*PARA 2004 Workshop On State-of-the-Art in Scientific Computing, Copenhagen, Denmark, June 2004*) Rajesh Nishtala, Richard Vuduc, James W. Demmel, Katherine A. Yelick

**Poster on Automatic Tuning Of Collective Communications in MPI** (*SIAM Conference on Parallel Processing for Scientific Computing (PP04), San Francisco, USA, February 2004*) Rajesh Nishtala, Neil Patel, Kushal Chakrabarti, Kaushal Sanghavi, Advisors: Katherine A. Yelick, James W. Demmel, Eric Brewer

**Performance Modeling and Analysis of Cache Blocking in Sparse Matrix Vector Multiply** (*UCB Tech Report UCB/CSD-04-1335, June 2004*) Rajesh Nishtala, Richard Vuduc, James W. Demmel, Katherine A. Yelick

**Performance Optimizations and Bounds for Sparse Matrix-Vector Multiply** (*Proceedings of the IEEE/ACM Conference on Supercomputing, 2002*.) Richard Vuduc, James W. Demmel, Katherine A. Yelick, Shoaib Kamil, Rajesh Nishtala, Benjamin Lee.

**Automatic Performance Tuning and Analysis of Sparse Triangular Solve** (*ICS 2002: Workshop on Performance Optimization via High-Level Languages and Libraries*.) Richard Vuduc, Shoaib Kamil, Jen Hsu,

**Computer  
Science  
Projects**

**CS252 Graduate Computer Architecture:** Aggregation Query Under Uncertainty in Sensor Networks  
**CS262a Advanced Topics in Computer Systems:** Automatic performance optimization of collective communications operations in MPI  
**CS262b Advanced Topics in Computer Systems:** Firehose: An Algorithm for Distributed Page Registration on Clusters of SMPs  
**CS263 Programming Languages:** An analysis of various Matlab compilation techniques  
**CS267 Applications of Parallel Computers:** An implementation of Parallel Sparse Triangular Solve and the NAS FT Benchmark in UPC  
**CS281a Statistical Learning Techniques:** A comparison of various statistical classification techniques to understand when to apply specific performance optimizations in linear algebra operations

**Haas School  
of Business  
Projects**

**MBA 290 Opportunity Recognition:** Market Survey of High Performance Computing  
**MBA 294 Marketing for High Tech Entrepreneurs:** Consulting project for Panasonic on when to outsource research and development  
**MBA 290.T.2 Strategic Planning during Technology Revolutions:** Future Strategic Opportunities for AT&T

**Honor  
Societies**

Member Eta Kappa Nu (EECS Honor Society) (since October 2000)  
Member Tau Beta Pi (Engineering Honor Society) (since October 2000)

**Leadership  
Experience**

5/02 – 5/03 Indus, UC Berkeley

Berkeley, CA

**Vice President of Indus**

Indus is the largest South Asian student group at UC Berkeley with over 500 members. My job as vice president was to lead the organization in all of the events and coordinate with the members as well as other members of the executive board to ensure that the events ran smoothly. Events ranged from local volunteer activities, cultural awareness weeks, social events, intercollegiate dance competitions, obtaining funding from the university, and three large theatrical shows with audiences of over 2000 in each. In this role I also represented the views of our community to university officials.

5/01 – 5/02 Indus, UC Berkeley

Berkeley, CA

**Technical Director for Indus**

In this capacity I was responsible for the flawless running of our theatrical productions by coordinating with the theater technical crew acting as a liaison between the club and the venue. In addition to helping plan and run all the events I maintained the website as well.

**Professional  
Experience**

5/01 – 8/01 Nexsi Corporation

Milpitas, CA

**Summer Intern**

Redesigned a graphical Simulation tool, using the C++ and the Gtk Libraries, for the design and verification group that is used to debug their design at any given time in the simulation of their network processor.

6/00-8/00 Ciena Corporation

Cupertino, CA

**Summer Intern**

Automated testing for setting up a network for large network stress testing of the Ciena CoreDirector switch using Tcl.

6/99-8/99 Ciena Corporation

Cupertino, CA

**Summer Intern**

Tested Network Planning Software, Automated Testing of Sonet Test Bed, Automated Testing of Network Planning Software, Wrote a number of Test Procedures

**Other  
Activities**

Play South Indian Classical Drums and South Indian Classical Flute

**References**

On request.