University of California at Berkeley
Department of Electrical Engineering and Computer Sciences

EE-247 : Analog-Digital Interface IC

Term Project – Flash ADC

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Content

7-bit Flash ADC Design

I. Specification:

Technology: 0.13µm

Type: flash ADC

Supply voltage: 1.2V

Number of bits: 7 (simulated only for the bottom 4-bits)

+ 1LSB=8mV, target your design for 0.5LSB accuracy

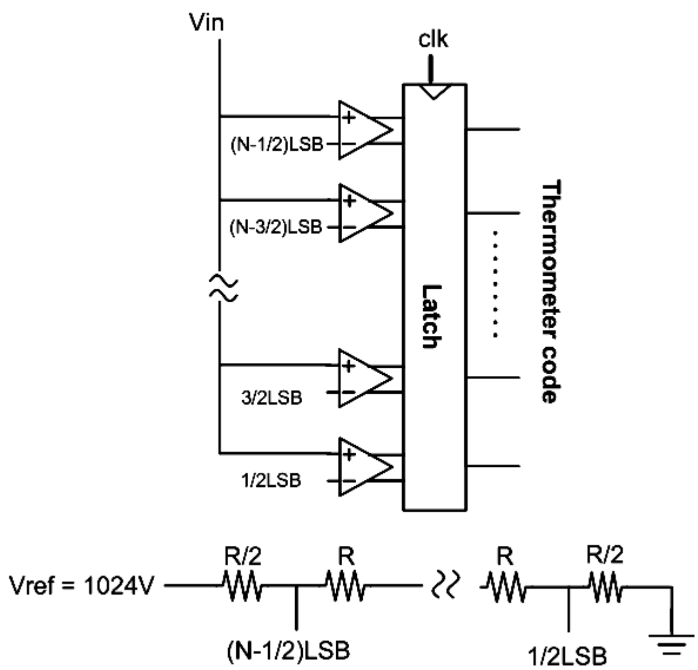
Comparator:

- The latch only portion: 3sigma offset of 50mV.

Device matching δ_{offset} = 5mV/sqrt(WxL)

Length: L = 0.2µm

Sampling rate: fs = 400MHz.



II. Hand Calculation and Device Analysis

1. Hand calculation

Start from the requirement of comparator input-referred offset:

$$3\delta_{offset} < 0.5LSB = 4mV$$

We have relation of pre-amp's offset, gain with latch's offset, as below:

$$3\sqrt{\delta_{pre-amp}^2 + \frac{\delta_{latch}^2}{G^2}} < 0.5LSB = 4mV$$

where $\delta_{pre-amp}$ is the offset voltage of the pre-amplifier, δ_{latch} is the offset voltage of the latch and G is the pre-amplifier's gain.

$$\rightarrow \ \delta_{pre-amp}^2 + \frac{\delta_{latch}^2}{G^2} < \frac{16}{9}(mV^2) \ (*)$$

For the latch : $3\delta_{latch} = 50mV$ → $\delta_{latch} \approx 16.667mV$

While from (*),

$$\frac{\delta_{latch}}{G} < \frac{4}{3}(mV)$$

$$\rightarrow \ G > \frac{3\delta_{latch}}{4} = \frac{17 \times 3}{4} \approx 12$$

To reduce the size of input pairs of the pre-amp, big G is desirable. However, it may not be good for fast response. Choose G = 16.

From (*), we have

$$\delta_{pre-amp}^2 < \frac{16}{9} - \frac{\delta_{latch}^2}{G^2} = \frac{16}{9} - \frac{16.667^2}{16^2} = 0.6488$$

$$\rightarrow \ \delta_{pre-amp} < 0.81mV$$

With equation given for the pre-amp offset δ_{offset} = 5mV/sqrt(WxL), we have the input device size: (WxL) = 38

Choose L to be minimum size: L = 0.2um → W = 192.6um → choose W=200um

→ Input device size:

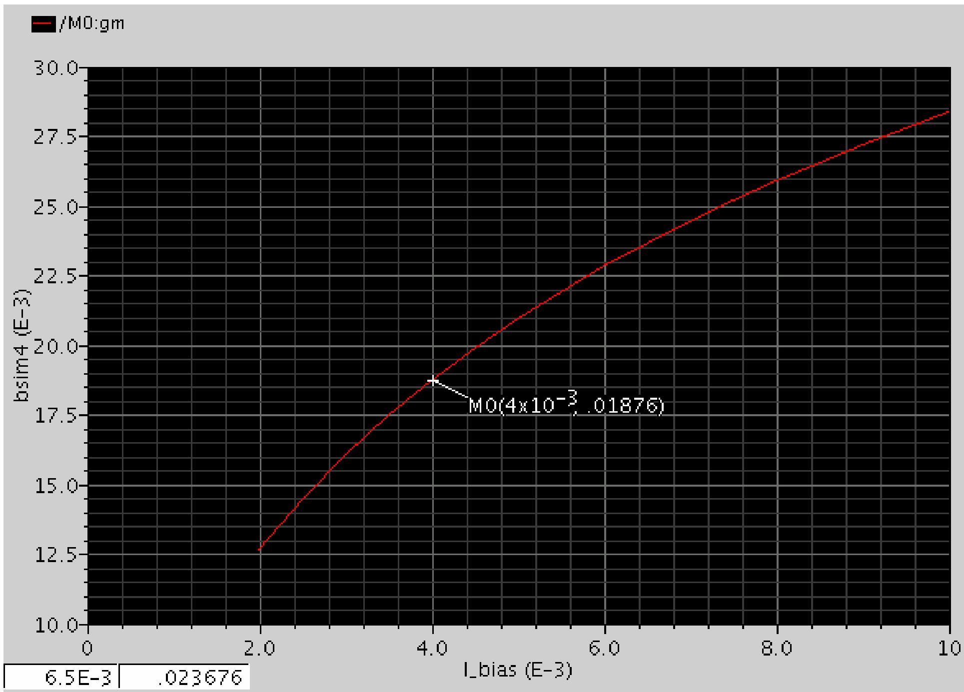
L = 0.2um

W=200um

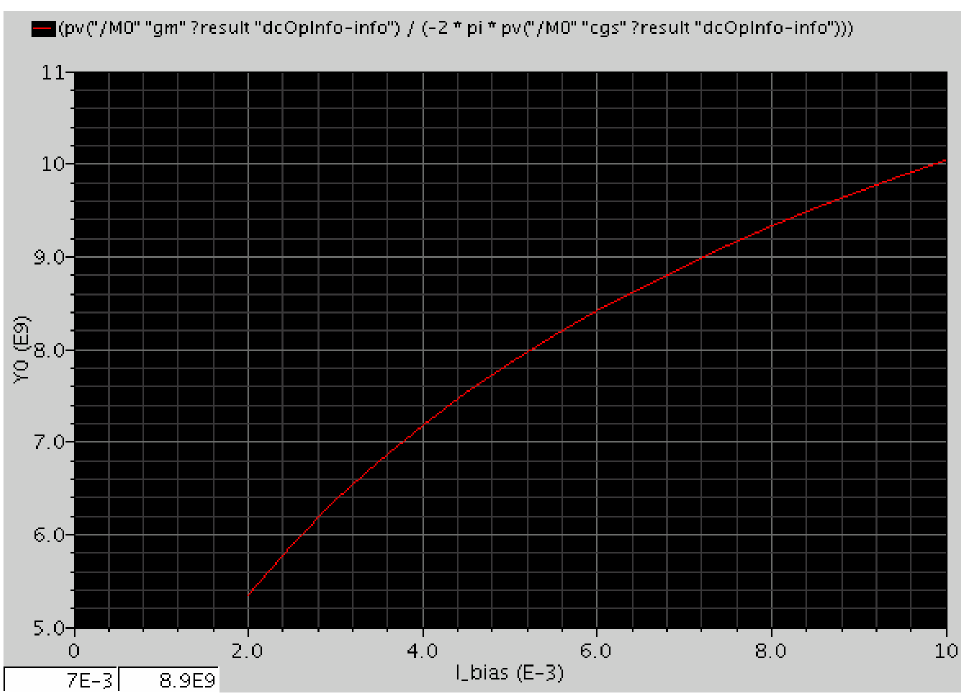
2. Input device analysis with Spectre:

Size: L = 0.2um → W = 200um

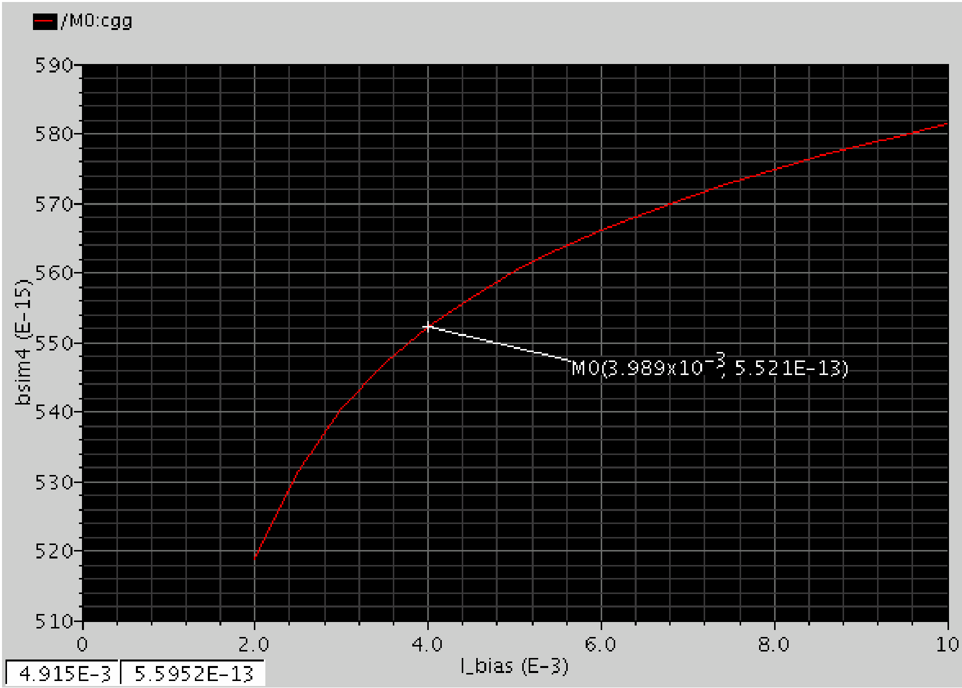
Transconductance Gm



f_T



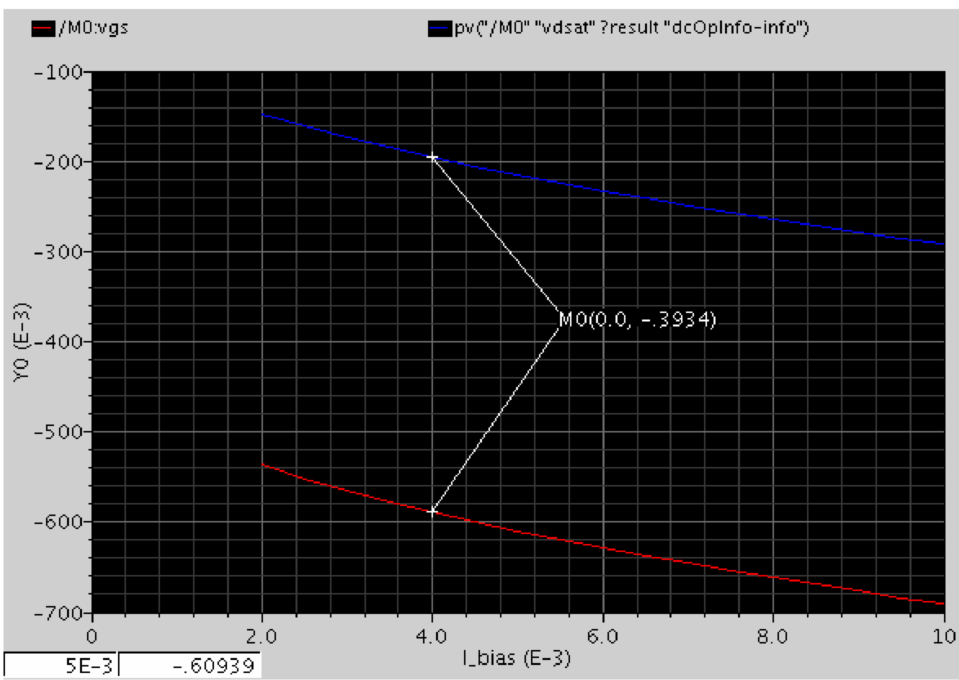
Input cap Cgg:



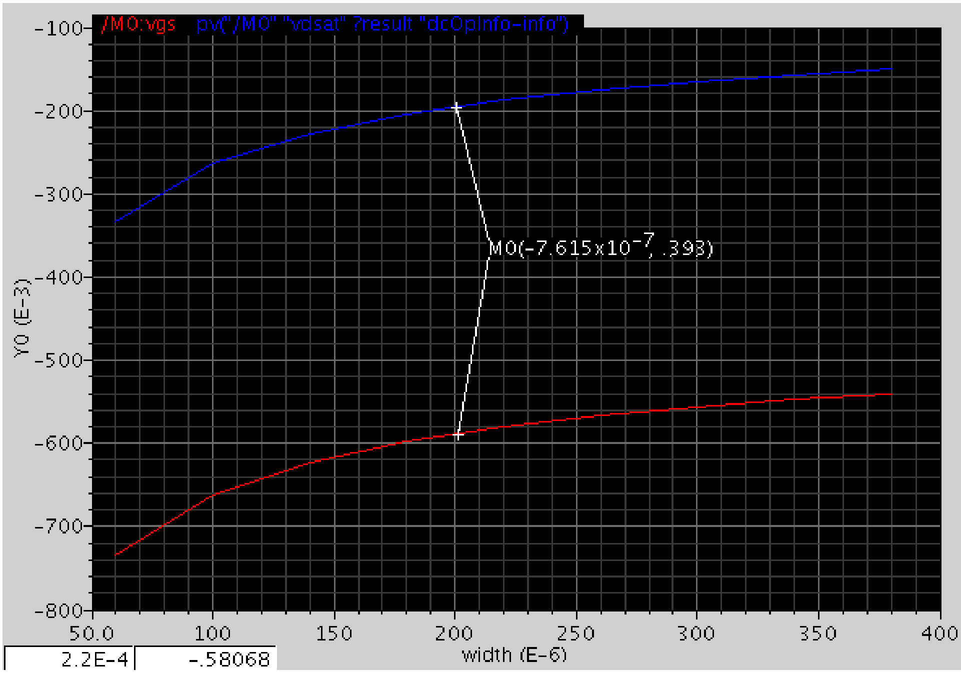
Choose bias current of one side: 2mA → pair bias: I_bias = 4 mA

→ gm = 18.7mA/V

Vgs, Vdsat v.s. bias current



Vgs, Vdsat v.s. size for 2mA bias



V_R < Vgs-Vdsat = 0.393V

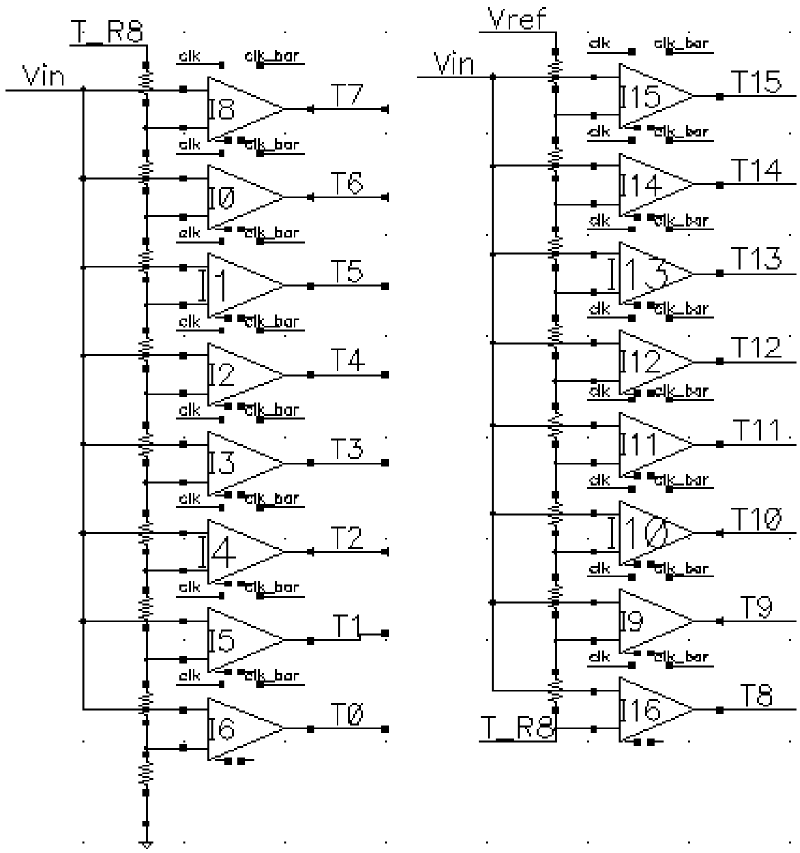
Comment: Notice that with the 4mA bias current, reducing transistor size will result in big Vgs. That is not desirable since pMOS input pair will be use for half of the comparators of 7 bits, where input reference voltage can be up to 512mV. Although an ideal current source is used to bias the pre-amp, a proper voltage room should remain over that current source, even at worst case.

With this consideration in mind, we see that increase of current will also lead to increase of size or vice versa, which are not appealing to us.

This is also one of the reasons that make our choice of size and bias current as stated.

III. Circuit Schematic

1. 4-bit thermometer code circuit



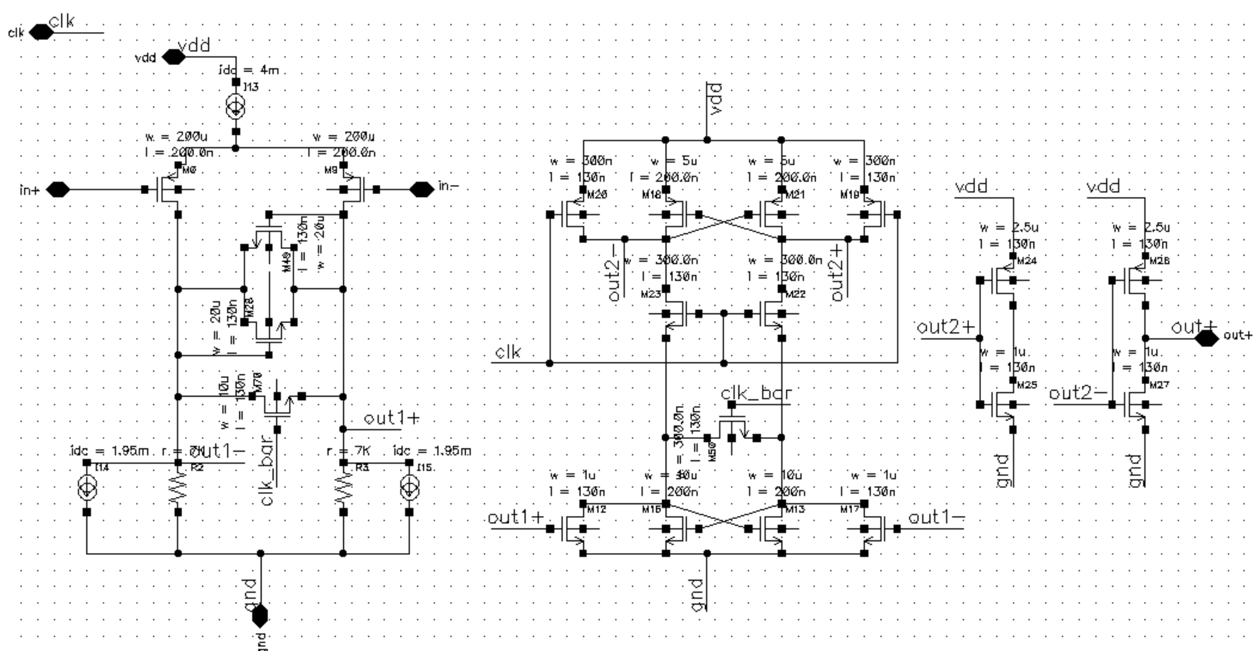
2. Comparator with sizing

A comparator is a modified version of that proposed by Yukawa, also mentioned in the lecture 21 of EE-247.

In this comparator we propose two additional reset switches at output of the pre-amp and at the latch. The reset is activated every cycle to improve the comparator performance, especially when the ADC experience overload.

As seen above in the device analysis, we need V_R < Vgs-Vdsat = 0.393V, with R = 7K → I_R < 0.056 mA. Say I_R = 50uA, the bias current at the low side must be 1.95mA

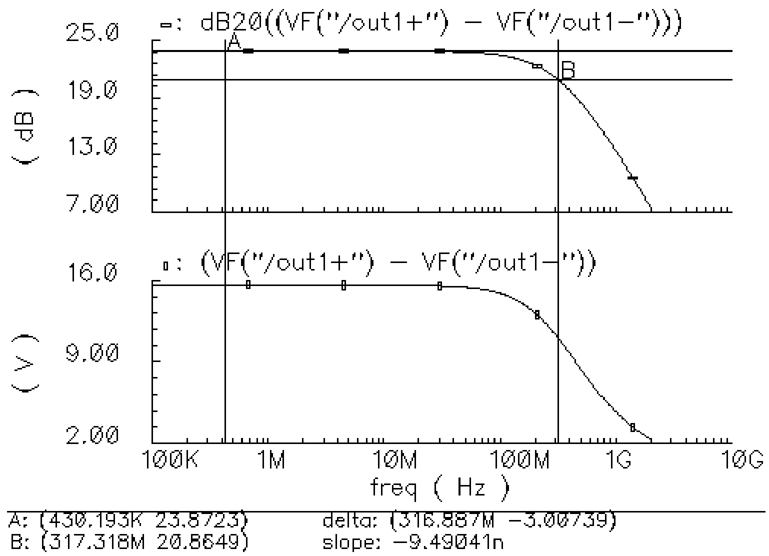
With 4mA bias current and device size of 200um x 0.2um, Vgs of input pairs is 580mV, which is reasonable. The comparator circuit with sizing is shown below.



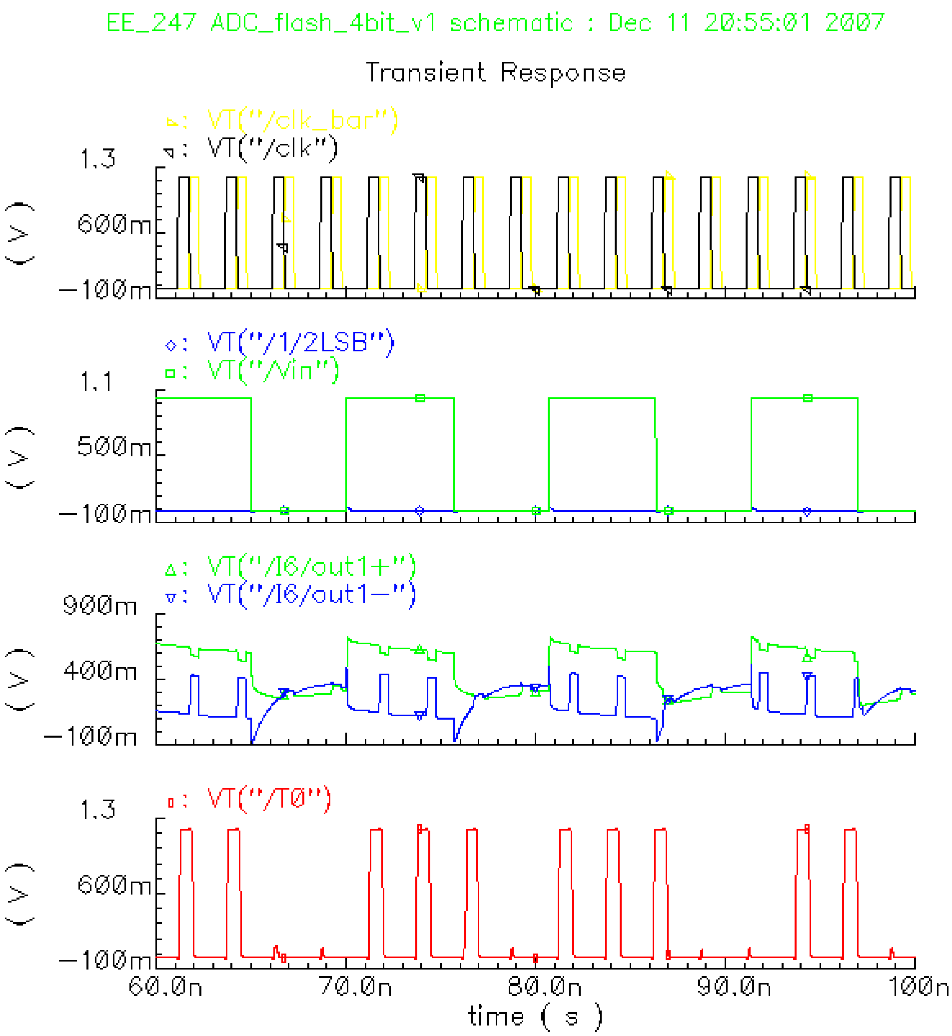
IV. Simulation Result:

1. Comparator performance

a. Pre-amp's gain



b. Overload recovery simulation with full 7-bit worst case signal



c. Worst case transient

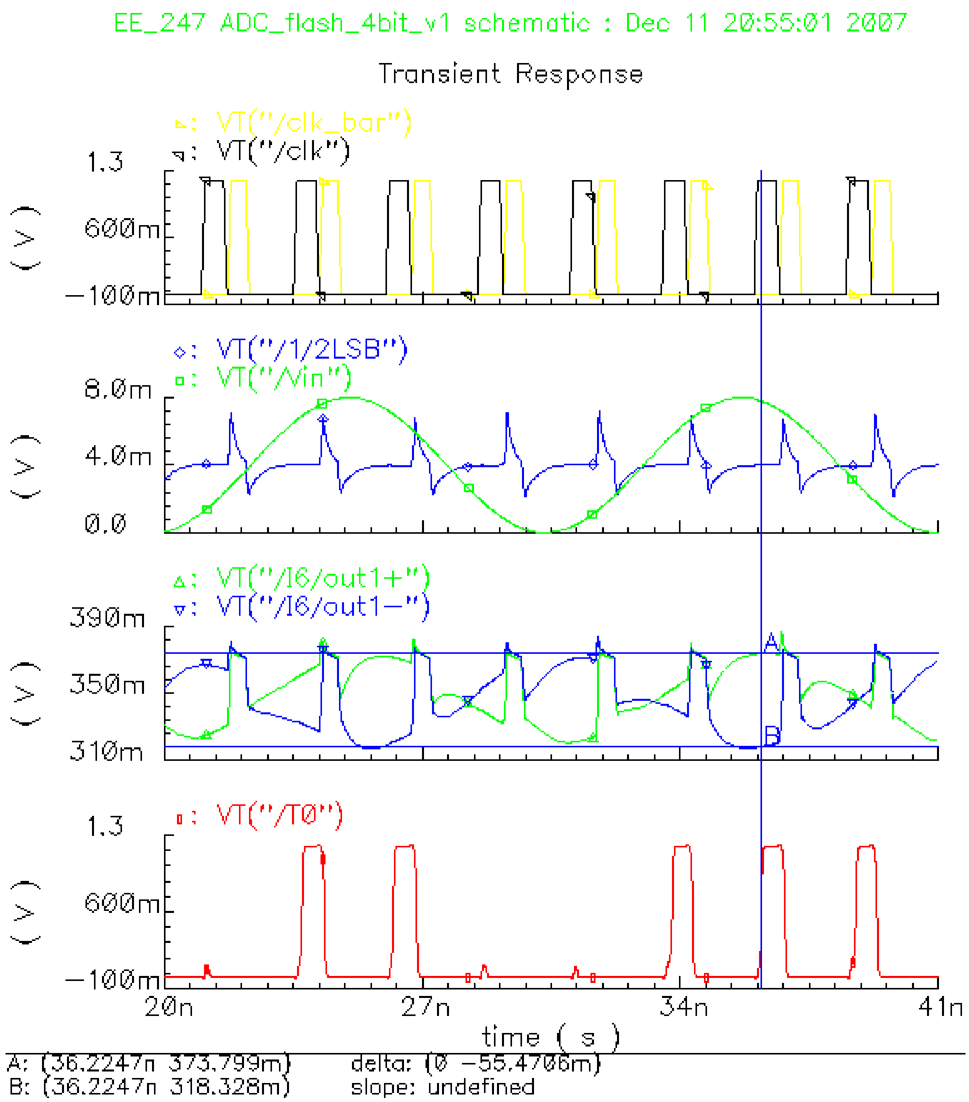
Transient simulation with worst case at the LSB comparator

Vin = 8mVp-p

fin = 100MHz

The simulation is done with the presence of 15 other comparators (4 bits) to check comparator's performance when working in the system, with consideration of kick-back effect…

The comparator functionality is verified in simulation shown below.



b. 4-bit ADC performance with FFT in Matlab.

The simulation is set up with full-scale 4-bit thermometer code ADC simulation. The output data of transient simulation is processed by Matlab and performed FFT to see the converter's performance.

Incoming signal:

Frequency: fin = 15*fs/64 = 93.75MHz

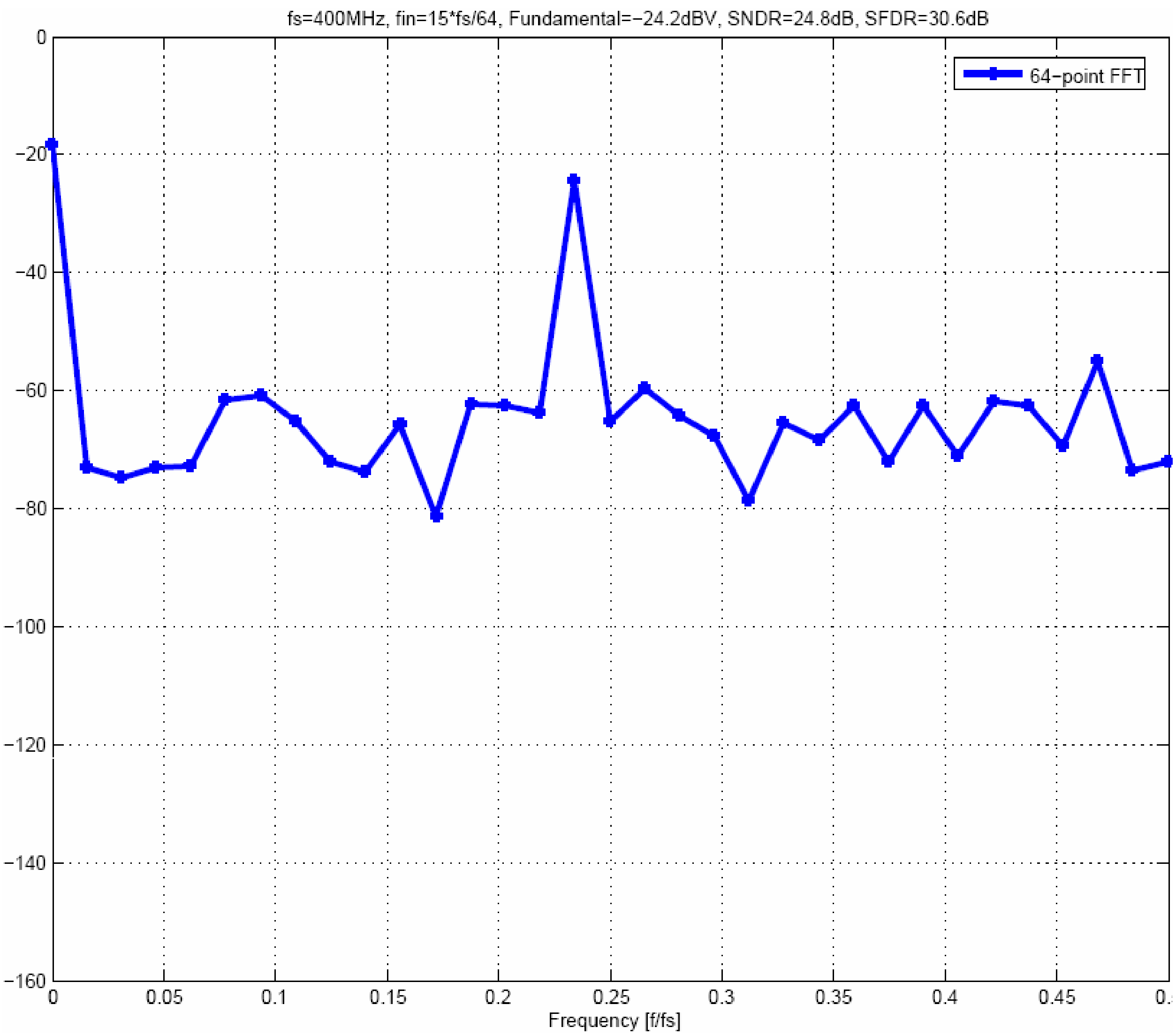
Sinusoidal 128mVp-p

Sampling rate: fs = 400MHz.

FFT 1

50Ω source impedance : NO

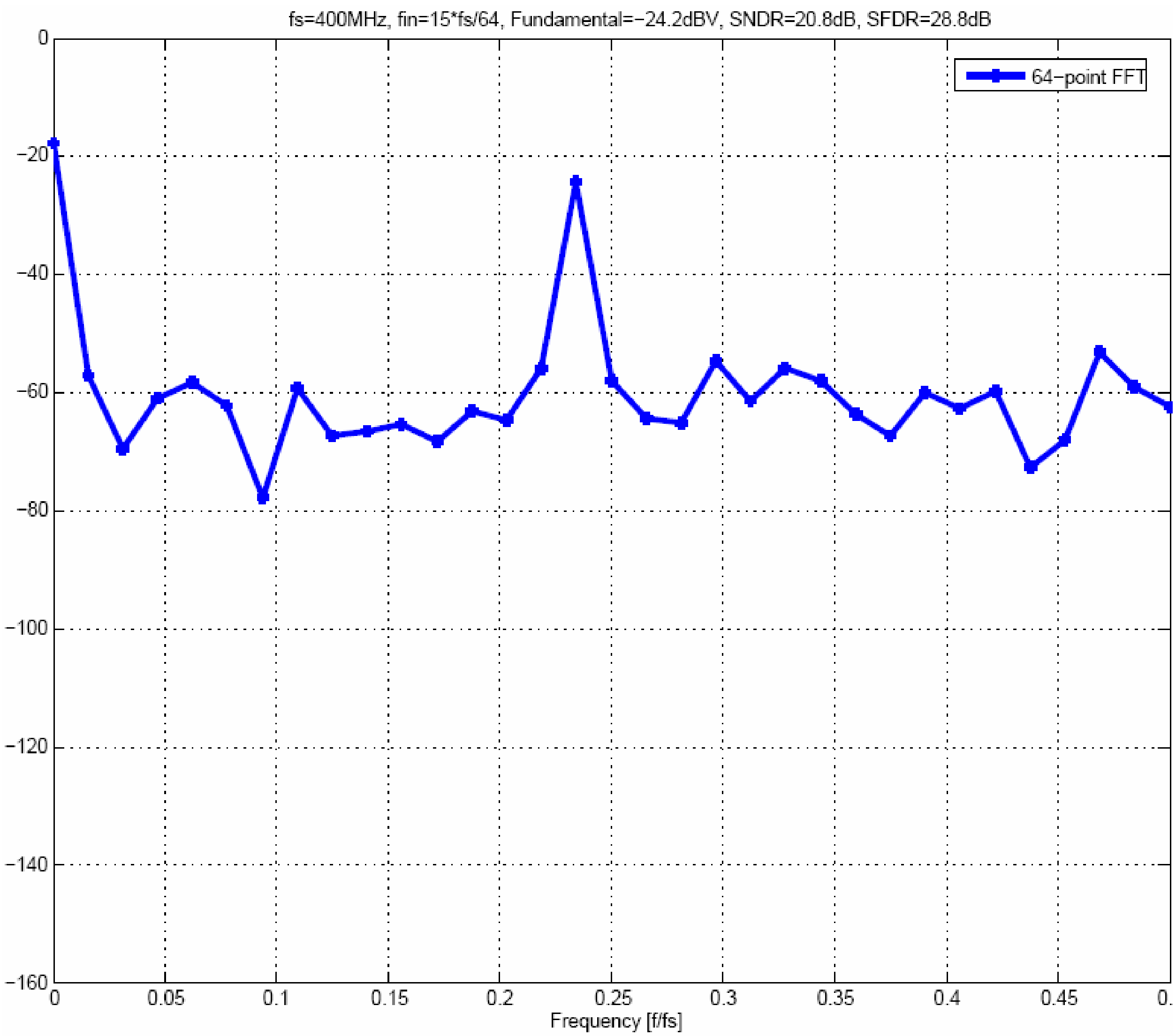
Offset at pre-amps and latches : NO



FFT 2

50Ω source impedance : NO

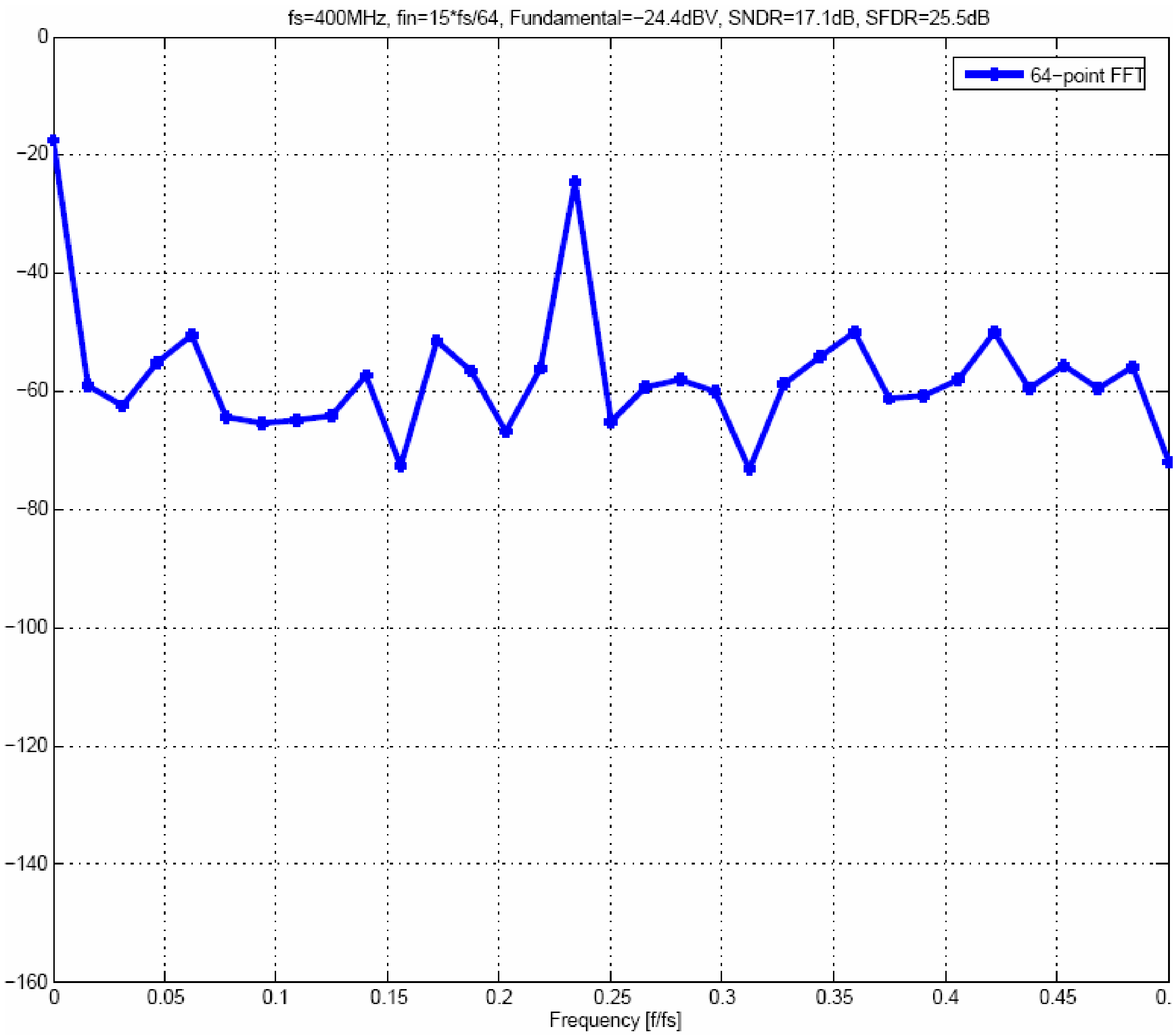
Offset at pre-amps and latches : YES, 2.8sigma added to 4 of the pre-amps and latches



FFT 3

50Ω source impedance : NO

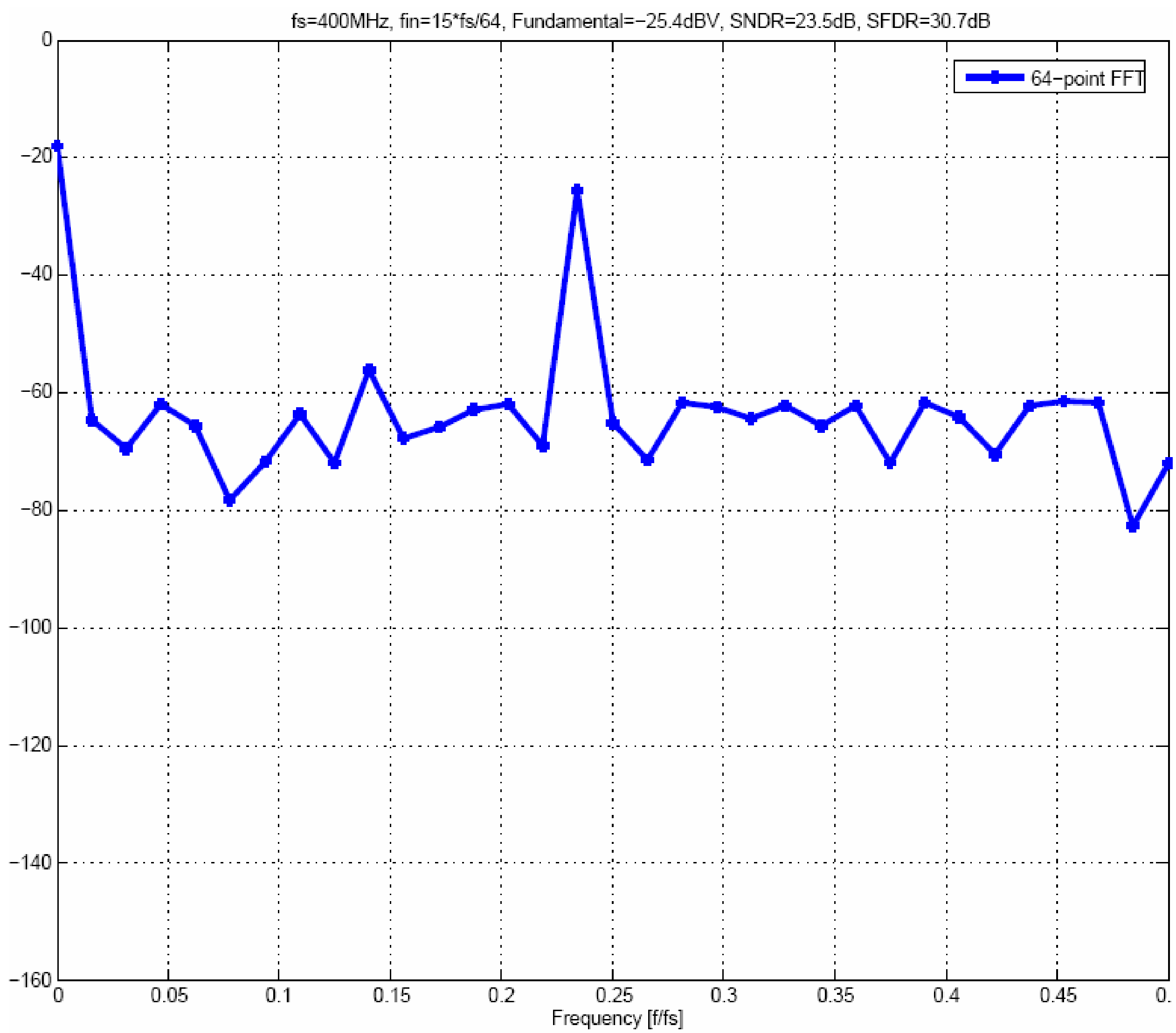
Offset at pre-amps and latches : YES, 5sigma added to 4 of the pre-amps and latches



FFT 4

50Ω source impedance : YES

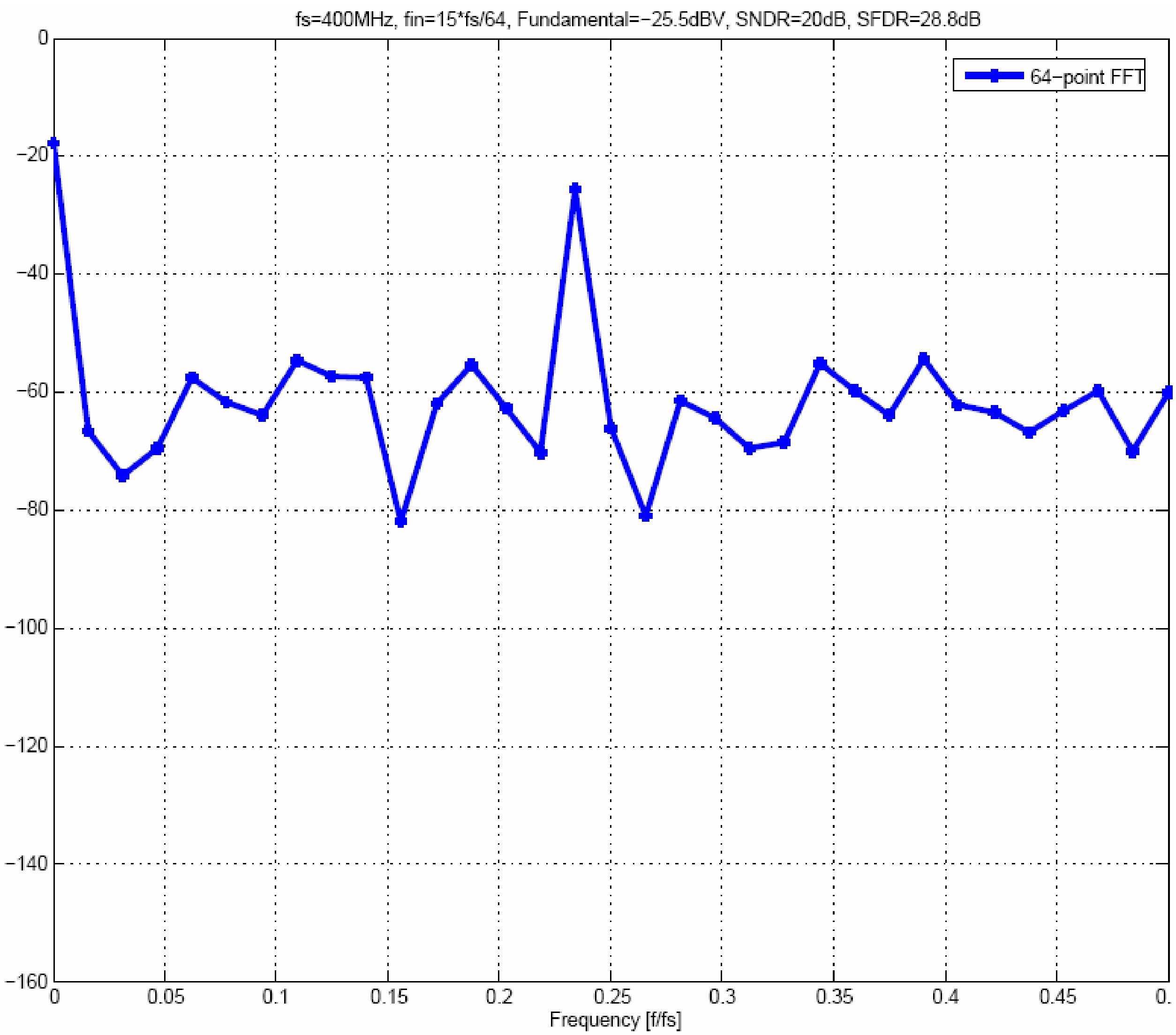
Offset at pre-amps and latches : NO



FFT 5

50Ω source impedance : YES

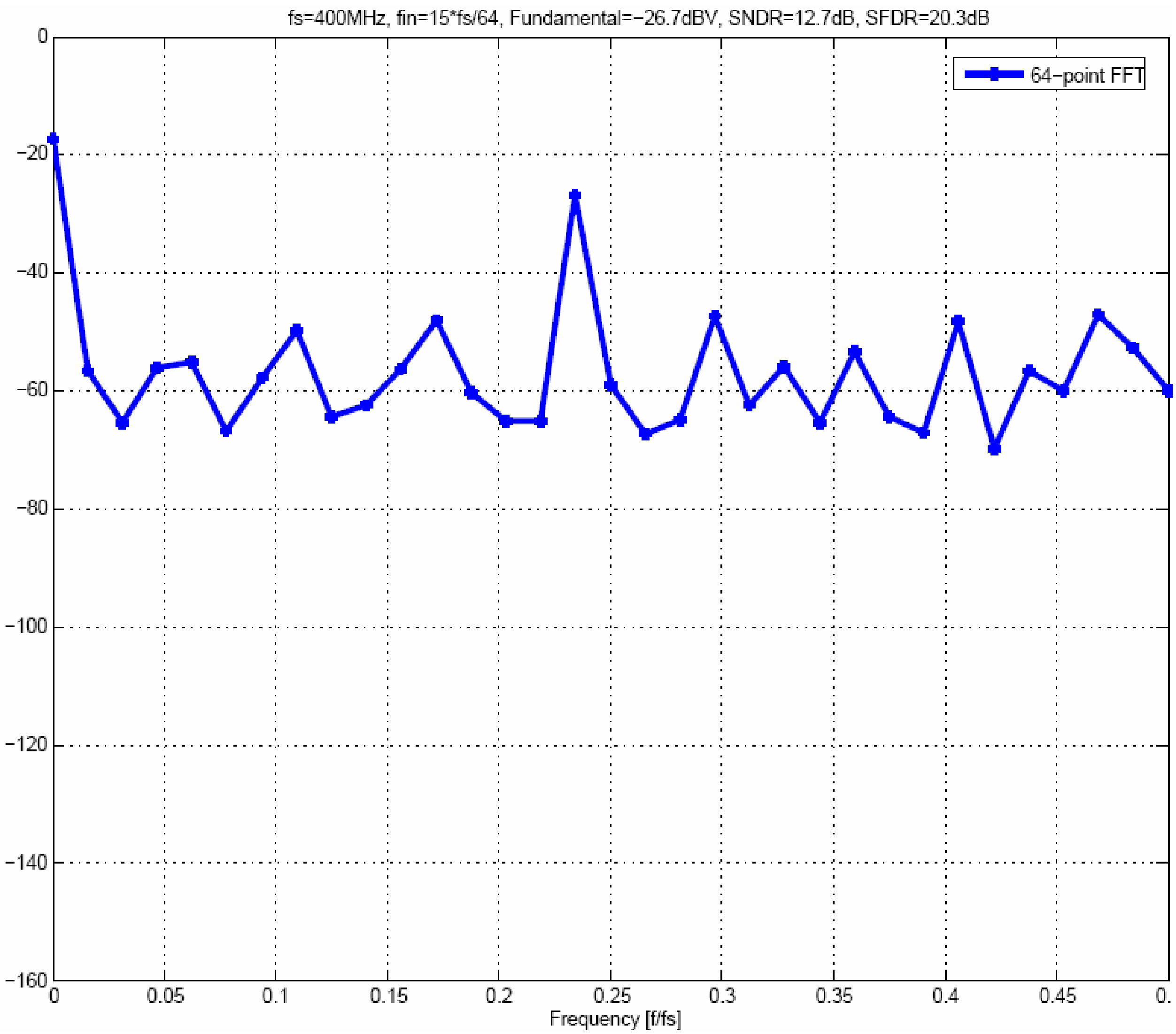
Offset at pre-amps and latches : YES, 2.8sigma added to 4 of the pre-amps and latches



FFT 6

50Ω source impedance : YES

Offset at pre-amps and latches : YES, 5sigma added to 4 of the pre-amps and latches



V. Power Consumption

a. From hand calculation analysis, since we use only 4mA bias current of the pre-amp and consider that the total current dissipated by the latches digital circuits is relatively small. We have the total current is:

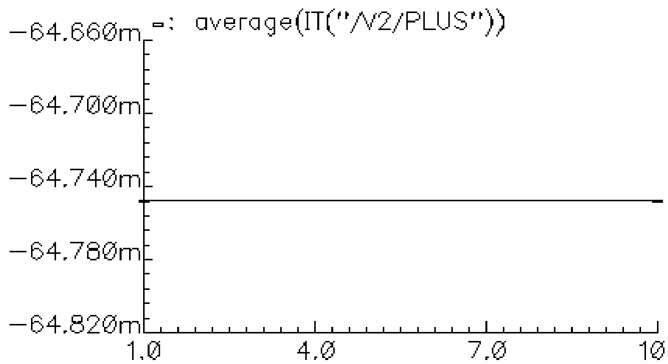
$$4 \times 128 = 512 \text{ (mA)}$$

Therefore, the power consumption is

$$P = V.I = 1.2 \times 512mA = 614.4mW$$

b. From simulation result, with consideration of all current used by digital circuit and resister string, we have:

Average current dissipated by 16 comparators (4 bits), including pre-amps and latches is 64.75mA



So, the total current consumed by 128 comparators (7 bits) is 64.75mA x 8 = 518mA

The current consumed by the resistor string is 0.8mA

→ the total current dissipation

$$518 + 0.8 = 518.8 \text{ (mA)}$$

Power dissipation for 7-bit ADC:

$$P = V.I = 1.2 \times 518.8mA = 622.56mW$$

VI. Summary

Input device size:

L = 0.2 um

W = 200 um

Pre-amp gain = 15.618 = 23.9dB

Worst case input-referred offset:

$$3\delta = 3\sqrt{\delta_{pre-amp}^2 + \frac{\delta_{latch}^2}{G^2}} = 3\sqrt{(0.79mV)^2 + \frac{(16.667mV)^2}{15.618^2}} = 3.98mV$$

→ $3\delta < 4mV$ → meet offset specification.

Overload recovery : verified

FFT results

fs = 400MHz

fin = 93.75MHz

Source impedance 50Ω	Offset	Fundamental (dB)	SNDR (dB)	SFDR (dB)
No	No	-24.2	24.8	30.6
No	2.8sigma	-24.2	20.8	28.8
No	5sigma	-24.4	17.1	25.5
Yes	No	-25.4	23.5	30.7
Yes	2.8sigma	-25.5	20	28.8
Yes	5sigma	-26.7	12.7	20.3

Power dissipation for 7-bit ADC: 622.56mW

VII. Conclusion

In this term project, a design of 7-bit flash ADC is studied and design with 0.13um technology. A comparator similar to Yukawa's with additional 2 reset switches is used. It has a 3sigma offset of 3.98mV. Simulations with 4 bits show that the ADC can achieve 23.5 SNDR with 50 Ω source impedance.

We have learnt a lot from this project with practical work for ADC design.

Appendix I – Matlab code

```
clear;

% Parameters: 1.2V supply, 128mV reference, 400MHz sampling freq,
%             64-point fft
vdd=1.2;
Vref=0.128;
N=64;
fs=400;
fin=15/64*fs;


% load hspice output
m = loadsig('power_0sig_0.tr0')

% list available signals
lssig(m);

% Read related signals(time, t0~t15) into matlab variables
t=evalsig(m, 'TIME');
for i=0:1:15
y=['t',int2str(i)];
output(:,i+1)=evalsig(m,y);
end

% Detect clock falling edge for signal reconstruction
clk_raw=evalsig(m, 'clk');
clk=sign(clk_raw-vdd/2);
f_edge=find(diff(clk)==-2);

% Signal reconstruction
for i=1:1:N+1
out_sample(i,:)=output(f_edge(i),:);
end
out_binary=(sign(out_sample-vdd/2)+1)/2;
out_binary_t=transpose(out_binary)

% Error Correction
code_error=diff(out_binary_t,1,1);
[R,C]=find(code_error==1)
out_binary_t(R,C)=1;
out=sum(out_binary_t);

% Thermometer to Binary
vod1=(out/16)*Vref;
vod=transpose(vod1);
%plot(1:65,vod)


% if first and last point don't match within good precison, the fft data is
garbage...
delta = vod(1)-vod(end)
if abs(delta)>1e-6
    disp('This looks like inaccurate fft data...');
    beep
```

```
end

% fft analysis
spectrum = abs(fft(vod(2:end)));
spectrum = 2/N*spectrum(1:N/2+1);
spectrumdb = 20*log10(spectrum+eps);
frequency = 1/N * (0:length(spectrumdb)-1);

% Calculate fundamental level and index
[fund, fundidx] = max(spectrum);

% If DC level larger than fundamental, ignore DC
if fundidx==1
    spectrum(1)=0;
end

[fund, fundidx] = max(spectrum);
funddb=20*log10(fund);

% Calculate the spur level and index
spec_nodc_nofund = [spectrum(2:fundidx-1); spectrum(fundidx+1:end)];
[spur, spuridx] = max (spec_nodc_nofund);

% Calculate SFDR and SNDR
sfdrdb = funddb-20*log10(spur);
sndr = norm(fund)/norm(spec_nodc_nofund);
sndrdb=20*log10(sndr);

figure(1);
plot(frequency, spectrumdb, '-*', 'linewidth', 3);
string = sprintf('fs=%0.3gMHz, fin=15*fs/64, Fundamental=%0.3gdBV,
SNDR=%0.3gdB, SFDR=%0.3gdB', fs, funddb, sndrdb, sfdrdb);
title(string);
xlabel('Frequency [f/fs]');
ylabel('Amplitude [dBV]');
string2 = sprintf('%0.3g-point FFT',N);
legend(string2);
axis([0 0.5 -160 0]);

%hold off;
grid;
```

Appendix II – Hspice code

```
* # FILE NAME: /USERS/PHUCLE/SIMULATION/ADC_FLASH_4BIT_V1/HSPICES/SCHEMATIC/
* NETLIST/ADC_FLASH_4BIT_V1.C.RAW
* NETLIST OUTPUT FOR HSPICES.
* GENERATED ON DEC 11 03:16:22 2007

* FILE NAME: EE_247_ADC_FLASH_4BIT_V1_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: ADC_FLASH_4BIT_V1.
* GENERATED FOR: HSPICES.
* GENERATED ON DEC 11 03:16:23 2007.

XI13 CLK CLK_BAR GND VIN NET040 T13 VDD SUB1
XI10 CLK CLK_BAR GND VIN NET065 T10 VDD SUB1
XI4 CLK CLK_BAR GND VIN NET8 T2 VDD SUB1
XI1 CLK CLK_BAR GND VIN NET17 T5 VDD SUB1
V6 CLK_BAR GND  PULSE 0.0 1.2 +1.70000000E-09 100E-12 100E-12 400E-12 2.5E-9
V1 CLK GND  PULSE 0.0 1.2 +1.10000000E-09 100E-12 100E-12 500E-12 2.5E-9
V0 NET094 0  AC 0.0 PULSE 1.024 0.0 1E-9 10E-12 10E-12 5E-9 10.6666E-9
V2 VDD GND  1.2
V8 VREF GND  +1.28000000E-01
V4 VIN_ORIGINAL GND  SIN +6.40000000E-02 +6.40000000E-02 93.75E6 1E-9
R67 VIN VIN  50.0
R68 NET094 0  1E3
R16 NET069 T_R8  10.0
R15 NET065 NET069  10.0
R14 NET036 NET034  10.0
R13 NET034 NET065  10.0
R12 NET040 NET036  10.0
R11 NET038 NET040  10.0
R10 NET042 NET038  10.0
R9 VREF NET042  5.0
R8 T_R8 NET08  10.0
R17 VIN VIN_ORIGINAL  1E-6
RV3 GND 0  1E-6
R7 NET08 NET20  10.0
R6 NET20 NET17  10.0
R5 NET17 NET14  10.0
R4 NET11 NET8  10.0
R3 NET14 NET11  10.0
R2 NET8 NET5  10.0
R1 NET5 NET2  10.0
R0 NET2 0  5.0
XI16 CLK CLK_BAR GND VIN T_R8 T8 VDD COMPARATOR_G1
XI15 CLK CLK_BAR GND VIN NET042 T15 VDD COMPARATOR_G1
XI14 CLK CLK_BAR GND VIN NET038 T14 VDD COMPARATOR_G1
XI12 CLK CLK_BAR GND VIN NET036 T12 VDD COMPARATOR_G1
XI11 CLK CLK_BAR GND VIN NET034 T11 VDD COMPARATOR_G1
XI9 CLK CLK_BAR GND VIN NET069 T9 VDD COMPARATOR_G1
XI8 CLK CLK_BAR GND VIN NET08 T7 VDD COMPARATOR_G1
XI6 CLK CLK_BAR GND VIN NET2 T0 VDD COMPARATOR_G1
XI5 CLK CLK_BAR GND VIN NET5 T1 VDD COMPARATOR_G1
XI3 CLK CLK_BAR GND VIN NET11 T3 VDD COMPARATOR_G1
XI2 CLK CLK_BAR GND VIN NET14 T4 VDD COMPARATOR_G1
XI0 CLK CLK_BAR GND VIN NET20 T6 VDD COMPARATOR_G1
```

```
* FILE NAME: EE_247_COMPARATOR_W_OFFSET_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: COMPARATOR_W_OFFSET.
* GENERATED FOR: HSPICES.
* GENERATED ON DEC 11 03:16:22 2007.

* TERMINAL MAPPING: CLK = CLK
*                    CLK_BAR = CLK_BAR
*                    GND = GND
*                    IN+ = 1
*                    IN- = 4
*                    OUT+ = 3
*                    VDD = VDD
.SUBCKT SUB1 CLK CLK_BAR GND 1 4 3 VDD
V0 NET049 1  +0.79000000E-03
V1 NET047 2  +1.66670000E-02
M50 NET95 CLK_BAR NET89 GND  NFET  L=130E-9 W=300E-9
M12 NET95 NET047 GND GND  NFET  L=130E-9 W=1E-6
M16 NET95 NET89 GND GND  NFET  L=200E-9 W=10E-6
M70 6 CLK_BAR 2 GND  NFET  L=130E-9 W=10E-6
M17 NET89 6 GND GND  NFET  L=130E-9 W=1E-6
M22 5 CLK NET89 GND  NFET  L=130E-9 W=300E-9
M23 7 CLK NET95 GND  NFET  L=130E-9 W=300E-9
M49 2 2 6 GND  NFET  L=130E-9 W=20E-6
M28 6 6 2 GND  NFET  L=130E-9 W=20E-6
M27 3 7 GND GND  NFET  L=130E-9 W=1E-6
M25 NET59 5 GND GND  NFET  L=130E-9 W=1E-6
M13 NET89 NET95 GND GND  NFET  L=200E-9 W=10E-6
M21 5 7 VDD VDD  PFET  L=200E-9 W=5E-6
M0 6 NET049 NET124 VDD  PFET  L=200E-9 W=200E-6
M20 7 CLK VDD VDD  PFET  L=130E-9 W=300E-9
M24 NET59 5 VDD VDD  PFET  L=130E-9 W=2.5E-6
M9 2 4 NET124 VDD  PFET  L=200E-9 W=200E-6
M18 7 5 VDD VDD  PFET  L=200E-9 W=5E-6
M19 5 CLK VDD VDD  PFET  L=130E-9 W=300E-9
M26 3 7 VDD VDD  PFET  L=130E-9 W=2.5E-6
I15 2 GND  DC=1.95E-3
I14 6 GND  DC=1.95E-3
I13 VDD NET124  DC=4E-3
R3 2 GND  7E3
R2 6 GND  7E3



* END OF SUBCIRCUIT DEFINITION.
.ENDS SUB1
* FILE NAME: EE_247_COMPARATOR_SCHEMATIC.S.
* SUBCIRCUIT FOR CELL: COMPARATOR.
* GENERATED FOR: HSPICES.
* GENERATED ON DEC 11 03:16:22 2007.

* TERMINAL MAPPING: CLK = CLK
*                    CLK_BAR = CLK_BAR
*                    GND = GND
*                    IN+ = 7
```

```
*                    IN- = 5
*                    OUT+ = 3
*                    VDD = VDD
.SUBCKT COMPARATOR_G1 CLK CLK_BAR GND 7 5 3 VDD
M50 NET95 CLK_BAR NET89 GND  NFET  L=130E-9 W=300E-9
M12 NET95 6 GND GND  NFET  L=130E-9 W=1E-6
M16 NET95 NET89 GND GND  NFET  L=200E-9 W=10E-6
M70 4 CLK_BAR 6 GND  NFET  L=130E-9 W=10E-6
M17 NET89 4 GND GND  NFET  L=130E-9 W=1E-6
M22 1 CLK NET89 GND  NFET  L=130E-9 W=300E-9
M23 2 CLK NET95 GND  NFET  L=130E-9 W=300E-9
M49 6 6 4 GND  NFET  L=130E-9 W=20E-6
M28 4 4 6 GND  NFET  L=130E-9 W=20E-6
M27 3 2 GND GND  NFET  L=130E-9 W=1E-6
M25 NET59 1 GND GND  NFET  L=130E-9 W=1E-6
M13 NET89 NET95 GND GND  NFET  L=200E-9 W=10E-6
M21 1 2 VDD VDD  PFET  L=200E-9 W=5E-6
M0 4 7 NET124 VDD  PFET  L=200E-9 W=200E-6
M20 2 CLK VDD VDD  PFET  L=130E-9 W=300E-9
M24 NET59 1 VDD VDD  PFET  L=130E-9 W=2.5E-6
M9 6 5 NET124 VDD  PFET  L=200E-9 W=200E-6
M18 2 1 VDD VDD  PFET  L=200E-9 W=5E-6
M19 1 CLK VDD VDD  PFET  L=130E-9 W=300E-9
M26 3 2 VDD VDD  PFET  L=130E-9 W=2.5E-6
I15 6 GND  DC=1.95E-3
I14 4 GND  DC=1.95E-3
I13 VDD NET124  DC=4E-3
R3 6 GND  7E3
R2 4 GND  7E3

* END OF SUBCIRCUIT DEFINITION.
.ENDS COMPARATOR_G1


* INCLUDE FILES


* END OF NETLIST
.TRAN  1.00000E-09 1.60000E-07 START=  0.0000
.TEMP    25.0000
.OP
.save
.OPTION  INGOLD=2 ARTIST=2 PSF=2
+        PROBE=0
.END
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