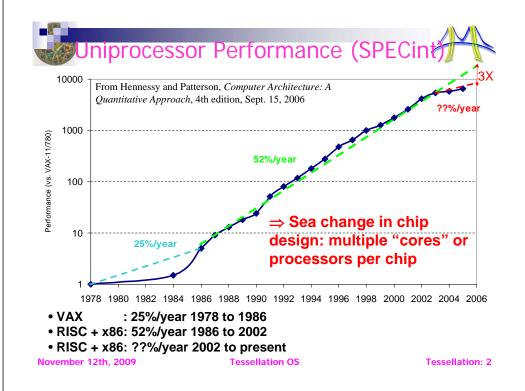
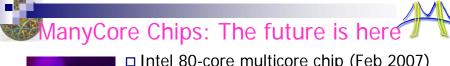
## **Tessellation OS**



### Architecting Systems Software in a ManyCore World

John Kubiatowicz UC Berkeley kubitron@cs.berkeley.edu







- Intel 80-core multicore chip (Feb 2007)
  80 simple cores
  Two floating point engines /core
  Mesh-like "network-on-a-chip"
  100 million transistors
  65nm feature size
- "ManyCore" refers to many processors/chip
  64? 128? Hard to say exact boundary
- □ How to program these?
  - $\Box$  Use 2 CPUs for video/audio
  - $\square$  Use 1 for word processor, 1 for browser
  - □ 76 for virus checking???
- □ Something new is clearly needed here...

#### November 12th, 2009





# Parallel Processing for the Masses

#### □ Why is the presence of ManyCore a problem?

- Parallel computing has been around for 40 years with mixed results
  - Many researchers, several generations, widely varying approaches
- Parallel computing has never become a generic software solution (especially for client applications)
- Suddenly, parallel computing will appear at all levels of our computation stack
  - Cellphones
  - Cars (yes, Bosch is thinking of replacing some of the 70 processors in a high end car with ManyCore chips)
  - Laptops, Desktops, Servers...
- □ Time for the computer industry to panic a bit???

Perhaps

# Why might we succeed this time?

- □ No Killer Microprocessor to Save Programmers (No Choice)
  - □ No one is building a faster serial microprocessor
  - $\hfill\square$  For programs to go faster, SW must use parallel HW
- □ New Metrics for Success (Different Criteria)
  - □ Perhaps linear speedup is not the primary goal
  - □ Real Time Latency/Responsiveness and/or MIPS/Joule
  - Just need some new killer parallel apps vs. all legacy SW must achieve linear speedup
- □ Necessity: All the Wood Behind One Arrow (More Manpower)
  - □ Whole industry committed, so more working on it
  - If future growth of IT depends on faster processing at same price (vs. lowering costs like NetBook)
- □ User-Interactive Applications Exhibit Parallelism (New Apps)
  - Multimedia, Speech Recognition, situational awareness
- Multicore Synergy with Cloud Computing (Different Focus)
  - Cloud Computing apps parallel even if client not parallel
  - Manycore is cost-reduction, not radical SW disruption

**Tessellation OS** 

Tessellation: 5

- Outline
- □ What is the problem (Did this already)
- Berkeley Parlab
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November 12th, 2009
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Tessellation OS

**Tessellation: 6** 



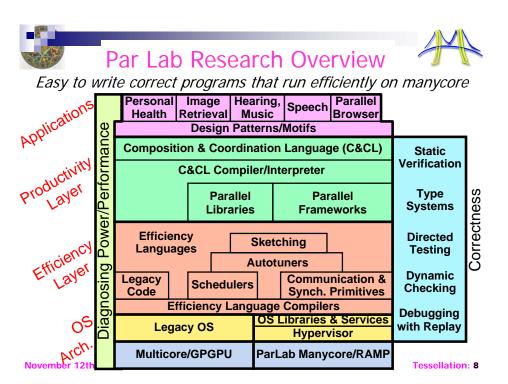
## ParLab: a Fresh Approach to Parallelish

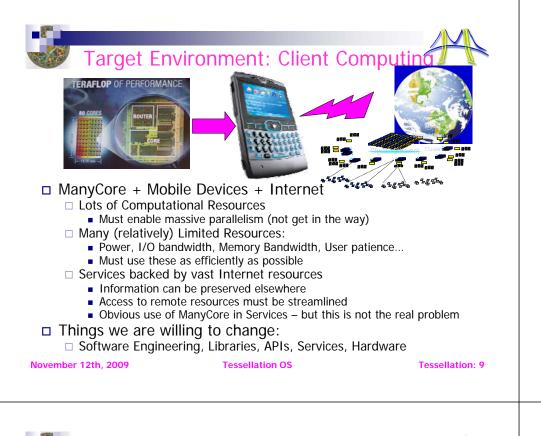
#### □ What is the ParLAB?

- □ A new Laboratory on Parallelism at Berkeley
  - Remodeled "open floorplan" space on 5th floor of Soda Hall
  - 10+ faculty, some two-feet in, others collaborating
- □ Funded by Intel, Microsoft, and other affilliate partners
- □ Goal: Productive, Efficient, Correct, Portable SW for 100+ cores & scale as core increase every 2 years (!)
- □ Application Driven! (really!)

#### □ Some History

- Berkeley researchers from many backgrounds started meeting in Feb. 2005 to discuss parallelism
  - Circuit design, computer architecture, massively parallel computing, computer-aided design, embedded hardware and software, programming languages, compilers, scientific programming, and numerical analysis
  - Considered successes in high-performance computing (LBNL) and parallel embedded computing (BWRC)
- Led to "Berkeley View" Tech. Report 12/2006 and new Parallel Computing Laboratory ("Par Lab")
  - Won invited competition form Intel/MS of top 25 CS Departments





# (David Wessel)

- Musicians have an insatiable appetite for
  - computation + real-time demands
  - More channels, instruments, more processing,
    - more interaction!
  - Latency must be low (5 ms)
    Must be reliable (No clicks!)
- 1. Music Enhancer
  - Enhanced sound delivery systems for home sound systems using large microphone and speaker arrays
  - Laptop/Handheld recreate 3D sound over ear buds
- 2. Hearing Augmenter
  - □ Handheld as accelerator for hearing aid
- 3. Novel Instrument User Interface
  - New composition and performance systems beyond keyboards
  - Input device for Laptop/Handheld

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Image

Database

1000's of

images

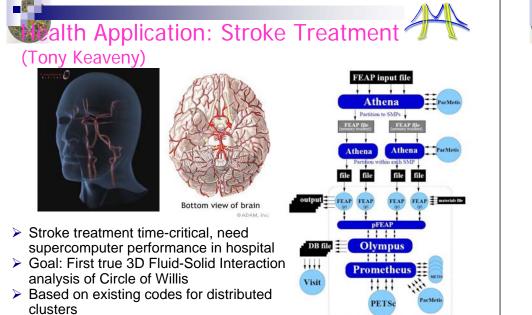
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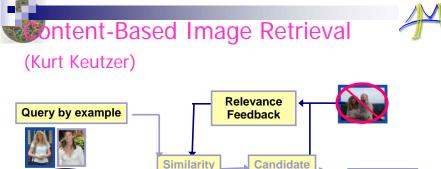
Tessellation OS

Tessellation: 10

Final Result

ressenation: 12





Results

□ Built around Key Characteristics of personal

Complex pictures including people, events, places,

□ Very large number of pictures (>5K)

**Metric** 

□ Non-labeled images

and objects

□ Many pictures of few people

ressenation up

databases



Technology (CNMAT) created a compact loudspeaker array: 10-inch-diameter

icosahedron incorporating 120 tweeters.

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## bust Speech Recognition

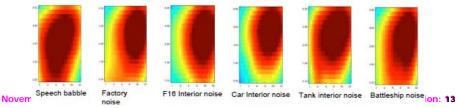
#### (Nelson Morgan)

#### Meeting Diarist

□ Laptops/ Handhelds at meeting coordinate to create speaker identified, partially transcribed text diary of meeting



#### Use cortically-inspired manystream spatio-temporal features to tolerate noise



# Parallel Browser

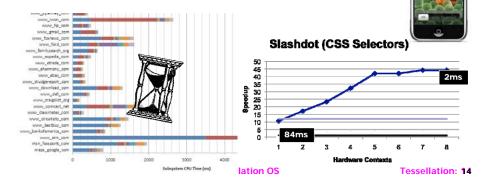
#### (Ras Bodik)

Goal: Desktop quality browsing on handhelds

□ Enabled by 4G networks, better output devices

#### □ Bottlenecks to parallelize

□ Parsing, Rendering, Scripting





# Parallel Software Engineering



#### □ How do we hope to tackle parallel programming?

□ Through Software Engineering and Control of Resources

- □ Two type of programmers:
  - □ Productivity programmers (90% of programmers)
    - Not parallel programmers, rather domain specific programmers
  - □ Efficiency programmers (10% of programmers)
    - Parallel programmers, extremely competent at handling parallel programming issues
- □ Target new ways to express software so that is can be execute in parallel
  - Parallel Patterns
- □ System support to avoid "getting in the way" of the result
  - □ Parallel Libraries, Autotuning, On-the-fly compilation
  - □ Explicitly managed resource containers (Partitions)

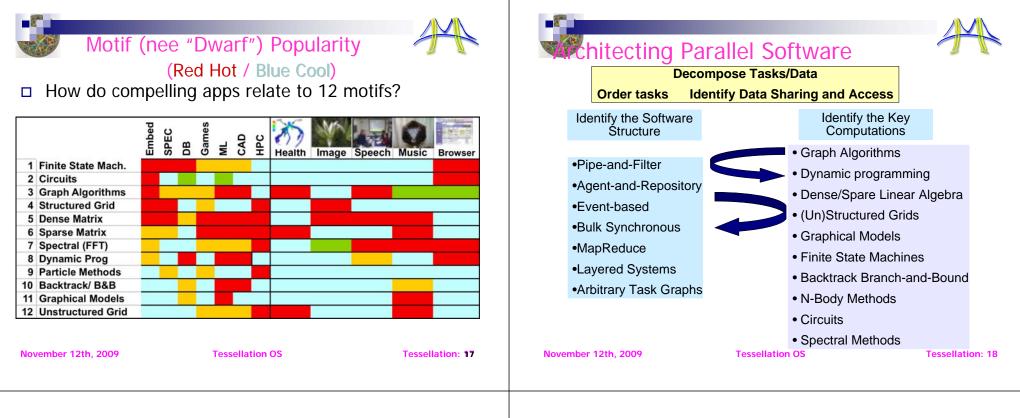
Architecting Parallel Software with Patterns (Kurt Keutzer/Tim Mattson)

Our initial survey of many applications brought out common recurring patterns:

"Dwarfs" -> Motifs

- Computational patterns
- □ Structural patterns
- Insight: Successful codes have a comprehensible software architecture:
- □ Patterns give human language in which to describe architecture





## Par Lab is Multi-Lingual



- Applications require ability to compose parallel code written in many languages and several different parallel programming models
  - $\hfill\square$  Let application writer choose language/model best suited to task
  - $\hfill\square$  High-level productivity code and low-level efficiency code
  - $\hfill\square$  Old legacy code plus shiny new code
- □ Correctness through all means possible
  - $\hfill\square$  Static verification, annotations, directed testing, dynamic checking
  - □ Framework-specific constraints on non-determinism
  - Programmer-specified semantic determinism
  - Require common spec between languages for static checker
- Common linking format at low level (Lithe) not intermediate compiler form
  - $\hfill\square$  Support hand-tuned code and future languages & parallel models

## Selective Embedded Just-In-Time Specialization (SEJITS) for Productivity (Armando Fox)

- Modern scripting languages (e.g., Python and Ruby) have powerful language features and are easy to use
- Idea: Dynamically generate source code in C within the context of a Python or Ruby interpreter, allowing app to be written using Python or Ruby abstractions but automatically generating, compiling C at runtime
- Like a JIT but
  - Selective: Targets a particular method and a particular language/platform (C+OpenMP on multicore or CUDA on GPU)
  - □ **Embedded**: Make specialization machinery productive by implementing in Python or Ruby itself by exploiting key features: introspection, runtime dynamic linking, and foreign function interfaces with language-neutral data representation

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## Autotuning for Code Generation

(Demmel, Yelick)

- Problem: generating optimal code like searching for needle in haystack
- □ Manycore → even more diverse
- □ New approach: "Auto-tuners"
  - 1st generate program variations of combinations of optimizations
     (blocking, prefetching, ...) and data structures
  - Then compile and run to heuristically search for best code for <u>that</u> computer
- Examples: PHiPAC (BLAS), Atlas (BLAS), Spiral (DSP), FFT-W (FFT) November 12th, 2009 Tessellation OS

Tessellation: 21

Search space for

(dense matrix):

Axes are block

Temperature is

speed

dimensions

block sizes

```
Outline
```

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Tessellation: 22

## Services Support for Applications

- What systems support do we need for new ManyCore applications?
  - □ Should we just port parallel Linux or Windows 7 and be done with it?
- □ Clearly, these new applications will contain:

#### □ Explicitly parallel components

- However, parallelism may be "hard won" (not embarrassingly parallel)
- Must not interfere with this parallelism
- □ Direct interaction with Internet and "Cloud" services
  - Potentially extensive use of remote services
  - Serious security/data vulnerability concerns
- Real Time requirements
  - Sophisticated multimedia interactions
  - Control of/interaction with health-related devices
- Responsiveness Requirements
  - Provide a good interactive experience to users

# PARLab OS Goals: RAPPidS

- □ Responsiveness: Meets real-time guarantees
  - □ Good user experience with UI expected
  - □ Illusion of Rapid I/O while still providing guarantees
  - □ Real-Time applications (speech, music, video) will be assumed
- □ Agility: Can deal with rapidly changing environment
  - Programs not completely assembled until runtime
  - □ User may request complex mix of services at moment's notice
- Resources change rapidly (bandwidth, power, etc)
- Power-Efficiency: Efficient power-performance tradeoffs
  Application-Specific parallel scheduling on Bare Metal partitions
  Explicitly parallel, power-aware OS service architecture
- □ Persistence: User experience persists across device failures
  - □ Fully integrated with persistent storage infrastructures
  - Customizations not be lost on "reboot"
- Security and Correctness: Must be hard to compromise
  - □ Untrusted and/or buggy components handled gracefully
  - Combination of *verification* and *isolation* at many levels
    Privacy, Integrity, Authenticity of information asserted

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**Tessellation OS** 





# The Problem with Current OSs

- What is wrong with current Operating Systems?
  - They do not allow expression of application requirements
    - Minimal Frame Rate, Minimal Memory Bandwidth, Minimal QoS from system Services, Real Time Constraints, ...
    - No clean interfaces for reflecting these requirements
  - □ They do not provide guarantees that applications can use
    - They do not provide performance isolation
    - Resources can be removed or decreased without permission
    - Maximum response time to events cannot be characterized
  - □ They do not provide fully custom scheduling
    - In a parallel programming environment, ideal scheduling can depend crucially on the programming model
  - □ They do not provide sufficient Security or Correctness
    - Monolithic Kernels get compromised all the time
    - Applications cannot express domains of trust within themselves without using a heavyweight process model
- □ The advent of ManyCore both:
  - Exacerbates the above with a greater number of shared resources
- Provides an opportunity to change the fundamental model
  November 12th, 2009
  Tessellation 0S
  Tessellation 25

# A First Step: Two Level Scheduling

Monolithic CPU and Resource Scheduling Application Specific

□ Split monolithic scheduling into two pieces:

Course-Grained Resource Allocation and Distribution

- Chunks of resources (CPUs, Memory Bandwidth, QoS to Services) distributed to application (system) components
- Option to simply turn off unused resources (Important for Power)
- □ Fine-Grained Application-Specific Scheduling
  - Applications are allowed to utilize their resources in any way they see fit

Scheduling

Other components of the system cannot interfere with their use of resources

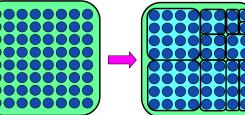
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Tessellation: 26



## Important Mechanism: Spatial Partitioning



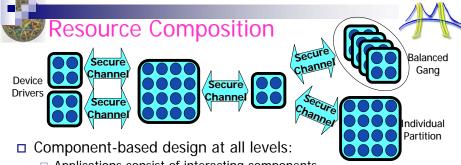
- Spatial Partition: group of processors acting within hardware boundary
  Boundaries are "hard", communication between partitions controlled
  Anything goes within partition
- □ Each Partition receives a *vector* of resources
  - Some number of dedicated processors
  - Some set of dedicated resources (exclusive access)
  - Complete access to certain hardware devices
  - Dedicated raw storage partition
  - □ Some guaranteed fraction of other resources (QoS guarantee):
    - Memory bandwidth, Network bandwidth
    - fractional services from other partitions

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Tessellation OS

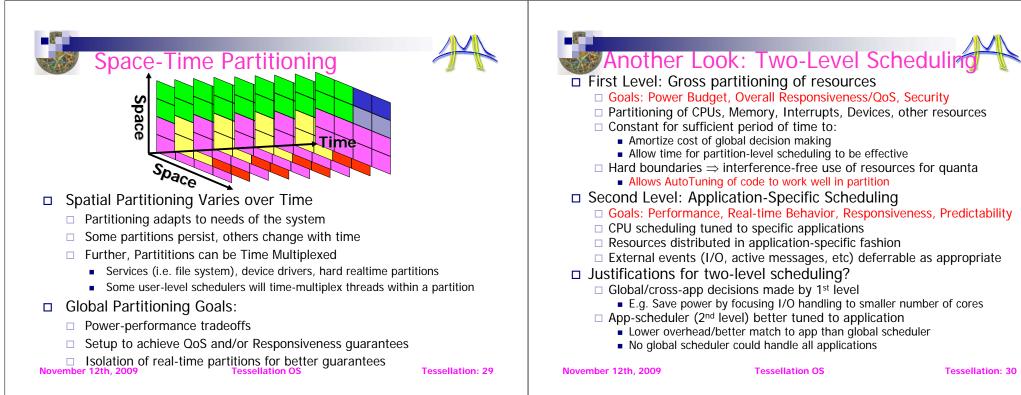


**Tessellation: 27** 



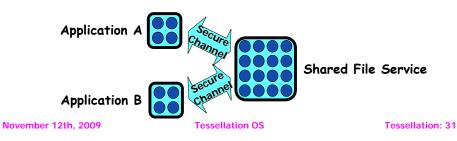
- Applications consist of interacting components
- Requires composable: Performance, Interfaces, Security
- □ Spatial Partitioning Helps:
  - □ Protection of computing resources not required within partition
    - High walls between partitions  $\Rightarrow$  anything goes within partition
    - "Bare Metal" access to hardware resources
    - Shared Memory/Message Passing/whatever within partition
  - $\hfill\square$  Partitions exist simultaneously  $\Rightarrow$  fast inter-domain communication
    - Applications split into mutually distrusting partitions w/ controlled communication (echoes of µKernels)

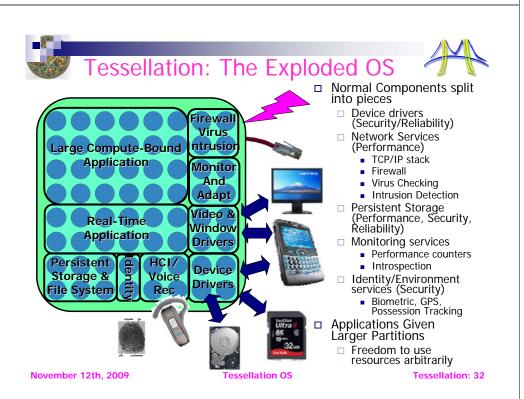
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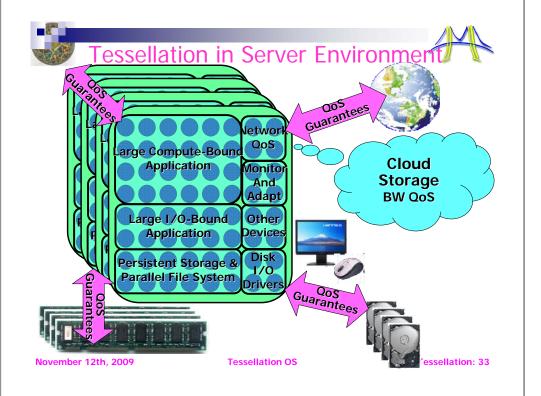


# It's all about the communication

- □ We are interested in communication for many reasons:
  - □ Communication represents a security vulnerability
  - Quality of Service (QoS) boils down message tracking
  - Communication efficiency impacts decomposability
- □ Shared components complicate resource isolation:
  - Need distributed mechanism for tracking and accounting of resource usage
    - E.g.: How do we guarantee that each partition gets a guaranteed fraction of the service:







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November 12th, 2009

**Tessellation OS** 

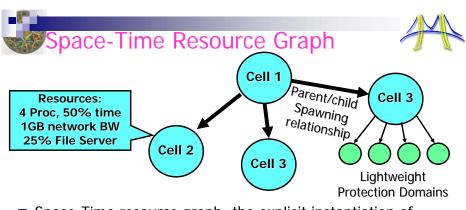
**Tessellation: 34** 



# **Defining the Partitioned Environment**

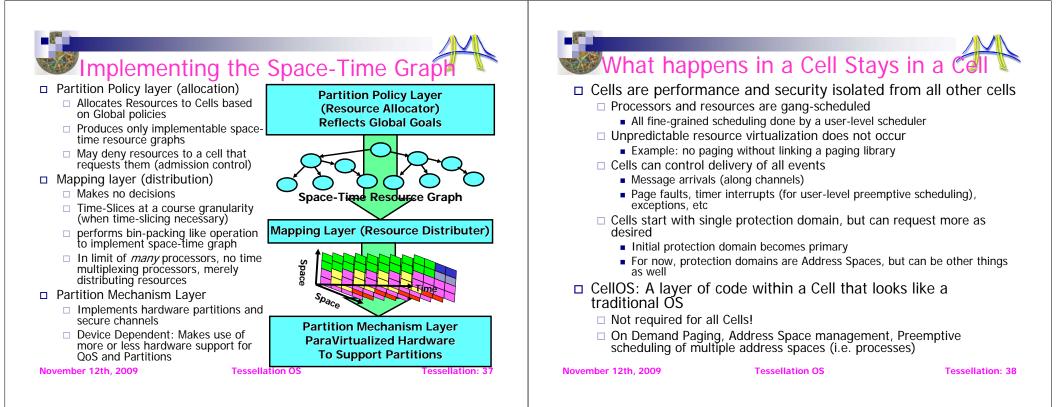
- □ Cell: a bundle of code, with guaranteed resources, running at user level
  - □ Has full control over resources it owns ("Bare Metal")
  - □ Contains at least one address space (memory protection domain), but could contain more than one
  - □ Contains a set of secured channel endpoints to other Cells
  - □ Interacts with trusted layers of Tessellation (e.g. the "NanoVisor") via a heavily Paravirtualized Interface
    - E.g. Can manipulate its address mappings but does not know what page tables even look like
  - □ We think of these as components of an application or the OS
- □ When mapped to the hardware, a cell gets:
  - □ Gang-schedule hardware thread resources ("Harts")
  - □ Guaranteed fractions of other physical resources
    - Physical Pages (DRAM), Cache partitions, memory bandwidth, power
  - □ Guaranteed fractions of system services

**Tessellation: 35** 



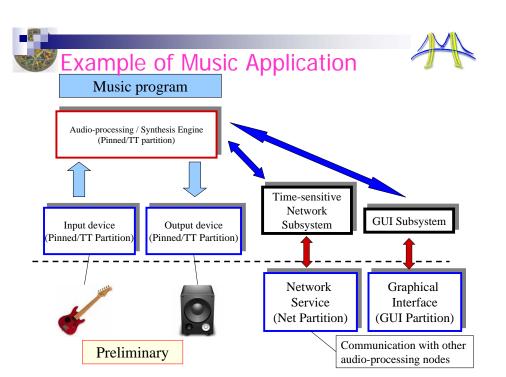
- □ Space-Time resource graph: the explicit instantiation of resource assignments
  - □ Directed Arrows Express Parent/Child Spawning Relationship
  - □ All resources have a Space/Time component
    - E.g. X Processors/fraction of time, or Y Bytes/Sec
- □ What does it mean to give resources to a Cell?
  - □ The Cell has a position in the Space-Time resource graph and
  - □ The resources are added to the cell's resource label

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## Scheduling inside a cell

- □ Cell Scheduler can rely on:
  - Course-grained time quanta allowing efficient fine-grained use of resources
  - □ Gang-Scheduling of processors within a cell
  - $\hfill\square$  No unexpected removal of resources
  - □ Full Control over arrival of events
    - Can disable events, poll for events, etc.
- □ Application-specific scheduling for performance
  - □ Lithe Scheduler Framework (for constructing schedulers)
  - □ Systematic mechanism for building composable schedulers
    - Parallel libraries with completely different parallelism models can be easily composed
- □ Application-specific scheduling for Real-Time
  - □ Label Cell with Time-Based Labels. Examples:
    - Run every 1s for 100ms synchronized to ± 5ms of a global time base
    - Pin a cell to 100% of some set of processors
  - □ Then, maintain own deadline scheduler
- □ Pure environment of a Cell ⇒ Autotuning will return same performance at runtime as during training phase November 12th, 2009 Tessellation 05 Tessellation: 39





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#### Tessellation implementation

- □ Hardware Support
- Tessellation Software Stack
- Status

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November 12th, 2009
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November 12th, 2009

**Tessellation OS** 

**Tessellation: 41** 

**Tessellation: 43** 

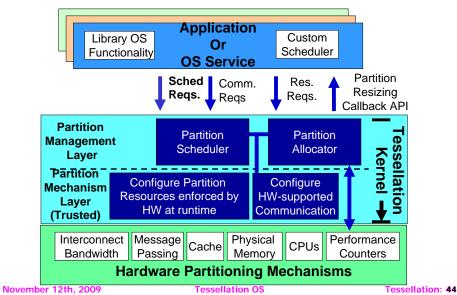
#### What would we like from the Hardwar A good parallel computing platform (Obviously!) Good synchronization, communication ■ On chip ⇒ Can do fast barrier synchronization with combinational logic Shared memory relatively easy on chip Vector, GPU, SIMD Can exploit data parallel modes of computation □ Measurement: performance counters Partitioning Support □ Caches: Give exclusive chunks of cache to partitions Techniques such as page coloring are poor-man's equivalent □ Memory: Ability to restrict chunks of memory to a given partition Partition-physical to physical mapping: 16MB page sizes? □ High-performance barrier mechanisms partitioned properly System Bandwidth Power Ability to put partitions to sleep, wake them up quicly Fast messaging support Used for inter-partition communication DMA, user-level notification mechanisms □ Secure Tagging? QoS Enforcement Mechanisms □ Ability to give restricted fractions of bandwidth Message Interface: Tracking of message rates with source-suppression for QoS □ Examples: Globally Synchronized Frames (ISCA 2008, Lee and Asanovic) Tessellation: 42 November 12th, 2009 Tessellation OS

RAMP Gold: FAST Emulation of new Hardware RAMP emulation model for Parlab manycore □ SPARC v8 ISA -> v9 □ Considering ARM model □ Single-socket manycore target MEMC MEMC MEMC □ Split functional/timing model, both in hardware Functional model: Executes ISA □ Timing model: Capture pipeline Timing Arch timing detail (can be cycle accurate) State State □ Host multithreading of both functional and timing models unctional Timing Built for Virtex-5 systems (ML505) Model Model or BEE3) Pipeline Pipeline

**Tessellation OS** 



## **Tessellation Architecture**



# Tessellation Implementation Status

□ First version of Tessellation Berkeley ParLAB ~7000 lines of code in NanoVisor layer □ Application Driven: New exciting parallel applications □ Supports basic partitioning □ Tackling the parallel programming problem via Software Cores and caches (via page coloring) Engineering Fast inter-partition channels (via ring buffers in shared memory, soon cross-network channels) □ Parallel Programming Motifs □ Network Driver and TCP/IP stack running in partition Space-Time Partitioning: grouping processors & Devices and Services available across network □ Hard Thread interface to Lithe – a framework for constructing userresources level schedulers behind hardware boundary □ Currently Two ports □ Focus on Quality of Service □ 4-core Nehalem system □ 64-core RAMP emulation of a manycore processor (SPARC) □ Two-level scheduling Will allow experimentation with new hardware resources 1) Global Distribution of resources Examples: 2) Application-Specific scheduling of resources QoS Controlled Memory/Network BW □ Bare Metal Execution within partition □ Cache Partitioning Fast Inter-Partition Channels with security tagging □ Composable performance, security, QoS □ Tessellation OS **Tessellation OS Tessellation: 45 Tessellation OS Tessellation: 46** November 12th, 2009

Conclusion