# Layout Compaction 

Prof. Kurt Keutzer
Prof. A. R. Newton
UC Berkeley
Prof. M. Orshansky
UCB $\rightarrow$ U of Texas

## RTL Design Flow




## Compaction: Introduction

- After P\&R, the layout is functionally complete
- Some vacant space may still be present in the layout
- Due to non-optimality of P\&R
- Compaction = removing vacant space
- Improves cost, performance, and yield
- Key for high-performance full-custom layouts
- Standard cells - only channel heights may be minimized
- But channel compactors are near-optimal


## Layout Compaction



## Compaction: Introduction

- Compaction tries to minimize total layout area while
- Retaining speed
- Respecting violating design rules and designerspecified constraints
- Three ways to minimize the layout area
- Reducing inter-feature space
- Check spacing design rules
- Reducing feature size
- Check size rules
- Reshaping features
- Electrical connectivity must be preserved


## Cross-Section of CMOS Technology



Jan Rabaey

## Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
- scalable design rules: lambda parameter
- absolute dimensions (micron rules)


## CMOS Process Layers

| Layer | Color | Representation |
| :--- | :--- | :--- |
| Well $(p, n)$ | Yellow |  |
| Active Area $(n+, p+)$ | Green |  |
| Select $(p+, n+)$ | Green |  |
| Polysilicon | Red |  |
| Metal1 | Blue |  |
| Metal2 | Magenta |  |
| Contact To Poly | Black |  |
| Contact To Diffusion | Black |  |
| Via | Black |  |

## Intra-Layer Design Rules





## Different Approaches to Compaction

- One dimensional vs. two-dimensional compaction
- 1-D compaction
- Components moved only in $x$ - or $y$-direction
- Efficient algorithms available
- 2-D compaction
- Components may be moved both in $x$ - and $y$-direction
- More effective compaction
- NP-hard
- Determining how x and y should interact to reduce area is hard!
- Historical interest: Constraint-graph based compaction vs. virtual grid based compaction
- Virtual grid methods are fast and simple. Results in larger area.


## Historical interest: Virtual Grid Compaction




- Every features is assumed to lie on a virtual grid line
- Required to stay at grid locations during compaction - no distortion of topology
- Compact by finding min possible spacing between each adjacent pair of grids
- Min spacing is given by worst-case design-rule for any feature on the grid
- Advantage: algorithm is simple and fast


## Constraint-based Compaction



Early tools: Floss, Cabbage, SLIP, SLIM, Sticks

## Layout Constraints

- For a given layout instance, all features may be described by a set of placement constraints
- These layout constraints are imposed by design rules - Min spacing (separation) design rules



## Expressing constraints



$$
\begin{array}{cc}
b \geq \text { origin }+1 & c \geq b+2 \\
d \geq \text { origin }+1 & d \geq b+2 \\
e \geq c+1 & e \geq d+3
\end{array}
$$

- Assuming a left-to-right ordering, can capture constraints by non-equalities
- Example: if $c$ is to the right of $b$, and they have to be 2 units apart: $c \geq b+2$


## Constraint Graph Generation

- Constraint graph generation is the most time-consuming part of constraint-based compaction, approached naively $\mathrm{O}\left(\mathrm{n}^{2}\right)$
- In the worst case, there may be a design rule between every shape of layout
- In reality only a small local subset of constraints are needed
- First generate connectivity (grouping
- In generating separation constraints, non-redundant constraints
- Shadow-propagation algorithm
- Scan-line algorithm



## How do we solve these constraints?



$$
\begin{array}{cc}
b \geq \text { origin }+1 & c \geq b+2 \\
d \geq \text { origin }+1 & d \geq b+2 \\
e \geq c+1 & e \geq d+3
\end{array}
$$

- What is a mathematically efficient way to solve these constraints?


## Use graphical structure



$$
\begin{array}{cc}
b \geq \text { origin }+1 & c \geq b+2 \\
d \geq \text { origin }+1 & d \geq b+2 \\
e \geq c+1 & e \geq d+3
\end{array}
$$



- We can construct a constraint graph to capture layout constraints


## Problem formulation-1

- Use a labeled directed graph
- $G=<V, E>$
- Vertices layout objects
- Edges represent constraints between vertices
- Labels represent constraint values
- Now what do we do with this?

Hint: What problem does this remind you of?


## Problem formulation - 2

- Goal of 1-D compaction is to generate a minimum width layout
- Determination of minimum width is equivalent to solving a longest path problem
- The longest path from source to a vertex is the coordinate of the vertex
- In practical layouts, the constraints graphs are very local
- Most edges represent very local constraints in the layout
- Theoretically, run time is $\mathrm{O}(|\mathrm{V}|+|\mathrm{E}|)$
- Practically, run time is close to linear in |V|, the size of the layout!





## Does graph always have a solution?



- What if we added this edge?


Check for cycles in a graph $G=<V, E$, constraints, Origin $>$ (Origin is the super-source of the graph) depth_first_search $(v)\{$
if visited $(v)==$ TRUE
then return "ERROR, CYCLE IN GRAPH WITH PATH THROUGH v"
else
visited $(v)=$ TRUE
for each edge $\langle v, w\rangle$ from $v$ depth_first_search ( $w$ )
\}

## First Elaboration - Equality Constraints -1

- Inequality constraints capture min spacing design rules
- Need also to capture grouping constraints
- Features from same circuit component
- Need to be moved together
- Grouping constraints are described by equality constraints



## First Elaboration - Equality Constraints -2



## Reflecting Equality Constraints

$e \geq c+1$
$c \geq e-1$


What challenges does this pose to our algorithm?

## Dealing With Legitimate Cycles



- Can we use the longest path algorithm on graphs with legitimate negative-edge cycles?
- Topological longest path algorithm can't handle them.
- Can use a Bellman / Moore algorithm for general graphs
- Run time is $\mathrm{O}\left(|\mathrm{V}|^{*}|\mathrm{E}|\right)$
- Run time of topological longest path algorithm on DAG is $\mathrm{O}(|\mathrm{V}|+|\mathrm{E}|)$


## Alternative Approach to Equality Constraints


origin


Handle equality constraints independently
Build independent graph for equality constraints
Express inequality constraints between designated representatives

## Handling Equality Constraints


origin $=x+1$

origin $=y+1$

$$
v=w+2
$$

$\mathrm{w}=\mathrm{u}-2$ i.e. $\mathrm{u}=\mathrm{w}+2$
$z=y+1$
origin $=\mathrm{z}+2$
$u=t-3$ i.e. or $t=u+3$

## Handling Equality Constraints

origin $=x+1$
origin $=y+1$
$y=z+1$

Generally, this
is known as the union-find algorithm


## Constraint-Based Compaction Approach: Overview

Build constraint graph
if equality constraint
add to equality constraint graph
if inequality constraint
find distinguished representatives of each vertex in constraint add constraint between distinguished representatives
Check for cycles in inequality constraint graph
If cycles exist terminate with error
Solve equality constraint graph
Solve inequality constraint graph

## Compaction Enhancements

- 1-D constraint-based compaction problem can be formulated optimally and computationally efficiently
- In real circuits what we want is often more complex than can be captured in simple linear inequalities of the form:
- $e \geq c+1$
- Or equalities of the form:
- $u=t-3$
- For example:
- Wirelength minimization
- Spacing, slack distribution
- Jog introduction
- Improving area minimization using:
- $1 \frac{112}{2}$ D compaction
- 2D compaction


## Enhancements: Sliding/Spacing Terminals




## Wire-Length Minimization



- Features not on the critical path will be pulled towards a layout edge because they are given their minimal legal spacing
- May lead to increased wire length and slower circuit performance
- Can re-distribute 'slack' (the available empty space) to the features not on the critical path



## One-and-a-half Dimensional Compaction



C compacted up



C compacted down


If we could just bump C over

## One-and-a-half Dimensional Compaction

- Key idea: provide enough lateral movements to blocks during compaction to resolve interferences
- Algorithm starts with a partially compacted layout (two applications of 1-D compaction)
- Maintain two lists - floor and ceiling
- Floor is a list of blocks visible from the top, ceiling is the list of blocks visible from the bottom
- Select the lowest block in the ceiling and move it to the floor maximizing the gap between floor and ceiling.
- Continue until all blocks have been moved from ceiling to floor.


## 1-Dimensional Compaction in 2D


$X$ then $Y$ 1D Compaction $Y$ then $X$ 1D Compaction

## True Two-Dimensional Compaction




2D Compaction

- Two dimensional compaction is NP Hard (C. K. Wong, 1984)
- Choosing how two dimensions should interact to produce optimal is hard
- Can formulate as integer-linear programming problem - Worst-case complexity is exponential


## What makes 2-D compaction hard?



- Two dimensional compaction is NP Hard (C. K. Wong, 1984)
- Choosing how two dimensions should interact to produce optimal is hard
- Can formulate as integer-linear programming problem
- Worst-case complexity is exponential


## Choices



## Background Material

Handout:
Chapter 2: entitled Images of Algorithms and Techniques for VLSI Layout Synthesis, Kluwer Academic Publishers, 1989. pages 6-30..
Algorithmic background:
Introduction to Algorithms, T. Cormen, C. Lesierson, R. Rivest, The MIT Press, Second Printing, 1996.
depth-first search 477-485
shortest paths 514-578 (probably overkill for our purposes)
union-find algorithm (disjoint forest implementation 448)

