Novel method for silicon quantum wire transistor fabrication

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Local stress-limited oxidation was used to fabricate silicon quantum wire transistors with a channel diameter of 5 nm. The oxidation of source and drain regions was prevented with a silicon nitride diffusion barrier. A novel wraparound gate was used to improve the gate control of the potential in the channel. The electrical properties of these devices were investigated at room temperature. Ideal subthreshold behavior, with the subthreshold swing equal to 60.3 mV/dec, was observed. © *1999 American Vacuum Society.* [S0734-211X(99)16906-3]

I. INTRODUCTION

Recently, fully depleted silicon-on-insulator (SOI) devices have been studied extensively as a solution to the short channel leakage problems associated with sub-100 nm gate metal-oxide semiconductor (MOS) field-effect transistors. In particular, structures that eliminate a part of the body region have been shown to result in reduced leakage currents.[1] An example of such a structure is a device that utilizes a very thin undoped silicon wire as the channel. The gate is wrapped around the oxide surrounding the wire, forming a quantum wire transistor. Quantum wire transistors are expected to show excellent subthreshold characteristics and are possible candidates for very short-channel length metal-oxide semiconductor field effect transistors (MOSFETs) and quantum devices.[2]

In this experiment, stress-limited[3–5] oxidation was used to fabricate quantum wire transistors with channels as small as 5 nm in diameter. Starting with (100) SOI wafers, 50 nm silicon lines were defined using electron beam lithography. A patterned nitride layer was used to confine the stress-limited oxidation to the wire regions, preventing the oxidation of the source and drain. The wire was gated with a wraparound phosphorus-doped polysilicon gate. The wires show ideal subthreshold behavior, and high on-state current.

II. EXPERIMENT

Electron beam lithography, for levels that required it, was performed using on a modified Leica VB6-HR system[6] (Nanowriter), at an operating voltage of 100 keV. The Nanowriter is equipped with a backscattered electron detector for use in alignment. However, at 100 keV, the contrast between the standard microfabrication materials—silicon nitride, silicon oxide, and silicon—was too low for the signal to be useful. This is because the backscattering coefficient is similar for all of these materials. Instead, alignment was done using $Si_{0.5}Ge_{0.5}$, alignment marks that were 8000 Å thick. The addition of 50% germanium to silicon significantly increases the material's backscattering coefficient, without drastically changing its response to dry or wet etches. The alignment marks were placed at the corners of every field, and the Nanowriter aligned automatically to them after each stage translation. To ensure the best possible alignment, field-stitching was avoided by keeping the die size below 520 μm. Typical misalignment was about 8 nm, which is the electron beam step size.

Devices were fabricated from (100) SOI wafers, created using the SmartCut®[7] technique. The thickness uniformity of the silicon film was approximately 50 Å in the center of the wafer. The top silicon layer was thinned to 30 nm using dry oxidation followed by a timed HF etch that left a 300 Å pad oxide. The first lithography level was the definition of the 8000 Å thick $Si_{0.5}Ge_{0.5}$ alignment layer deposited on the pad oxide. Since the alignment marks were crosses with a minimum width of 1 μm, this level was defined using an I-line optical lithography process. After the dry etch of the alignment layer, the pad oxide was removed from the field by another timed HF dip. The next lithography level defined the silicon mesa by an electron beam exposure using SAL-601 negative resist.[8] A single-pass exposure and a short 30 s post-exposure bake were used to achieve linewidths down to 30 nm. The threshold line dose was 0.3 nC/cm, exposed with a beam 8 nm in diameter. This level defined the source and drain mesas, as well as the wire width prior to stress-limited oxidation. The area exposure of the mesas was done with a dose of 80 $\mu C/cm^2$. Wires of various widths were fabricated using different line doses and number of passes. Figure 1 shows a SEM picture of a 50 nm wide wire and pads, after a dry etch and resist strip. This wire was exposed with three passes of 0.15 nC/cm. The multiple pass exposure was used to decrease the linewidth variation. The single pass lines had 10 nm width variation, using three passes the variation was reduced to 5 nm. The line quality further improved with an increasing number of passes, but at the expense of a larger feature size.

Stress-limited oxidation was used to shrink the silicon wires defined by the mesa etch to their final diameter of a few nanometers. However, since stress-limited oxidation relies on the fact that wires oxidize more slowly than planar

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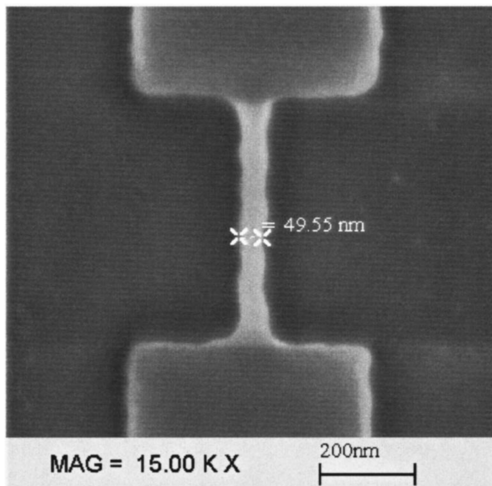

FIG. 1. SEM of a 50 nm wide, 30 nm tall silicon line defined by the mesa etch. The line shows variation due to the noise in the electron beam lithography system.

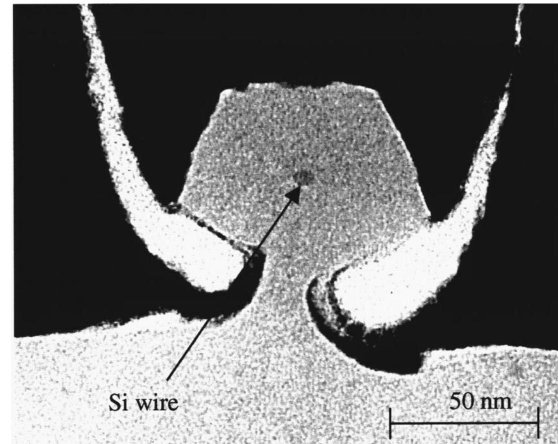

FIG. 3. TEM cross section micrograph of a 5–7 nm Si quantum wire. This wire was formed by a 925 °C stress-limited oxidation of a 45 nm wide 40 nm tall silicon line drawn in the ⟨100⟩ direction. The black region is a metal layer used to protect the wire during sample preparation.

regions, the source and drain regions had to be protected during the oxidation step. Therefore, after the mesa etch, a 200 Å layer of pad oxide and 250 Å layer of silicon nitride were deposited. The nitride was patterned using a second electron beam lithography step. The nitride windows were exposed in the regions where the wires were to be thinned, as shown in Fig. 2. The source and drain pad regions retained their nitride coat.

Following the nitride etch, the pad oxide was removed with a timed HF dip. The HF overetch also undercut the buried oxide under the wires. The partial undercut of the oxide prior to stress-limited oxidation is needed to make the oxidation proceed symmetrically.[4] The stress-limited oxidation was done at 875 °C, in a dry O_2 ambient, for 5 h. After stress-limited oxidation, the wire diameter is projected[3] to be 4–8 nm, for wires that were 50 nm wide and 30 nm tall prior to oxidation. Figure 3 shows a TEM micrograph of a 5–6 nm wire, prepared using stress limited oxidation in an earlier study. After the stress limited oxidation, the nitride was removed with a wet phosphoric acid etch. It is important to have a nitride coat of sufficient thickness, since it will be under severe stress during the oxidation. The nitride thickness of 250 Å was chosen due to the nitride-to-oxide etch selectivity limitations, and some signs of stress induced cracking in the nitride were observed. The SF_6 nitride etch used in this experiment etches silicon quickly, and has only a 3:1 selectivity to oxide. Therefore the 250 Å nitride film thickness was chosen to prevent the nitride etch from attacking the silicon mesa during the overetch step. A 1200 Å thick polysilicon gate, *in situ* doped with phosphorus, was deposited following the nitride removal. The pad oxide remaining from the nitride etch served as the gate oxide in the mesa regions, and the oxide generated during stress limited oxidation served this purpose in the wire regions. The gate was patterned using the third and final electron beam lithography step, using the same lithography process as mesa definition. Figure 4 shows a 200 nm gate after etching and resist removal. Following gate etch the wafers were implanted with a 3×10^{15} ions/cm^2, 50 keV, As^+ source, and drain implant. The dopants were activated using a 950 °C, 15 min, anneal in nitrogen. The contact and metal layers were defined using optical lithography, using deposited oxide as dielectric, and aluminum as metal. Alignment of the optical levels was done using alignment keys exposed at the gate level.

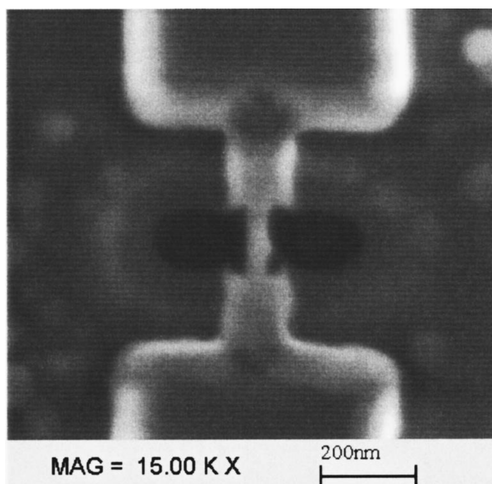

FIG. 2. SEM of a 50 nm wide silicon line after the isotropic nitride etch. Outside the oval region the silicon is covered by 200 Å of pad oxide and 250 Å of nitride. The nitride opening is 130 nm wide, approximately 30 nm wider then drawn.

III. DISCUSSION

The aspect ratio of the wires prior to stress-limited oxidation strongly impacts their post-oxidation profile. For the post-oxidation profile to be that of a thin wire, 4–6 nm in diameter, wires drawn in the ⟨110⟩ direction should be wider than they are tall. This is because the linear oxidation rates for the (100) plane is ~1.6 times slower than the rate for the (110) plane.[9] For wires in the ⟨100⟩ direction, the aspect ratio

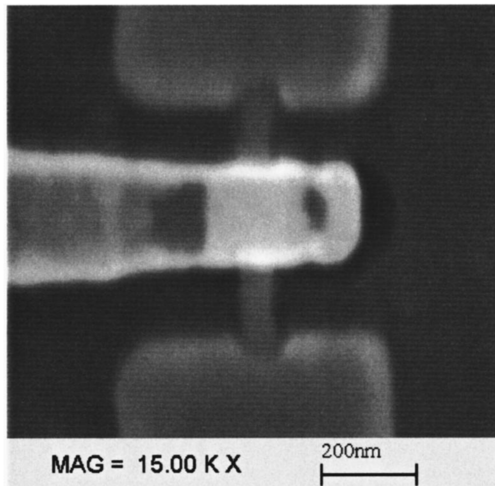

FIG. 4. SEM of a quantum wire transistor following gate etch. The wraparound phosphorus doped polysilicon gate is 200 nm wide and 1200 Å tall.

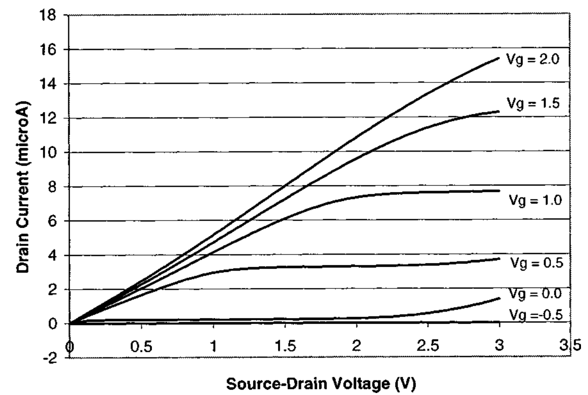

FIG. 5. Plot of the drain current vs drain voltage for different gate bias (V_g), of a 250 nm gate-length quantum wire transistor. Wire is drawn in the ⟨110⟩ direction, and has an estimated diameter of 5 nm, and gate oxide of 250 Å.

should be close to 1, as in Fig. 3. Wires with aspect ratios that deviate from these values usually pinchoff into a double wire core profile during the oxidation.

The preoxidation linewidth was not limited by the resolution of the electron beam lithography process. By using SAL-601 resist exposed by a 100 keV electron beam, together with resist ashing, lines down to 20 nm were achieved. However, using lines that thin was impractical since, for the correct aspect ratio to be maintained, the mesa would have to be only 12 nm tall. With such thin source and drain pad regions, the contact and series resistance of the device would be large. Taking into consideration the series resistance concerns, a mesa height of 30 nm was chosen, giving a ⟨110⟩ wire width of approximately 50 nm, well above the minimum resolution of the e-beam lithography process.

Due to the undercut of the supporting oxide prior to oxidation, the wires oxidized from all sides. Previous studies of stress-limited oxidation indicate that approximately 30 nm of oxide was grown on the (110) sides, and 20 nm was grown on the top and bottom, giving an average gate oxide thickness of around 250 Å. A thinner gate oxide is desirable for device application, since it results in reduced drain induced barrier lowering (DIBL), and an increase in the inversion charge density at a fixed gate voltage. A thinner gate oxide can be fabricated by stripping the oxide generated in the stress-limited oxidation, and regrowing a thinner oxide. However this approach is risky, since the fragile silicon wires, only several nanometers in diameter, are left free standing between the oxide strip and gate deposition steps. The conformal deposition of the polysilicon gate resulted in a wraparound gate, at least in the regions where the buried oxide was etched away. Since the gate was above as well as below the channel, gate doping by implantation is impossible. A simple solution is *in situ* doping but it makes the incorporation of NMOS and PMOS devices on the same wafer difficult, since PMOS and NMOS devices require different gate workfunctions. The use of *in situ* doping for CMOS would require two deposition steps and a removal of the inappropriate gate material from each region. The wraparound gate also creates etching problems in a NMOS process since part of the gate is masked by the wire during the gate etch. However since the gate is underneath the wire only in sections defined by the second lithography step, this problem is solved by making the gate wider then the nitride opening. In this experiment the gate was made 128 nm wider than the nitride window.

The exact profile of the wire between the edge of the gate and the bulk source and drain regions is also important to device behavior. Since the stress-limited oxidation was confined with a silicon nitride coat, it is expected that the oxide profile is similar to the birds-beak profile seen in local oxidation of silicon (LOCOS). Therefore it is expected that the wire next to the nitride opening will also be thinned, significantly increasing the series resistance. A simple solution is to shorten the wire, and make the gate overlap the bulk regions. In the devices described in this article this was not done due to misalignment tolerances.

IV. RESULTS

Gated quantum wires exhibited transistor characteristics. Figure 5 shows the drain current response of a 250 nm gate length quantum wire for different applied gate voltages (V_g). The saturation current at a V_g of 1 V is 7.5 μA. Assuming the wire is only 5 nm wire diameter, this translates to a saturation current of 1.5 mA per micron width. Of course the wire cannot be scaled in width directly; wires can only be placed in parallel, with their separation limited by the linewidth before oxidation. The 100 kΩ series resistance, extracted through current measurements at different gate voltages, limits the linear regime current of this quantum wire. The high series resistance is caused by the extension of thin Si wire from under the gate. It is not clear that bulk resistivity of doped silicon can be extrapolated to these small dimensions, but even with a full activation of source/drain doping in the wire the resistance of the extension regions is 1 kΩ per nanometer.

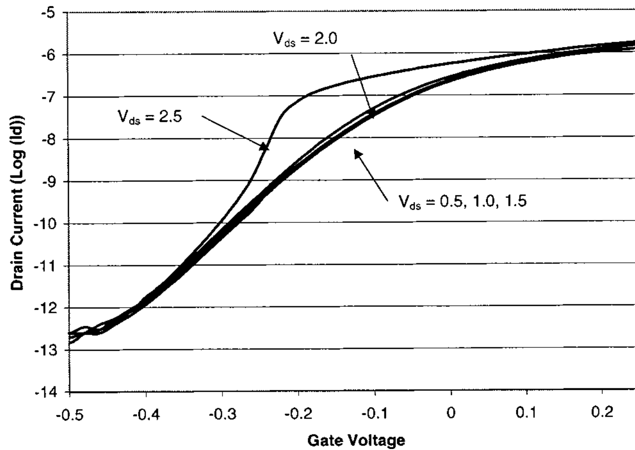

FIG. 6. Plot of the $\log_{10}$ of the drain current vs gate voltage for different source drain bias (V_{ds}), of a 250 nm gate length quantum wire transistor. The threshold voltage is -0.15 V, and the subthreshold swing is 60.3 mV/dec.

Figure 6 shows the subthreshold behavior of a 250 nm quantum wire transistor. The threshold voltage is approximately -0.15 V, exactly as expected with no body doping and an n-type gate. The fact that the quantum wire effectively has no body means that the oxide thickness does not strongly affect the threshold voltage. For gate voltages below the threshold voltage there is no charge in the wire, and therefore no field across the gate oxide. So the electron band energies in the wire track the electron band energies in the gate when the wire is off, except in regions around the source and drain where barrier lowering is significant. The wire turns on when the difference in the Fermi levels between the wire and the source becomes sufficiently small, around 0.15 V. Although the traditional method of threshold voltage control via the body implant is clearly impossible in quantum wire transistors, using a gate material with a different work function can change the threshold voltage. For example, p-type $Si_{0.2}Ge_{0.8}$ can be used to achieve a more typical threshold voltage of around 0.4 V.

Since the quantum wire electron bands track the gate electron bands in the subthreshold region, the subthreshold swing has the ideal value of 60 mV/dec at room temperature. The subthreshold swing is low even though the gate oxide is relatively thick at 250 Å. The thick oxide does reduce the drive current once the device is on. With electrons in the wire, a field develops in the gate oxide, and the wire and gate band potentials are no longer the same; a thinner gate oxide would strengthen the capacitive coupling between the wire and the gate. The thick oxide also increases the DIBL. In Fig. 5 DIBL is clearly visible in the 250 nm quantum wire at source-drain voltages around 3 V with the gate voltage of 0 V. The subthreshold behavior shows an anomaly with V_{ds} of 2.5 V, close to device breakdown. This anomaly is the kink effect often observed in fully depleted SOI devices. It results from the lowering of the barrier by holes in the channel generated by hot electron impact ionization.

Quantum conduction effects are expected in wires with a diameter close to the electron wavelength. Even at 300 K wires with a diameter of 5 nm should show some quantum effects. The high parasitic resistance and thick oxide made the measurement of such effects at room temperature very difficult for quantum wires fabricated in this experiment.

V. CONCLUSION

Stress limited oxidation has been used to fabricate silicon quantum wires down to 4 nm in diameter. These wires were incorporated into transistors by using a LOCOS process to protect the source and drain. The 250 nm gate length quantum wire transistors demonstrate good subthreshold swing, of 60 mV/dec due to the wraparound gate and a lack of body doping. The on current of the transistors was approximately 4 μA, with a 1 V source drain bias, and 1 V $V_g - V_t$. The drive current can be further increased and the behavior of shorter gate devices improved, if the gate oxide thickness in the process can be reduced.

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