

# MOSFETs with 9 to 13 Å Thick Gate Oxides.

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## Abstract

In this work, MOSFETs with gate oxides between 9 to 13 Å have been fabricated and its behavior analyzed. An improved methodology of extracting gate oxide thickness from the MOSFET gate currents in the accumulation regime is proposed. Experimental evidence for mobility reduction mechanism, namely Remote Charge Scattering has been presented. The mobility was found to be degraded because of scattering by ionized impurities in the poly-gate.

## Introduction

Some of the main limitations of MOSFET gate oxide scaling below 15 Å are tunneling leakage currents through gate oxides [1], mobility degradation of the inversion charge because of a large vertical field [2], IR drop in the gate electrode because of a combination of large tunneling current and a finite gate resistance [3]. In previous work, we theoretically speculated that the inversion layer mobility would be further degraded because of ionized impurities in the gate through remote charge scattering (RCS) [4]. In this study, MOSFETs with ultra-thin gate oxides, gate oxide thickness  $T_{ox}$  between 9-15 Å were fabricated and analyzed, and experimental results of the aforementioned physical mechanisms have been characterized and reported.

A big hurdle in the analysis of MOSFETs with ultra-thin oxides (less than 13 Å) is a lack of an accurate tool to precisely determine the gate oxide thickness. In this work, we introduce a novel methodology to extract  $T_{ox}$  from the MOSFET accumulation tunneling currents. Fujioka et al [5] modeled direct tunneling currents through gate oxides and verified it down to  $T_{ox}=15$  Å. We have expanded upon that work by numerically evaluating the direct tunneling currents. The tunneling current through the gate is given by:

$$J = 4\pi me/h^3 \int dE (E_{fm} - E) T(E) \quad (1)$$

Where  $m$  is the free electron mass,  $e$  the electronic charge,  $E$  the electron energy,  $T$  is the transmission probability within the WKB approximation [6]. The above expression has been numerically integrated as a result of which accurate simulation results for the tunneling current in the low field regime is obtained. Also, the sub-0.5 Volt tunneling regime has been modeled by evaluating the integral limits in eqn. (1) as the electron energy varies from  $(E_{fm} - eT_{ox})$  to  $E_{fm}$ . This fairly accurately models the knee in the direct tunneling currents. The tunneling probability also includes

an analytical expression for the reflection of the electron wave at the potential discontinuities [7]. From the simulation of tunneling currents in MOSFETs with different  $T_{ox}$ , simple empirical relationships have been formulated and presented here.

The mobility of inversion layer electrons in MOSFETs is then computed with  $T_{ox}$  extracted from the previously explained procedure. Mobility was found to be degraded by 20-30 % because of RCS.

## Experiment

LDD NMOSFETs were fabricated on P-type Czochralski and epitaxial Si substrates (100) with LOCOS isolation. Gate oxides were grown thermally at 600-675 °C for 5 minutes with varying post oxidation anneals. Drawn gate lengths were between 0.5-50  $\mu\text{m}$  and the resist patterns were further reduced by 0.4  $\mu\text{m}$  using an isotropic  $\text{O}_2$  plasma ashing process. The gate was etched with a high selectivity Si etch based on HBr and  $\text{Cl}_2$  chemistry which prevented the active areas from being damaged during the gate etch. Poly-Si gate was doped using P implantation with varying doses ( $7.5 \times 10^{14}$ ,  $1.5 \times 10^{15}$ ,  $3 \times 10^{15}$ ,  $7 \times 10^{15} / \text{cm}^2$ ) which formed the experimental split to study the effect of remote charge scattering. RTA was performed at 1000 °C for 7 sec to activate dopants.

## Results and Discussion

Fig. 1 is a high resolution TEM cross-section showing a gate stack with  $13 \pm 2$  Å gate oxide thickness.

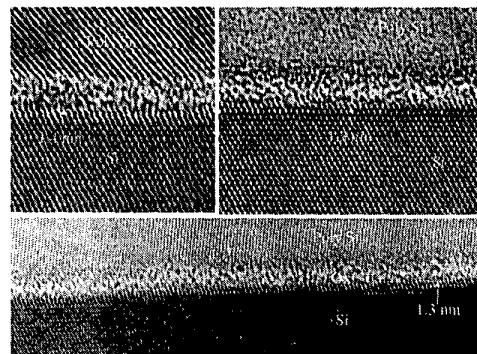


Fig 1: High resolution TEM of a MOSFET gate stack. Gate oxide thickness extracted from the lattice fringes of Si correspond to 1.3 nm with a variation of 0.2 nm within the wafer.

**High Frequency CV of NMOSFETs:**  
L/W = 10/10; Tox = 13 Å

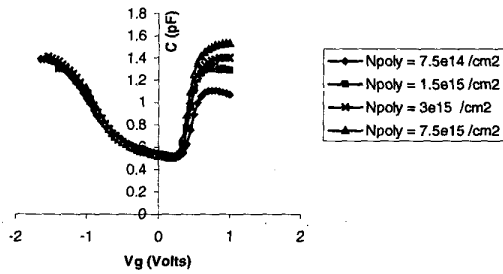


Fig 2: CV curves are consistent with 13 Å oxide thickness. Substrate doping concentrations are the same for all poly-gate dopant densities, suggesting negligible dopant penetration from the poly to the channel. However, it is difficult to extract Tox from CV.

The ellipsometer data taken immediately after the gate oxide growth on test wafers showed  $13 \pm 5$  Å. High frequency CV curves taken on a 10/10 MOSFET (Fig. 2) confirmed the Tox to be 13-14 Å. CV curves are not reliable to measure Tox in the ultra-thin gate oxide regime since large gate leakage currents affect measurement readings. However, we have used it for determining the active gate and substrate dopant concentrations. In this work, Tox was extracted by measuring gate tunneling currents from FET structures. Fig. 3 shows that the direct tunneling currents measured in the positive gate polarity are sensitive to poly depletion and threshold shifts.

**Inversion tunneling characteristics:**  
L/W = 10/10: Epi substrate NMOSFETs

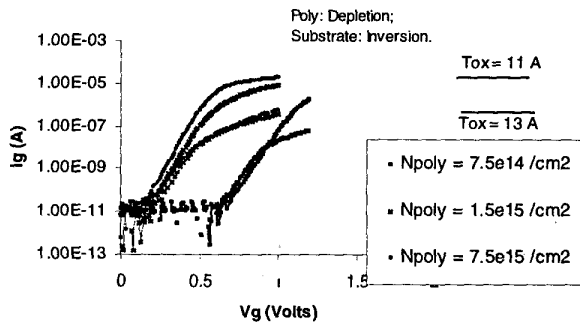


Fig 3: Inversion gate currents of a MOSFET are sensitive to poly depletion and  $V_t$  differences. Tox extraction becomes error prone.

We propose to extract Tox from MOSFET gate currents in the accumulation regime. At negative gate bias, both the poly and the substrate are in accumulation. As shown in Fig. 4, the gate currents in accumulation for any Tox with different poly doping and  $V_t$ , all fall in the same curve and therefore,

**Accumulation tunneling currents:**  
L/W=10/10 NMOSFETs

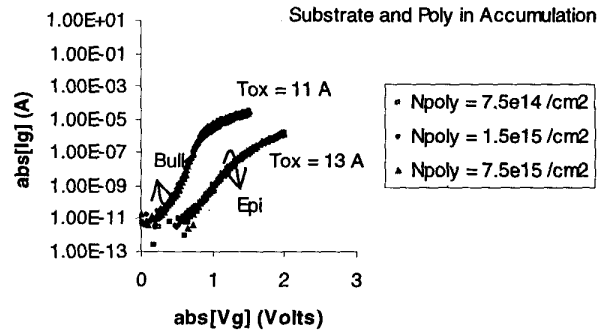


Fig 4: Accumulation gate currents of a MOSFET are insensitive to poly depletion and  $V_t$  differences, therefore ideal for Tox extraction.

provide an excellent way to determine Tox. Also, the gate current characteristics were not significantly different for the epi and the Czochralski substrates. Tox was determined with the direct-tunneling model described above. As shown in Fig. 5, the model shows good agreement with measured data for MOSFET accumulation currents between 14.5-23 Å. This model was then used to extract Tox down to 9 Å as shown in Fig. 5. Simple equations that evaluate Tox from the gate currents are the following:

$$\text{Tox (nm)} = (10.1 - \log(J_d \text{ (A/cm}^2\text{)})) / 6.2 \quad (2)$$

$$\text{Tox (nm)} = (9.6 - \log(J_d \text{ (A/cm}^2\text{)})) / 6.5 \quad (3)$$

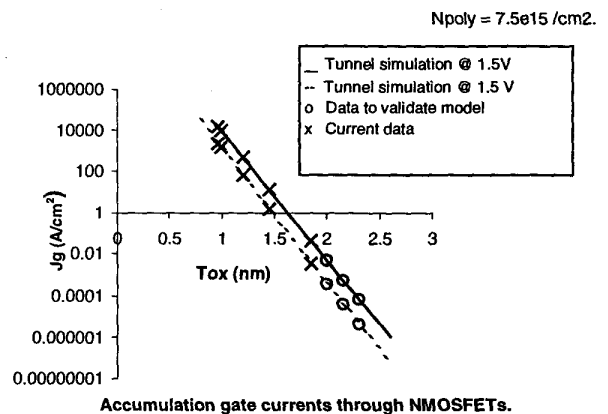


Fig 5: Tunneling model that yields excellent agreement for accumulation gate currents in MOSFETs with Tox between 14-25 Å. The model was used to extract Tox of MOSFETs down to 9 Å by measuring the accumulation gate currents.

Eqn. (2) is for  $T_{ox}$  extracted from the direct tunneling currents measured at 1.5 V, and eqn. (3) when they are measured at 1 V. Though there is no clear difference, equations (2) and (3) produce a better fit for thicker and thinner oxides, respectively. The measured and simulated accumulation gate current characteristics with the extracted  $T_{ox}$  are reproduced in Fig. 6. At moderate to high gate voltages, the simulation matches the experimental curves very accurately. However, there is disagreement in the sub-0.5 V. The reason why the simulated direct tunneling currents is not seen in experimental results in the sub 0.5 V regime is not clear.

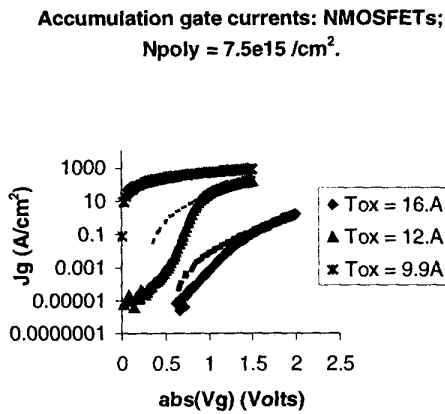


Fig 6: Simulated tunneling currents agree with the experimental data in the direct tunneling regime. In the sub-0.5 V tunneling regime, there is significant deviation.

Figs. 7(a-c) show the transfer characteristics of a 10/10 MOSFET with  $T_{ox}=9.6-13.2$  Å. As can be seen, the thin gate oxide MOSFETs show large leakage in the linear region. The drive currents are comparable to that of Ref. [8], lending more confidence to obtain mobility data from these FETs.

Fig. 8a shows that the gate currents of a 10/10 MOSFET with  $T_{ox} = 13.2$  Å decreasing with increasing drain voltage. Shown in Fig. 8b is the gate IR drop of MOSFETs with  $T_{ox} = 13.2$  Å. The minimum L (0.1  $\mu m$ ) transistors have a smaller IR drop because the measured gate currents are small in these devices apparently due to a larger  $T_{ox}$ . The small IR drop, and the large ratio of the drain to gate currents in short channel transistors suggest that tunneling may not adversely affect performance in reduced gate length transistors. This observation was also reported by Momose et al [8].

The electron mobility was computed from  $I_d$ - $V_g$  data by taking into account the effect of quantization and poly depletion on the inversion charge. Fig. 9 shows the electron mobility to increase with increasing inversion charge, which points to a coulombic scattering mechanism. The mobility was lower for a higher poly doping. Fig. 10 shows the electron mobility to decrease super-linearly with  $T_{ox}$  for the same poly doping.

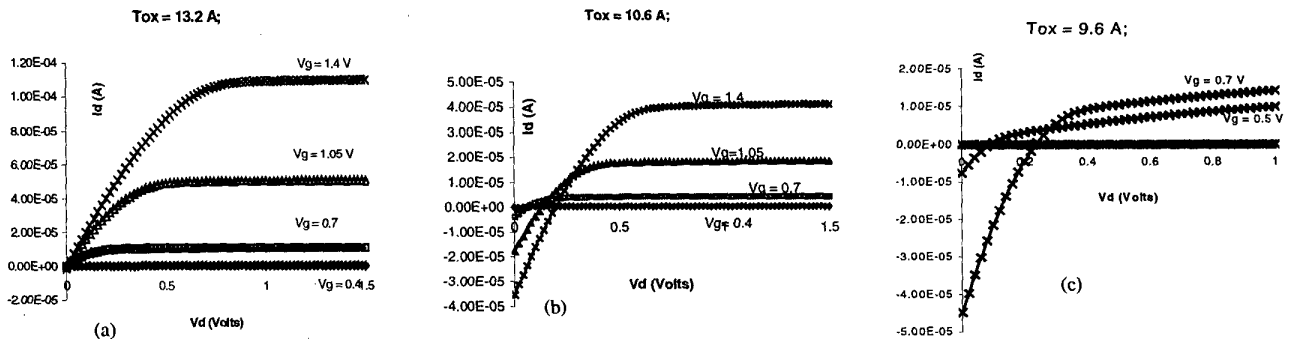


Fig. 7: Transfer characteristics of ultra-thin gate oxide MOSFETs:  $T_{ox}$ : 9-13 Å L/W drawn lengths of 10/10  $\mu m$ .  $N_{poly} = 2e20 /cm^3$ .

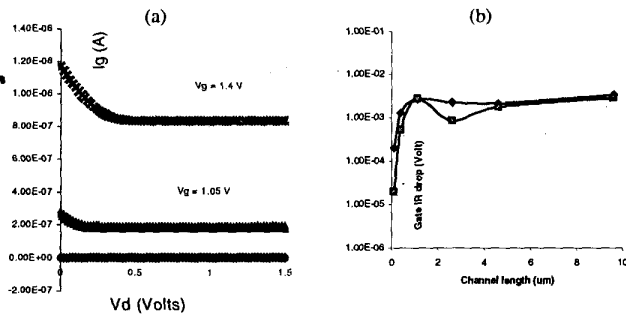


Fig. 8: Gate currents decrease with increasing drain voltage and therefore may be not be significant in the saturation region. Squares and diamonds in Fig. 8b represent saturation and linear regions, respectively. The measured gate IR drop is negligible in short channel transistors ( $L=0.1 \mu\text{m}$ ).

Fig. 11 shows the dependence of electron mobility on poly doping. The CV curves for different poly doping (fig. 2) show the same capacitance in the depletion region, suggesting that the substrate doping is the same for all the different poly doping. Hence, we interpret the mobility dependence on poly doping and  $T_{ox}$  as that arising out of RCS. The super-linear decrease of mobility with  $T_{ox}$ , and its dependence on poly doping is explained with our theory for RCS [4]. Also, the mobility is insensitive to poly doping beyond  $6 \times 10^{19} / \text{cm}^3$  (Fig. 11). This is also consistent with the model we developed for RCS [4]. Note that if RCS were eliminated, mobility would be doubled.

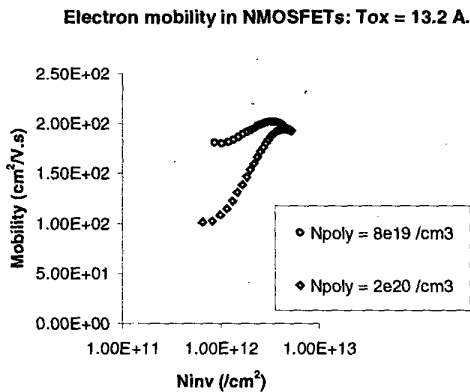


Fig. 9: Mobility curves for electrons in MOSFETs with different poly doping. Mobility increasing with increasing inversion charge is a signature of coulombic scattering, and hence ionized impurity scattering.

### Conclusion

In this work, we have fabricated NMOSFETs with gate oxides between 9-15 Å. We have introduced an improved methodology for extracting  $T_{ox}$  based on MOSFET accumulation tunneling currents that is simple and convenient to at least 9 Å. We have found experimental evidence for the presence of remote charge scattering, an effect that was only theoretically predicted before. The electron mobility data for 9-13 Å  $T_{ox}$  MOSFET are

presented. We infer that mobility may be the main limitation in gate oxide scaling down to the 9 Å regime.

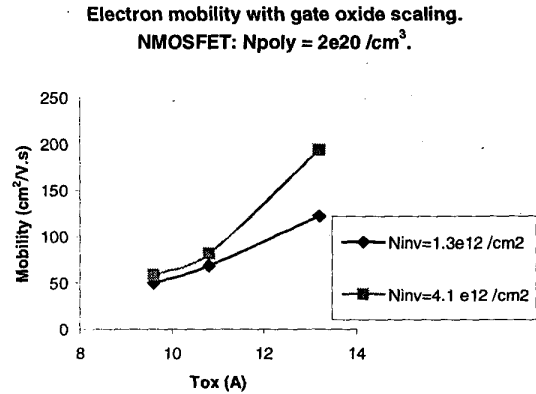


Fig. 10: The measured electron mobility is seen to decrease exponentially with  $T_{ox}$  at a given poly doping concentration.

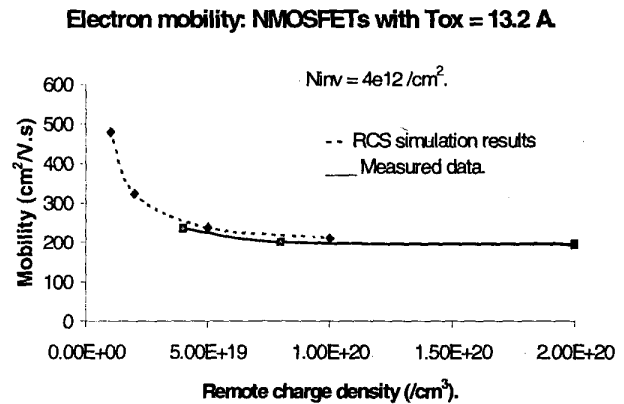


Fig. 11: The dependence of mobility on remote charges (poly doping) confirms RCS. Simulation predicts the RCS mobility to be insensitive to poly doping beyond  $6 \times 10^{19} / \text{cm}^3$ . This agrees well with the experimental data.

### References

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