A Bulk-Si-compatible Ultrathin-body SOI Technology for sub-100nm MOSFETs

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Introduction

Scaling of MOSFET technology to 0.05μm and beyond poses considerable challenges to conventional MOSFET structures. The heavy doping required to provide adequate short-channel effect (SCE) suppression results in degraded mobility and enhanced junction leakage. Simulations show that a promising structure that suppresses SCE without using a heavily doped channel is the ultrathin-body SOI MOSFET [1].

A difficulty associated with the fabrication of ultrathin-body SOI MOSFETs is the formation of the thin Si film, the thickness of which is typically less than 30% of the channel length, necessitating thicker source and drain films to reduce resistance. In etch-back or oxidation-thinning processes, the uniformity of the body thickness is limited by the thickness uniformity of the starting SOI layer. A deposited channel film is therefore desirable to provide adequate thickness uniformity. An additional advantage of a deposited channel technology is the potential incorporation of the same into a bulk CMOS process, enabling the use of SOI and bulk devices on a single chip.

We report on an 80nm gate length ultrathin-body SOI NMOSFET that is formed in deposited and laterally crystallized amorphous Si. This approach offers the advantage of having excellent body thickness uniformity, and results in excellent off-state behavior, validating the ultrathin-body MOSFET design.

Experimental Details

Figure 1 shows the process flow used. Devices were fabricated on mesa-isolated SmartCut™ wafers having a 50nm thick SOI layer on a 400nm buried oxide. The SOI layer was etched away completely except for the S/D islands, and 20nm amorphous silicon was deposited. Native oxide between the SOI layer and the amorphous silicon was broken up using a Si+ amorphizing implant. Implant parameters were chosen to ensure displacement of every atom at the α-Si / SOI interface. The films were then crystallized at 550°C, resulting in epitaxial growth, as evidenced by RBS on vertically crystallized 160nm a-Si films deposited on Si substrates, inset in figure 1.

Next, device islands were patterned. A 2.5nm SiO_2 gate dielectric was grown, and an *in-situ* n+ polysilicon gate was deposited. The gate was patterned and source / drain junctions were formed. Finally, contact formation and metallization were completed. Minimum L_{drawn} was 80nm, resulting in an extracted L_{eff} of approximately 75nm.

Results and Discussion

Good leakage behavior is evident in fig. 2. The poor on-current (fig. 3) is explained by the low thermal budget (800°C/2min activation), resulting in high series resistance. Because the source / drain islands both served as seeds for growth, a twin boundary exists in the channel. The excellent SCE immunity is shown in figure 4. While this may be attributed to the ultrathin body, it may be partially due to the twin boundary.

Evidence of lateral epitaxy is obtained by examining performance distributions. Poly-Si channels result in performance variations due to variations in the number of channel grains. The drive- and off-current distributions of these devices were compared to those of similarly fabricated poly-Si devices (Fig. 5). The tighter distributions are evidence of lateral epitaxy. A similar analysis for larger devices (Fig. 6) confirms epitaxy over 0.4μm distances.

To understand the effect of the twin boundary, the activation energy of the barrier as a function of gate bias is extracted and compared to that of a poly-Si FET (Fig. 7). The asymptotic value of the activation energy at high bias is representative of the effect of the twin boundary on mobility [2]. Clearly, the SPE-FET activation energy is smaller than that in a Poly-Si FET and hence will have a smaller effect on mobility. Additionally, since the use of a silicon implant has been found to be crucial to the removal of the native oxide, a masked implant can potentially be used to ensure growth from one side of the device only, eliminating the twin boundary within the channel.

Conclusions

A novel method of forming ultrathin-body SOI MOSFETs has been presented. Lateral solid-phase epitaxy of a deposited amorphous film was used to provide excellent controllability over 20nm body thickness, resulting in good uniformity of device characteristics. The ultrathin body provides good SCE suppression. Further optimization should enable fabrication of high-performance devices using a technology compatible with on-chip bulk devices.

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References

[1] B. Yu *et al*, Proc. 1997 International Semiconductor Dev. Res. Symp., Dec. 10-13, Charlottesville, VA, pp. 623.
[2] J. Levinson *et al*, J. Appl. Phys., vol. 53, pp. 1193, 1982.

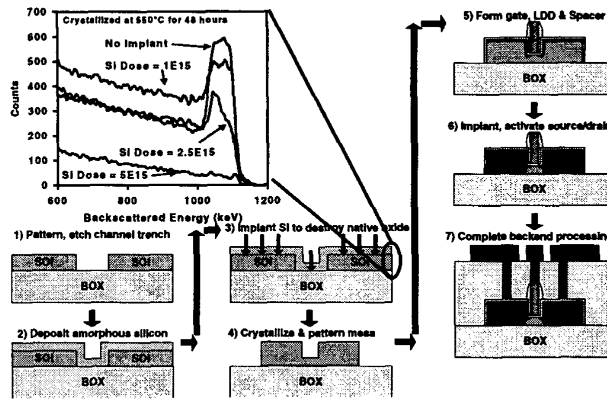

Fig 1: Process flow for fabrication of ultrathin-body MOSFET (Inset: RBS spectra showing effect of Si implant on crystallinity

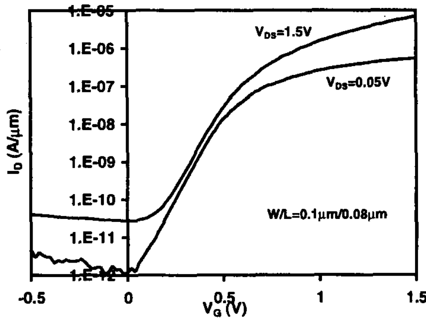

Fig. 2: Transfer characteristics of ultrathin-body NMOSFETs.

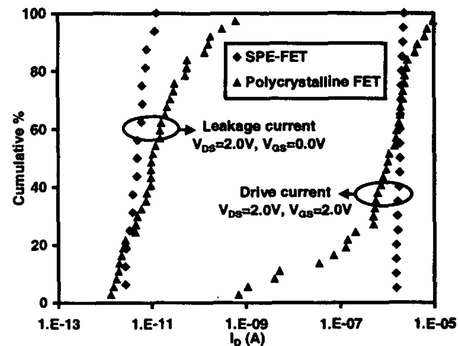

Fig. 5: Distribution of drive-current and leakage current in SPE-FETs and polycrystalline FETs (W/L=100nm/80nm)

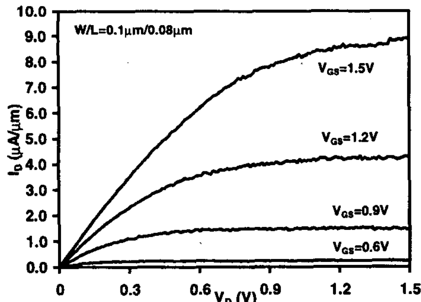

Fig. 3: Output characteristics of ultrathin-body NMOSFETs

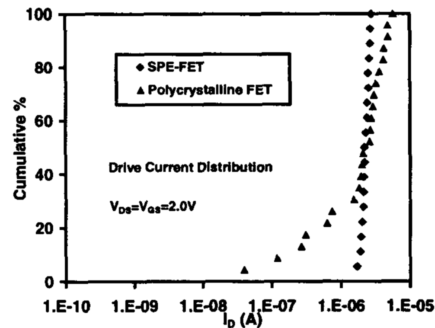

Fig. 6: Drive-current distribution in SPE-FETs and polycrystalline FETs (W/L=0.4μm/0.4μm)

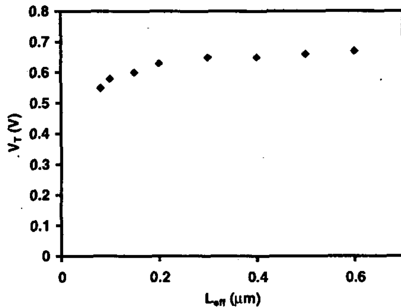

Fig. 4: V_T rolloff for ultrathin-body NMOSFETs

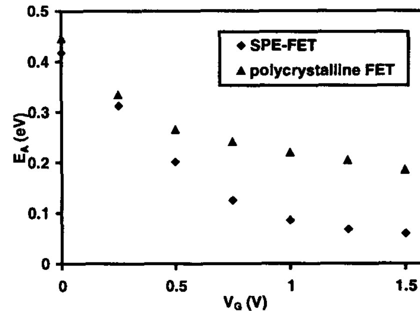

Fig. 7: Comparison of drain current activation energy in SPE-FET and polycrystalline FET (W/L=0.4μm/0.4μm)