

Impact of Velocity Overshoot, Polysilicon Depletion, and Inversion Layer Quantization on NMOSFET Scaling

Michael Orshansky, Dennis Sinitzky, Paul Scrobohaci*, Jeffrey Bokor, and Chenming Hu

211-121 Cory Hall #1772, Dept. of EECS, University of California at Berkeley,
Berkeley, CA, 94720, FAX: (510) 643-2636, E-mail omisha@eeecs.berkeley.edu

* TMA Corp., Sunnyvale, CA

The impact of electron velocity overshoot on MOSFET scaling is investigated. The calibration of a 2-D device simulator MEDICI to experimental data is first described. Then, NMOS scaling trends are studied using the calibrated simulator. Inversion layer quantization effect as well as polysilicon gate depletion are taken into account and shown to have a significant impact on NMOS current drive. The results show that velocity overshoot will allow the continued enhancement of the NMOS current drive, despite the scaling of power supply voltages.

Simulator Calibration

As MOSFET size scales in the sub-quarter micron regime, electron velocity overshoot becomes an important factor in enhancing the device current drive. Due to high electric field gradient in a short channel device, electron velocity can exceed the saturation velocity value yielding current drive higher than that predicted by conventional models and simulators. This high current drive was observed at room temperature in [1]. A direct observation of electron velocity overshoot using special devices with the nominally uniform field in the channel was done in [2].

Recently, several 2-D device simulators that incorporate velocity overshoot effect by solving energy-balance equations appeared [3, 4]. These simulators, however, require that the velocity overshoot parameters of these simulators, such as energy relaxation time, be calibrated to match the experimental data. The amount of velocity overshoot is very sensitive to the channel electric field profile, therefore the simplest - uniform - profile is desired. The thick oxide devices, such as used in [2], are the ideal candidates for such calibration. By applying a gate voltage that is much larger than a drain voltage, and due to very thick oxide, a uniform tangential field is produced.

The simulator has been calibrated by matching it to the experimental data from four test devices with channel lengths (0.43 μm , 0.33 μm , 0.23 μm , and 0.13 μm). The oxide thickness is 500 \AA and the uniform doping in channel is $2 \times 10^{17}/\text{cm}^3$. Saturation velocity was found to be 8×10^6 cm/sec, as determined by the experimental measurements [2], and was used as a universal parameter. The best fit is obtained with the energy relaxation time parameter set to 0.32 ps, and further used universally.

For $L_{\text{eff}}=0.33$ and 0.43 μm , the conventional drift-diffusion and energy balance (i.e. velocity overshoot) simulation results agree closely, drift-diffusion yielding only very slightly lower currents. The difference is drastic, however, for the case of $L_{\text{eff}}=0.13$ μm . In this case, the "energy balance" simulation agrees well with the experiment, but the drift-diffusion simulation yields a substantially lower current. The reason is that electron velocity overshoot is more important in shorter channel devices. Thus, the conventional drift-diffusion model becomes inadequate for the accurate prediction of the device characteristics.

Device Scaling

Device scaling trend was studied using the calibrated MEDICI simulator. For thin oxide devices polysilicon depletion and inversion layer quantization effects start to significantly influence current drive. To take these effects into account, a silicon region doped with $3 \times 10^{19}/\text{cm}^3$ phosphorus was defined on top of gate oxide, and a gate electrode on top of that silicon region. Polysilicon gate depletion can be modeled with the depletion of that silicon region [6]. The inversion layer thickness was calculated using a coupled Poisson/Schrödinger equation solver that incorporates full Si band structure [7]. The average inversion layer thickness x_{inv} corresponds to $\epsilon_{\text{ox}} x_{\text{ox}} / \epsilon_{\text{Si}}$ extra gate oxide thickness, and reduces current drive. Note that although x_{inv} decreases as L scales down due to the increase of the electric field in the gate oxide, the fraction $x_{\text{inv}}/L_{\text{ox}}$ slightly increases, which makes inversion layer capacitance contribution increase.

A notable difference (up to 9%) between the drift-diffusion simulation with and without poly depletion and quantized inversion layer capacitance is observed. Thus, velocity overshoot would be hard to experimentally observe and match to the analytical model without accounting for poly depletion and inversion layer quantization. The energy-balance simulation predicts a substantially higher current drive for future technologies. The difference between drift-diffusion and energy balance (i.e. with velocity overshoot) results increases from 10-15% for sub-0.25 μm technologies to 35-45% for sub-0.1 μm . Moreover, although drift-diffusion simulation predicts a slight current drive degradation due to V_{dd} reduction, current drive still improves due to velocity overshoot. The amount of improvement due to velocity overshoot is a very strong function of series resistance. Not only current degrades with R_s , but also the ratio of energy balance to drift-diffusion currents. Also, the output resistance is somewhat degraded.

Reference:

1. G. G. Shahidi et al, "Electron Velocity Overshoot at Room and Liquid Nitrogen Temperatures in Silicon Inversion Layers", *IEEE Electron Device Lett*, vol. 9, no. 2, p.p. 94-96, February 1988.
2. F. Assaderaghi et al, "Saturation Velocity and Velocity Overshoot of Inversion Layer Electrons and Holes", in *IEDM Tech. Dig.*, p.p. 479-482, 1994.
3. ATHENA manual, Silvaco Inc., 1996.
4. MEDICI v. 2.0 manual, TMA Inc., 1994.
5. W. S. Choi et al, "Simulation of Deep Submicron SOI N-MOSFET Considering Velocity Overshoot Effect", *IEEE Electron Device Lett*, vol.16, p.p. 333-335, July, 1995.
6. K. Schuegraf et al, "Ultra-thin Silicon Dioxide Leakage Current and Scaling Limit", *Symp. VLSI Techn. Dig.*, pp. 18-19, 1992.
7. H. Fujioka, "Manual for 2-Dimensional Electron/Hole Gas Simulation Software", U.C.Berkeley, 1996.

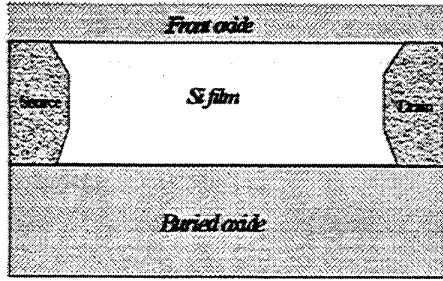


Fig. 1. SOI structure with thick front oxide is used to make tangential electric field uniform. This is necessary for 2D simulator calibration.

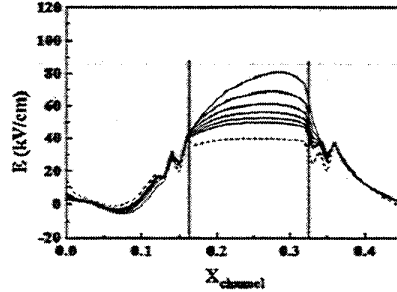


Fig. 2. The tangential electric field along the channel with V_g varying. At high V_g the field is close to linear.

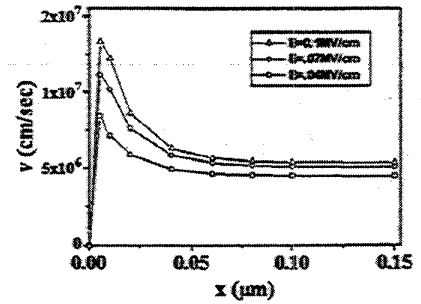


Fig. 3. Velocity can transiently overshoot the saturation velocity significantly.

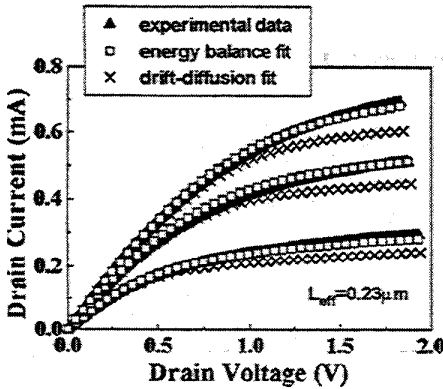


Fig. 4. Energy balance simulation agrees well with the experimental data. Energy relaxation time is 0.32ps. RMS error of fit is 0.54 %.

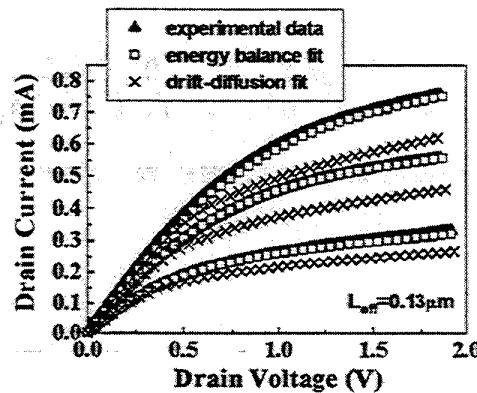


Fig. 5. Drift-Diffusion simulation significantly differs from experimental data while energy balance simulation is accurate. RMS error of fit is 0.35 %.

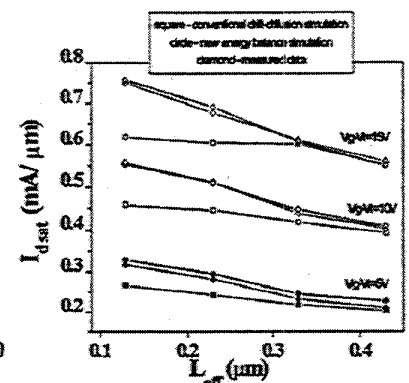


Fig. 6. As L_{eff} decreases Drift-Diffusion simulation differs more from Energy Balance simulation and measurement data.

Minimum Feature Size (μm)	5	35	25	.18	.13	.09	.06
Power Supply Voltage, V_{dd} (V)	5.0	3.3	2.5	2.0	1.8	1.5	1.2
MOSFET Gate Oxide, T_{ox} (Å)	140	85	55	40	38	30	25
Threshold Voltage V_t (V)	.7	.5	.45	.4	.4	.35	.30
Series Resistance R_s, R_d ($\Omega \mu\text{m}$)	550	500	450	410	380	350	320
Inversion layer Thickness x_{inv} (Å)	19	18	15	14	13	12	11

Table 1. Parameters for different technology generations. The parameters are estimated using the SIA roadmap. Inversion layer thickness is extracted from quantum-mechanical simulation.

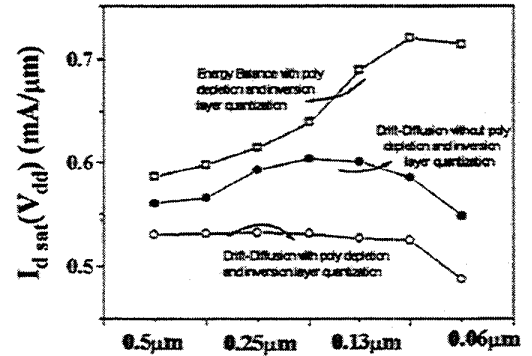


Fig. 7. Drift-Diffusion simulations, with and without poly depletion and quantization, significantly under-predict the future saturation current drive.

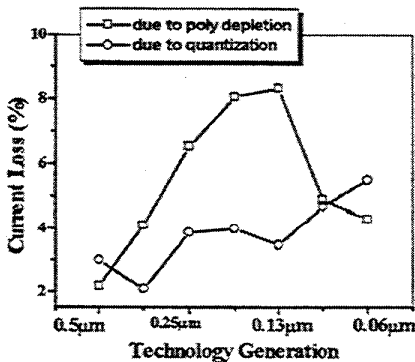


Fig. 8. Current loss due to poly depletion and inversion layer quantization effects.

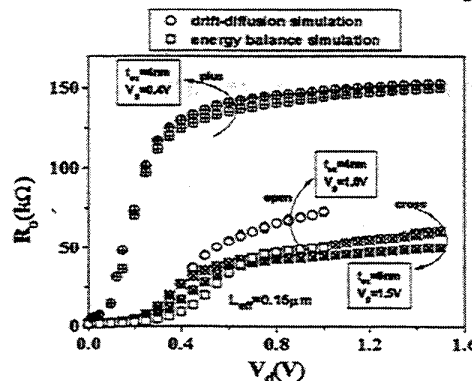


Fig. 9. R_{out} is degraded as a result of velocity overshoot.

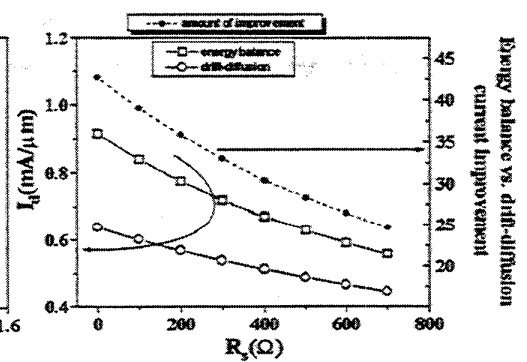


Fig. 10. Current drive improvement due to velocity overshoot diminishes as R_s increases.