High Field Hole Velocity and Velocity Overshoot in Silicon Inversion Layers

Dennis Sinitsky, Fariborz Assaderaghi, Chenming Hu, and Jeffrey Bokor

Abstract—**We report measurements of the drift velocity of holes in silicon inversion layers. The saturation velocity of holes at 300 K is found to be strongly dependent on the effective vertical field. No hole velocity overshoot was observed down to 0.16-μm channel length at room temperature. At 77 K, hole velocity saturation is much less pronounced, and a 10% higher average velocity is observed for 0.16-μm channel length as compared to 0.36-μm channel length.**

I. Introduction

As DEVICE size shrinks into the deep submicron regime, the saturation velocity of holes starts to play a significant role in P-MOSFET performance [1]. Quantitative measurements of high field carrier drift velocities in inversion layers are hard to make, due to the difficulty of achieving uniform carrier density and tangential electric field along the channel. There have been attempts to measure hole saturation velocity in the past using resistive gate MOSFET structures [2], [3]. Although high uniform tangential fields could be achieved using resistive gate scheme [3], the device channel length could not be scaled into the deep submicron regime due to presence of two gate contacts that define the voltage drop across the resistive gate. Hence, the examination of nonstationary effects could not be performed.

We employ a modification of a method first introduced in [4], which has already been used to study high field transport of electrons in Si inversion layers [5], [6]. The technique employs a short channel device with a very thick gate oxide (about 56 nm), as shown in Fig. 1(a). By applying rather high gate-to-source voltage $V_{\rm gs}$ (10–30 V) as compared to the drain-to-source voltage $V_{\rm ds}$ ($\sim$2 V), we obtain a reasonably uniform electric field in the channel as verified by the two-dimensional (2-D) device simulator MEDICI 2.0 [7]. Transport parameters in MEDICI were carefully calibrated to show agreement between experimental and simulated I_d–$V_{\rm gs}$ and I_d–$V_{\rm ds}$ curves (here I_d is the drain current). The uniformity of the field is enhanced in our case since we use an SOI substrate. By applying positive voltage on the back side, since the Si film thickness $T_{\rm Si} < 2x_{d\max}$ (the maximum depletion length in Si), the film is fully depleted, and the

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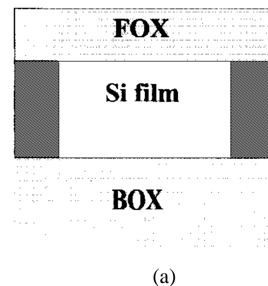
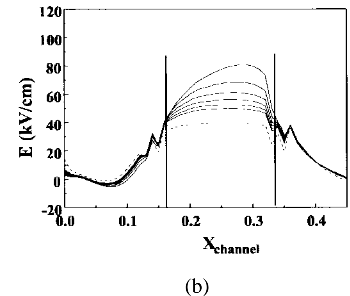


(a)



(b)

Fig. 1. (a) Test structure for hole velocity measurement, and the simulated tangential field along the channel for a 0.16-μm device. FOX and BOX stand for front and back gate oxide. The dark colored areas denote source/drain implanted regions. (b) $V_{\rm gt}$ =5–30 V in 5 V steps (solid lines), and 100 V (dashed line) for an electric field plot. The vertical lines denote the metallurgical junction positions. The higher fields correspond to the lower $V_{\rm gs}$'s because of smaller V_d loss due to series resistance. Since holes show almost no velocity overshoot, drift-diffusion option was used.

depletion charge is constant along the channel. This minimizes threshold voltage variation along the channel. We make sure that back-gate current is negligible compared to front-gate current when we do measurements. Channel field and carrier velocity are determined by using the following formulas [5]: $E = (V_d - 2I_dR_s)/L_{\rm eff}; v = I_d/WC_{\rm ox}(V_{\rm gs} - V_t)$, where R_s is source series resistance.

The results of simulations are shown in Fig. 1(b), which plots the tangential electric field versus the coordinate along the channel, with $V_{\rm gs}$ as a parameter. Note that Fig. 1 corresponds to the worst case scenario of the highest $V_{\rm ds} = 2$ V and the shortest PMOS $L_{\rm eff} = 0.16$ μm. The bumps in channel electric field at the edges of the device are due to gate oxide fringing field and p-n junction field variation. The measurement error for the highest drain bias case can be estimated as follows. The change in channel electric field is about 50–25% for $V_{\rm gs} - V_t(\equiv V_{\rm gt})$ of 10–25 V. Even for the case of extremely large $V_{\rm gt}$ of 100 V there is still unavoidable 10% field variation from source to drain. The field we extract is the average field and it is within $50/2 \sim 25\%$. In the case of $V_{\rm gt} = 5$ V a larger channel electric field variation of 90% is observed. The error in v however is smaller: $\frac{\Delta v}{v} = \frac{\Delta E}{E}\frac{dv/dE}{v/E}$. The second term in the product is about 30% for the highest $V_{\rm ds}$. This is because of the nonlinearity in the v-E curve because of velocity saturation, as can be seen from Fig. 2. Hence, in case of $V_{\rm gt} = 10$ V, the error in v is $.25 * .3 \sim 8\%$

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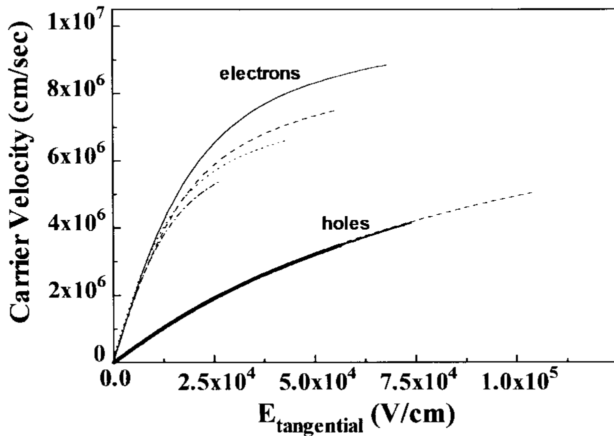

Fig. 2. Measured velocity-tangential field curves at room temperature; $E_{\text{eff}} = 0.55$ MV/cm. The electron velocity-field curves from [6] are plotted on the same y-axis as holes for comparison. The effective channel lengths for PMOS devices are 0.16, 0.26, and 0.36 μm; for NMOS devices—0.12, 0.18, 0.22, and 0.38 μm. Shorter devices extend to larger tangential fields and, in case of electrons, yield higher velocity.

for the highest tangential field. For $V_{\text{gt}} = 5$ V, the error in v is about 14%.

The carrier velocity and field extraction are straightforward and discussed in [5] and [11]. For very short devices (0.2 μm and below), V_t versus V_{ds} correction for Drain Induced Barrier Lowering (DIBL) must be performed. This is accomplished by checking the parallel shifts in the subthreshold current versus V_{ds} [8], which give the V_t versus V_{ds} dependence.

II. Device Fabrication

The p-channel MOSFET's were fabricated on a single SIMOX wafer using mesa isolation. The gate oxide thickness was 56 nm, the buried oxide thickness was 400 nm, and the Si film thickness was 130 nm. Channel doping was about $2.5 \times 10^{17}/\text{cm}^3$, roughly uniform. The photoresist ashing technique was used to define deep submicron gates [9]. A 20 KeV boron implant with dose $5 \times 10^{15}/\text{cm}^2$ into the source/drain and gate was used, resulting in p$^+$-poly PMOS devices. Devices down to 0.16 μm L_{eff} without significant punchthrough were successfully fabricated. The source/drain series resistance at room temperature was measured to be 1.72 kΩ-μm. Since the measured hole mobility versus E_{eff} agreed well with the universal mobility-vertical field relation for holes [1], we conclude that the quality of Si film and Si/SiO_2 interface was satisfactory.

III. Results and Discussion

Fig. 2 shows velocity-tangential field curves for devices with L_{eff} ranging from 0.36 to 0.16 μm. All the curves overlap perfectly, in contrast to analogous electron velocity-field curves from [6], which show higher average velocity for shorter devices. Thus no hole velocity overshoot is observed at these channel lengths, although electron velocity overshoot clearly occurs [5], [6]. Note that the hole velocity shown reaches 5.5×10^6 cm/s and is only just beginning to saturate even for tangential field as high as 0.1 MV/cm. This indicates a rather high value of saturation velocity for holes, in fact, comparable to v_{sat} of electrons.

TABLE I
Extracted and Measured Parameters for Velocity-field Curves of Holes at Room Temperature. The Extraction of v_{sat} Is Based on the Assumption That $\beta = 1$

E_{eff}(MV/cm)	μ (cm²/V·sec)	v_{sat}(x10⁷cm/sec)	v@0.1MV/cm
0.40	105	1.35	0.55
0.55	93	1.06	0.47
0.70	83	0.97	0.42
0.85	75	0.86	0.37
1.0	67	0.79	0.34

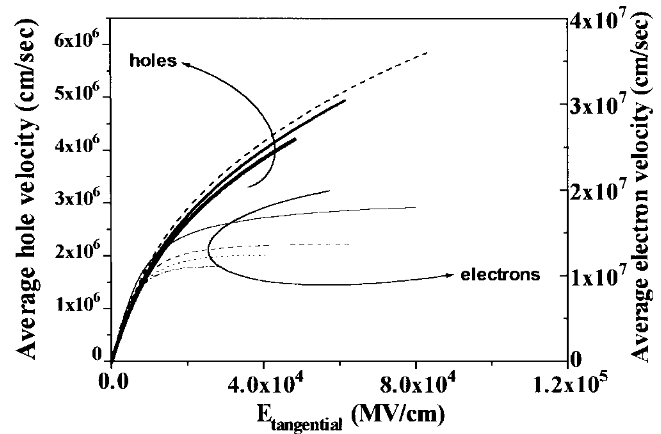

Fig. 3. Measured velocity-tangential field curves at 77 K along the left y-axis; $E_{\text{eff}} = 0.55$ MV/cm. The electron velocity-field curves at 85 K from [6] are plotted on the same graph along the right y-axis for comparison. Electron velocity overshoot is much stronger for electrons than holes. The effective channel lengths for PMOS devices are 0.16, 0.26, and 0.36 μm; for NMOS devices— 0.12, 0.22, 0.32, and 0.42 μm. Shorter devices extend to larger tangential fields and yield higher velocity.

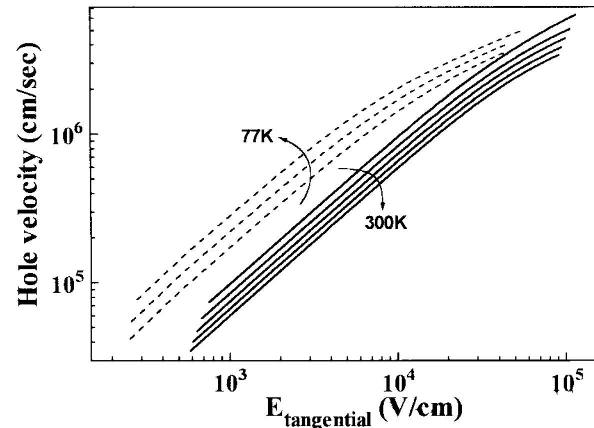

Fig. 4. The measured velocity-tangential field curves at both room and liquid nitrogen temperatures for different effective vertical fields for inversion layer holes. For low temperature data, E_{eff} increases from .4 to .7 MV/cm in .15 MV/cm steps. For room temperature, E_{eff} increases from .4 to 1 MV/cm in .15 MV/cm steps. The lower velocity corresponds to the higher E_{eff}.

Fig. 3 shows velocity-tangential field curves for the same devices at 77 K (and 85 K for electrons from [6]). The average velocity in the high tangential field regime is higher for $L_{\text{eff}} = 0.16$ μm than for $L_{\text{eff}} = 0.36$ μm. We attribute this to a slight velocity overshoot of holes at 77 K. Electrons

exhibit much higher velocity overshoot at 85 K than holes at 77 K. The amount of velocity overshoot of electrons was found to be correlated with carrier mobility [10], [11]. At 77 K the hole mobility is comparable to the electron mobility at room temperature, but the amount of velocity overshoot is much smaller. The reason is that the origin of carrier velocity overshoot is dependent upon the interrelation between momentum and energy relaxation rates.

Fig. 4 shows dependence of hole velocity on the vertical effective field. This data was fitted to Thornber's equation [12]: $v = \mu E/(1 + (\mu E/v_{\rm sat})^{\beta})^{1/\beta}$. These fits are essential for modeling hole transport in 2-D device simulations. For holes, at 300 K, β is assumed to be 1, as verified in [12] and [13]. Fitting parameters $v_{\rm sat}$ and μ as well as velocity v at 0.1 MV/cm are presented in Table I. Note that the fitting parameter μ agrees closely with long-channel mobility measurement. Fitted $v_{\rm sat}$ is substantially higher than measured velocity at 0.1 MV/cm, and higher than the previously reported value in [2]. From velocity-field plot in [3] it can be seen however that $v_{\rm sat}$ of [3] agrees well with $v_{\rm sat}$ extracted in our measurements. Data presented in [3] also shows strong dependence of $v_{\rm sat}$ on $E_{\rm eff}$ for holes.

Since the critical field for holes is much higher than for electrons, no data on hole velocity far beyond $E_{\rm crit}(= v_{\rm sat}/\mu)$ is available. However holes at fields lower than $E_{\rm crit}$ and electrons at fields both lower and higher than $E_{\rm crit}$ follow Thornber's equation, so we extrapolate it for holes at fields higher than $E_{\rm crit}$ as well.

We find an appreciable dependence of $v_{\rm sat}$ parameter for holes on $V_{\rm gs}$ and $E_{\rm eff}$. As $E_{\rm eff}$ changes from 0.4 to 1 MV/cm, the extracted $v_{\rm sat}$ decreases by about 40%. This is similar to electrons [11], although dependence for holes is stronger. Strong dependence of $v_{\rm sat}$ on $E_{\rm eff}$ agrees with experimental findings of [3] as well.

IV. Conclusion

In this paper the high field transport parameters of holes at room and liquid nitrogen temperature were studied. A rather strong dependence of $v_{\rm sat}$ on $E_{\rm eff}$ was observed. No velocity overshoot was observed at 300 K down to 0.16 μm channel length. A slight velocity overshoot of holes was observed at 77 K. The smallness of the effect limits the application of hole velocity overshoot in P-MOSFET's.

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