Fabrication of planar silicon nanowires on silicon-on-insulator using stress limited oxidation

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A new method is proposed for the fabrication of planar single crystal silicon nanowires down to 8 nm in diameter. In this method silicon lines are defined on silicon-on-insulator with electron beam lithography followed by a metal liftoff process and a silicon plasma etch. Low temperature oxidation is then used to shrink these lines to a sub-10 nm diameter. Normal stress generated by the expansion of the viscous oxide during oxidation eventually stops the reaction, leaving a small silicon core at the center of the line. The effect of the crystallographic orientation of the line and the stress complications caused by the substrate are investigated. © *1997 American Vacuum Society.* [S0734-211X(97)04706-9]

I. INTRODUCTION

There is a strong interest in the fabrication of silicon nanostructures for microelectronic applications. As silicon devices shrink in size quantum effects become increasingly important. To experimentally measure these effects it is necessary to fabricate silicon structures that have critical dimensions on the order of an electron wavelength. One of the simplest structures where quantum effects dominate is the one-dimensional nanowire. Due to their versatility silicon nanowires promise to be an important component of future quantum devices. In addition to their device potential, the study of electron behavior in these structures can yield important information about quantum conduction,[1] ballistic transport, Coulomb blockades,[2] and other quantum effects.

A preliminary step to the investigation of quantum effects in single crystal silicon nanowires is the fabrication of such wires with a sufficiently small diameter. Many methods for the fabrication of single crystal nanowires, which exhibit quantum conductance at low temperatures, have been proposed.[3] However, it would be desirable to make silicon wires that exhibit quantum effects at room temperature. The fabrication of such wires presents a serious technological challenge, since such wires would have to have a diameter of less than 4 nm.

Silicon pillars down to 2 nm in diameter have already been successfully fabricated using stress-limited oxidation.[4,5] However vertical pillars are hard to integrate into a traditional planar technology and attaching contacts to such pillars is difficult. In this article, we propose a technique, which uses self-limited oxidation to fabricate horizontal silicon nanowires down to 8 nm in diameter. Using electron beam lithography, we defined the width of a silicon line on a silicon-on-insulator (SOI) wafer. These lines were then oxidized down to their final diameter using stress-limited oxidation. The advantage of this method is that the final wire diameter is not strongly dependent on oxidation time, and wires with a reproducible diameter can be fabricated.

II. FABRICATION PROCESS

Silicon nanowires were fabricated from (100) p type, separated by implanted oxygen (SIMOX), SOI wafers. Initially, the top silicon layer was thinned by oxidation to the desired thickness of 40 nm. Next, a layer of electron beam resist, PMMA (950 k 2% in chlorobenzene) was spun on at 6 krpm for a thickness of 500 Å. In order to promote resist adhesion, the wafer was dehydrated and treated with HMDS before the application of resist. The wire pattern was written using electron beam lithography. A range of doses was used to expose wires of different widths; consistently the dose of 1.25 nC/cm yielded the thinnest continuous lines. Lines 30–40 nm in width were produced repeatedly. The linewidth was most sensitive to beam focus, so to compensate for stage tilt the e-beam focus was manually adjusted between the exposure of large arrays of wires.

After development, a 200 Å layer of metal was thermally evaporated onto the resist and into the developed regions to provide a masking layer for the silicon etch. Initially chromium was used for this purpose, but due to its high tensile stress cracking it was abandoned in favor of nichrome (80% Ni, 20% Cr). Scanning electron microscopy (SEM) pictures of the deposited metal wire reveal that it has a trapezoidal cross section, with a 40 nm bottom and a 30 nm top. This profile is caused by the gradual closing up of the resist opening during the evaporation due to the lateral growth of the metal film deposited on the PMMA. The metal layer on top of the resist was lifted off by dissolving the PMMA in acetone. Five minutes of ultrasonic agitation following the 1 h acetone soak helped to ensure good liftoff. The resulting metal pattern served as a mask for an anisotropic silicon plasma etch. The etch used chlorine as its main reactive gas, and it was done at a high rf power to improve anisotropy. The erosion of the mask during the etch was sufficiently low

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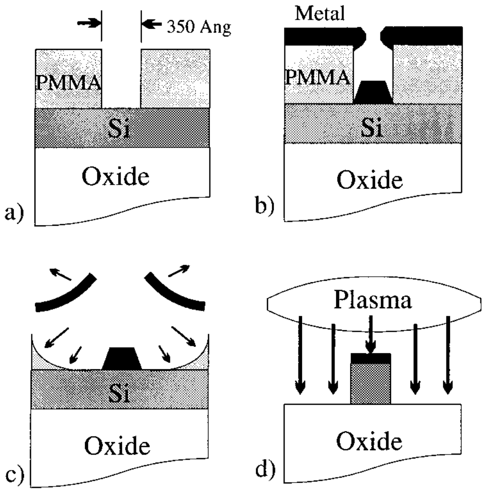

FIG. 1. Silicon nanowire fabrication process. (a) Exposure; (b) metal evaporation; (c) metal liftoff; (d) Si plasma etch.

for the silicon sidewalls to be vertical. After the etch, the metal mask was removed; nichrome was dissolved in a 3:1 mix of HCl and H_2O_2, while chromium was dissolved in a photomask etchant. Figure 1 shows a schematic cross section of the processing steps prior to oxidation.

To reach the final silicon wire diameter of under 10 nm the wires were oxidized at a low temperature. Stress generated during oxidation prevented the wires from oxidizing away completely. Since SiO_2 occupies a larger volume than Si, as the oxidation progresses newly formed inner oxide layers tend to push the older oxide layers further out. At low temperatures the high viscosity of the SiO_2 makes this radial plastic deformation of the outer oxide layers difficult, and as a result a large normal stress is generated back toward the $Si-SiO_2$ interface. Figure 2 shows a schematic diagram of the oxide stress fields during a radially symmetric oxidation.

Normal stress at the silicon interface slows the oxidation rate by making the transition of Si to SiO_2 less energetically favorable. Eventually, at a certain wire radius, oxidation slows down to an insignificant rate, leaving behind a thin silicon core. Liu *et al.* have demonstrated that silicon pillars between 2 and 16 nm in diameter can be fabricated using stress-limited oxidation.[5]

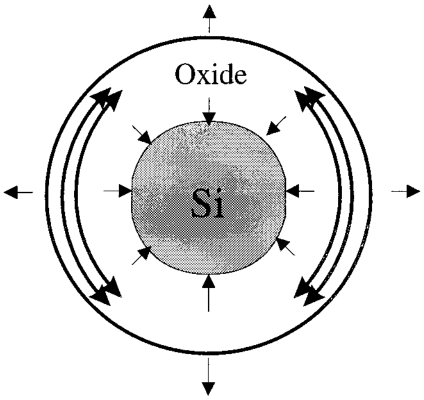

FIG. 2. Stress profile in a radially symmetric oxidation. Lower radius of curvature of the core produces more interface stress.

The anisotropic oxidation rates of single crystal silicon further complicate the oxidation profile. In the planar geometry the (111) crystal plane oxidizes the fastest, followed by the (110) plane, and the (100) plane. The difference in these oxidation rates modifies the stresses generated and makes the postoxidation profile depend on the crystallographic orientation of the wire.

The presence of a substrate oxide further breaks down the symmetry of the oxidation. The oxide supporting the wire hampers oxygen diffusion and enhances the stress effects at the bottom of the wire. During oxidation the supporting oxide constrains the expansion of the SiO_2 layer generated at the bottom of the wire and reduces the amount of oxygen available; since no such effect is present at the top or sides, the oxidation of the bottom proceeds slower. To remove this effect, the silicon wires were undercut from the supporting oxide using a short HF dip. With the oxide under the wires gone, the pads at the end of the wires provided mechanical support.

The oxidation was done at 875 °C for 5–7 h. This temperature was chosen because, according to the data published by Liu *et al.*,[4] it results in a 2–4 nm diameter Si core left after the oxidation of 30–40 nm pillars. Their data also indicated that the oxidation stops after 5 h, our oxidation time was at least that much to ensure that the oxidation had run its course. Following the oxidation a 20 min anneal was used to improve the quality of the silicon–oxide interface.

Since the wires are still freestanding after the oxidation, they are too fragile for transmission electron microscopy (TEM) cross section preparation. We reinforced the wires by evaporating a 100 nm nichrome layer onto the wafer. Nichrome was chosen due to its low inherent stress and high TEM contrast to the oxide.

III. RESULTS

Both the preoxidation and postoxidation profile of the wires were investigated using transmission electron microscopy. Figure 3(a) shows the TEM cross section of a 35 nm wire before oxidation. The variation of the width and height of the wire was determined by measuring a large number of wires drawn on the same wafer. These lateral dimensions varied by ±5 nm, from wire to wire. The variation in the width is caused by changes in electron beam focus across the wafer as well as the uneven evaporation of the metal mask. Height variations can be attributed to the fluctuations in the SOI silicon layer thickness, and can be eliminated with better quality starting material.

The high TEM contrast in this and the other images demonstrates clearly that the silicon wires retain their single crystal orientation, in some micrographs the actual atomic planes are visible. The electron diffraction pattern of the silicon wire is nearly identical to that of the bulk substrate indicating that the crystallographic alignment between the wires and the wafer was maintained.

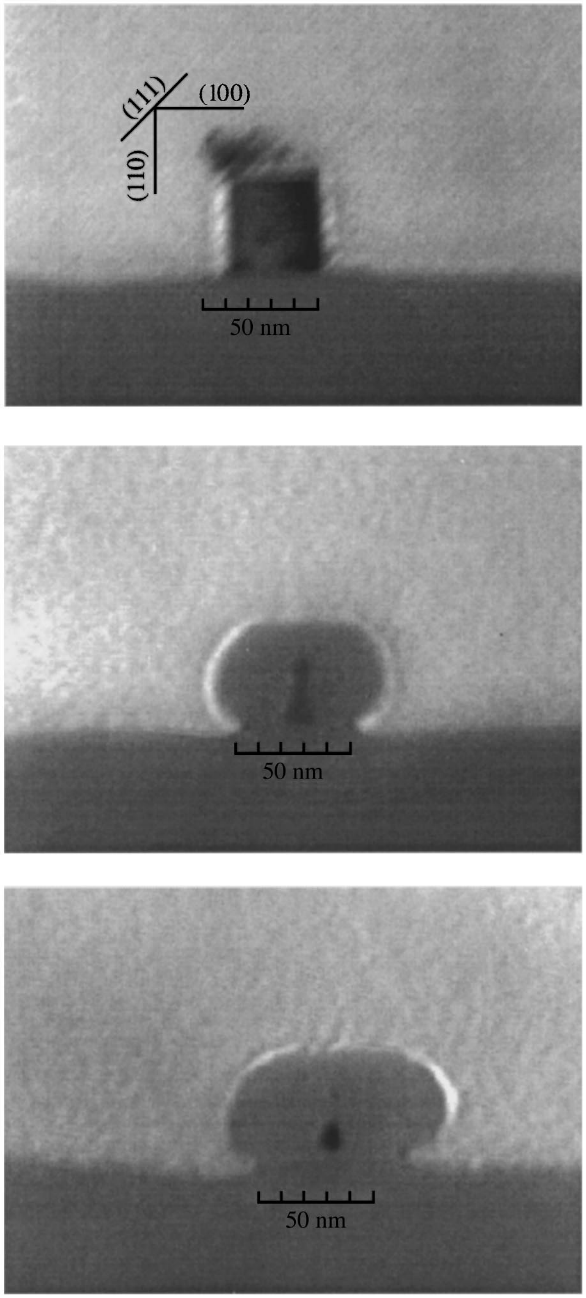

FIG. 3. TEM cross section images of the: (a) Si line before oxidation; (b), (c) Si ⟨110⟩ cores after oxidation.

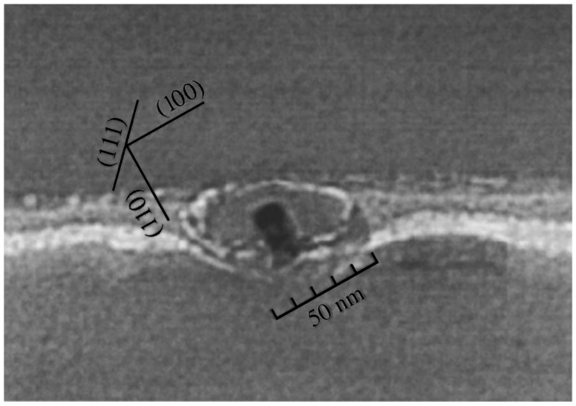

FIG. 4. TEM cross section of the fully undercut Si $\langle\overline{110}\rangle$ core after oxidation (oxide damaged during sample prep).

Figure 3(b) shows a TEM cross section of a 35 nm wire drawn along the ⟨110⟩ direction after a 5 h oxidation at 875 °C. The silicon core in this wire is 25 nm tall and 5 nm wide at the girth, about the largest obtained under these conditions. In this sample the wire was not fully freed from the substrate before oxidation, only partially undercut. As a result the bottom portion of the Si wire is thicker then the top, since the effect of the substrate slowed the oxidation at the bottom of the wire. Wires with no undercut of the supporting oxide oxidized very little from the bottom, leaving a flat core several nanometers tall but just about as wide as before the oxidation. Figure 3(c) shows a postoxidation profile of a wire that was originally slightly thinner, but had the same oxidation conditions. Here the (110) planes oxidized until they touched, pinching off an 8 nm diameter silicon wire at the bottom. Most of the wires oxidized under these conditions had a postoxidation profile between these two extremes. The typical hourglass shape of the silicon cores is due to stress retardation of oxidation at the corners. Since the corners have a shorter radius of curvature than the flat faces, they generate more stress during oxidation; eventually the oxidation of the sides overtakes the corners giving the pinched in look of the profile. Such an oxidation pattern was already observed for high aspect ratio nanowires.[1]

It is evident from the difference in the thickness of the oxide grown at the sides and at the top, that the (110) sides of the wire oxidized more then the (100) top and bottom. This is due to the faster linear oxidation rate of the (110) plane, and resulted in all the cores being taller then they are wide. It is interesting that the (111) plane did not oxidize at all, although the (111) plane has a larger linear oxidation rate than either the (110) or (100) planes. The absence of a (111) oxidation front can be understood by observing that the (111) planes were exposed only at the corners, so they were put at an initial disadvantage of having a shorter radius of curvature. As a result the oxidation of the (111) planes generated more stress then the flat (100) and (110) sides, this stress barrier was sufficiently large to slow the oxidation of the (111) planes to below that of the (100) side. Being the slowest, the (111) plane could not catch up with the other sides to develop its own facet, and therefore it does not appear in the postoxidation profile. The (111) mode of oxidation failed to appear even when the sample was initially oxidized at a high temperature of 1000 °C for 6 min, to reduce the stress effects by having a lower oxide viscosity. The introduction of a (111) facet could help to even out the aspect ratio of the cores and perhaps yield a rounder core profile.

TEM cross sections of the wires drawn in the ⟨110⟩ direction consistently indicate that the (110) plane oxidized more then twice as far as the (100). However, the measured planar linear oxidation rate difference between (110) and (100) is only 35%.[6] This suggests that the (100) linear oxidation rate has a stronger dependence on stress then the (110).

The postoxidation cross section of a ⟨110⟩ wire, which is totally freed from the substrate prior to oxidation, is shown in Fig. 4. In an attempt to introduce the (111) plane of oxidation, this sample was oxidized at 1000° for 6 min and then at 850° for 5 h. The core is about 22 nm tall and 12 nm wide. This sample was not stabilized with a metal layer after the oxidation, so the wire rotated a little and the oxide around it cracked during TEM sample preparation. However, this profile demonstrates that freeing the wire from the substrate restores the oxidation symmetry between the top and bottom.

IV. CONCLUSION

We have demonstrated that planar silicon wires down to 8 nm in diameter can be fabricated using self-limited oxidation. TEM cross sections of the wires reveal that the linear oxidation rates of the crystal planes forming the wire sides have a strong influence on the shape of the postoxidation profile. Particularly that square wires with (110) and (100) sides oxidize faster on the (110) plane, giving them a rectangular profile. In addition, the presence of a supporting oxide enhances the stress limitation effects at the bottom of the wire.

ACKNOWLEDGMENTS

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