High-Field Transport of Inversion-Layer Electrons and Holes Including Velocity Overshoot

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***Abstract*— In this paper, we experimentally address the effect of a wide range of parameters on the high-field transport of inversion-layer electrons and holes. The studied parameters include substrate doping level, surface micro-roughness, vertical field strength, nitridation of the gate oxide, and device channel length. We employ special test structures built on Silicon-On-Insulator (SOI) and bulk wafers to accurately measure the high-field drift velocity of inversion-layer carriers. Our findings point to electron velocity overshoot at room temperature, dependence of electron and hole saturation velocities on nitridation of the gate oxide, dependence of the high-field drift velocity on the effective vertical field, and relative insensitivity of electron and hole mobility and saturation velocity to moderate surface roughness.**

I. Introduction

Saturation velocity plays a significant role in MOSFET performance. This role becomes more important as the device channel length shrinks to deep-submicrometer regime. Widely used simulators employ 1×10^7 cm/s as the room-temperature saturation velocity of electrons in the inversion layer even though many direct measurements have indicated a lower value [1]–[6]. There is even a greater discrepancy for hole inversion-layer velocity, with very few experimental results available in this case. Furthermore, these "Drift-Diffusion" simulators do not take velocity overshoot into account. Recent reports have shown that this effect should not be ignored in very short devices [6]–[12]. On the other hand, "Energy-Balance" and "Hydrodynamic" simulators that can correctly simulate this effect, employ parameters (such as relaxation times) that need calibration and should be adjusted by comparison with experimental results. Using experimental results from very short-channel regular MOSFET's to calibrate these simulators is prone to error due to the complexity of field, velocity, and charge distribution in regular MOSFET's. We employ special test structures built on Silicon-On-Insulator (SOI) and bulk wafers to measure the high-field drift velocity of inversion layer electrons and holes under uniform field. Simplicity of our test structures make these data ideal candidates for calibration of "Energy-Balance" and "Hydrodynamic" simulators. Using these test structures, we report the effects of several important process and device parameters on the inversion-layer carrier velocity.

This paper is organized as follows. In Section II, the requirements for accurate measurement of high-field drift velocity of inversion-layer carriers are described. Previous measurement techniques are also mentioned and their advantages and limitations pointed out. In Section III, we explain our measurement method and provide two-dimensional device simulations to verify its principle. In Section IV, device fabrication and experimental setup are outlined. Experimental results are presented and discussed in Section V. In this section, we also offer an explanation for the cause of apparent discrepancies in past reported values. Section VI summarizes the study.

II. Measurement Requirements and Past Attempts

Uniformity of tangential field and inversion-charge concentration is necessary for the study of drift velocity of inversion-layer carriers. This condition is violated in regular MOSFET's, since inversion-charge concentration decreases from the source to drain, while tangential field increases. These variations are small in the low-field (linear) regime of MOSFET $I-V$ and can be neglected. Consequently, drain currents at low drain voltages are routinely used to determine the low-field carrier mobility (or drift velocity). Clearly, this method cannot be extended to the high-field or "saturation" regime.

The two factors leading to the variation of inversion charge are the channel voltage and the bulk charge, both of which increase from the source to drain. In [1], MOSFET's with very thick gate oxides ($\sim$1 μm) were employed, so that the gate voltage was much larger than the drain voltage. This makes the inversion charge variation due to the channel potential very small. However, the bulk charge effect becomes more severe, as this effect is proportional to the gate-oxide thickness

$$\frac{Q_{\rm nd}}{Q_{\rm ns}} \approx \frac{(V_{\rm gs} - V_t - \alpha V_{\rm ds})}{V_{\rm gs} - V_t} \quad (1)$$

where $Q_{\rm nd}$ and $Q_{\rm ns}$ represent the inversion charge at the drain and source, respectively. V_t is the threshold voltage at the

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source end, and α is given by [13]

$$\alpha = 1 + \sqrt{\frac{2\varepsilon_{\rm si} q N_a}{2\Phi_B}} \frac{0.74 + 0.84(2\Phi_B)}{1.74 + 0.84(2\Phi_B)} \frac{T_{\rm ox}}{\varepsilon_{\rm ox}} \tag{2}$$

where $T_{\rm ox}$ is the gate-oxide thickness, and other terms have their usual meanings. The second term on the right hand side of (2) is the contribution from the nonuniform body charge, and is linear in $T_{\rm ox}$. This equation can be further approximated by

$$\alpha \approx 1 + \frac{\varepsilon_{\rm si}}{\varepsilon_{\rm ox}} \frac{T_{\rm ox}}{T_{\rm dep}} \tag{3}$$

where $T_{\rm dep}$ is the depletion-layer width at the source. It is seen from (2) and (3) that to minimize the bulk-charge effect, a small $V_{\rm ds}$ should be used. This means the use of short channel length if a large tangential field is desired. Also, a very light substrate doping can be used (making the depletion layer very wide). In that case, very short channel lengths cannot be studied because of punch-through. Another way to reduce the bulk-charge effect is to apply a large reverse bias to the body. We will discuss this method in Section III.

A second method of achieving charge and field uniformity in the device was devised in [2], and further developed in [4] and [5]. This technique uses resistive-gate MOSFET's, with contacts made to both ends of the gate. The two gate voltages V_{g1} and V_{g2} are controlled separately, and can be adjusted to account for the difference between the source and drain voltages. The premise is that since the gate voltage increases from the source to drain linearly, the surface-carrier concentration becomes uniform. Note that $V_{g1} - V_{g2}$ should not be set merely to $V_{\rm ds}$, since that would ignore the bulk-charge effect. Thus, this technique requires computation of the threshold voltage at the drain end, and adjusting $V_{g1} - V_{g2}$ accordingly. It is unclear whether this effect was taken into account in the above reports. Another limitation of this method is the difficulty of providing contacts at both ends of a sub-micrometer resistive gate.

A third method of measuring high-field drift velocity of inversion-layer electrons was introduced in [3]. In this technique the time-of-flight of discrete charge packets, introduced by a pulsed laser, are observed. The packets drift in a region of uniform tangential field at the interface. A MOS gate-controlled diode is used in the experiment, and the structure remains in a state of deep depletion, so that any electrons reaching the surface are swept into the drain and an equilibrium inversion cannot form. The electrons and holes are generated in this region by pulses from a mode-locked laser. The holes are swept to the substrate, while electrons remain at the surface where they drift in the uniform tangential field. In the actual test structure two electron packets were injected through two separate optical apertures. The time difference between the arrival of the two pulses was used to calculate the drift velocity. This differential method improves accuracy of the measurement. A drawback of this method was that only very low effective vertical fields could be created (<0.2 MV/cm), making the extension of results to typical operating conditions of regular MOSFET's problematic. The absence of an inversion layer in this technique also makes the relevance of the results a bit questionable. We will discuss the measured results of above techniques further in Section V.

III. Measurement Method

To achieve uniformity of tangential field and inversion charge concentration, we recognized that a modified version of the method reported in [1] becomes very attractive and convenient in present and future short-channel structures. Thick gate-oxide MOSFET's are used in the study, and the drain voltage is limited to small values (below 1 V). By setting the gate voltage much larger than the drain voltage, uniformity of the inversion charge and field is assured. Since deep-submicrometer devices are used in the study ($L_{\rm eff}$ from 0.5 μm to 0.1 μm), this small drain voltage is sufficient for creating large tangential electric fields. Both bulk and SOI MOSFET's with $T_{\rm ox} = 50$ nm are fabricated. In the case of bulk MOSFET's, a large reverse body bias (10 V) is used to improve the charge and field uniformity. This large reverse bias minimizes the charge nonuniformity due to the bulk-charge effect: for a uniform substrate doping of 2×10^{17} cm^{-3}, $V_{\rm ds} = 1$ V, and $V_{\rm bs} = -10$ V, the depletion width would vary from the source to drain by less than 5%. For SOI devices, due to the full depletion of the silicon film, and the large thickness of the buried oxide layer, the tangential field is very uniform and reverse body bias is not needed

$$\frac{Q_{\rm nd}}{Q_{\rm ns}} \approx \frac{(V_{\rm gs} - V_t) - \left(1 + \frac{T_{\rm ox}}{\frac{\varepsilon_{\rm ox}}{\varepsilon_{\rm si}} T_{\rm si} + T_{\rm box}}\right) V_{\rm ds}}{V_{\rm gs} - V_t} \tag{4}$$

where $T_{\rm si}$ is the silicon film thickness and $T_{\rm box}$ is the buried-oxide thickness. We found it important to use extensive two-dimensional device simulations to verify the uniformity of charge and field. A typical case is shown in Fig. 1. For this device the gate oxide thickness, the silicon film thickness, and the buried oxide thickness are 50 nm, 70 nm, and 400 nm, respectively. The gate voltages used are 20, 30, and 40 V, and the drain voltage is 1 V. As seen in Fig. 1, the tangential field is fairly uniform at the Si/SiO$_2$ interface. The reduction of the average electric field is is because of the effective $V_{\rm ds}$ drop on $R_{\rm source,drain}$ difference due to different current levels. The corresponding inversion-charge concentration is shown on the second y-axis of the plot.

Because of charge and field uniformity, the current can be simply written as

$$I = W C_{\rm ox} \left(V_g - V_t - \frac{V_{\rm ds}}{2} \right) v \tag{5}$$

where $C_{\rm ox}$ is the gate-oxide capacitance, V_t is the threshold voltage at the source, W is the channel width, and v is the drift velocity. Since v is the only unknown in this relation, it can be determined from the measured current. The tangential field is given by

$$E_x = \frac{V_{\rm ds} - I R_{\rm sd}}{L_{\rm eff}} \tag{6}$$

where $R_{\rm sd}$ is the source and drain series resistance, which was measured using the constant $V_{\rm gs} - V_t$ method of [22]. Using

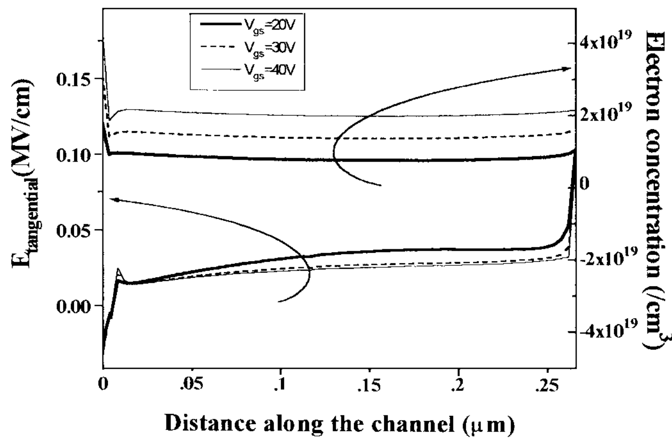

Fig. 1. Tangential electric field (E_x) and electron concentration in the SOI test structure with $T_{\rm ox} = 50$ nm, $T_{\rm si} = 70$ nm, $L_{\rm eff} = 0.4$ μm, $T_{\rm box} = 400$ nm, 5 Å from the Si/SiO_2 interface.

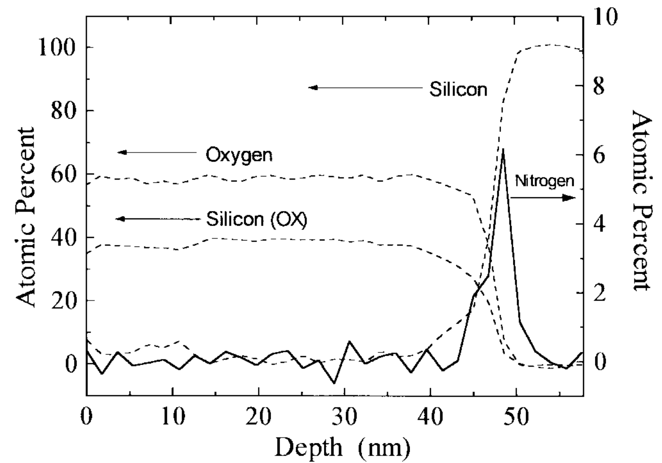

Fig. 2. Depth compositional profile for a 50-nm N_2O-annealed oxide. Note the nitrogen pile up at the silicon-oxide interface.

above relations, the carrier drift velocity can be obtained as a function of tangential field. For ultra-short devices, correction of V_t as a function of drain voltage is required, due to the drain-induced barrier-lowering (DIBL). This is accomplished by monitoring parallel shifts of the subthreshold current versus $V_{\rm gs}$ as the drain voltage is changed [14].

IV. Device Fabrication and Experiment Setup

⟨100⟩ silicon bulk and SOI wafers were used in this study. The SOI wafers were SIMOX and BESOI with buried-oxide thicknesses of 370 nm–400 nm and ~1 μm, respectively. The starting silicon film thicknesses varied from 200 nm to 250 nm. To achieve better short-channel behavior in MOSFET's, a high doping concentration in the body is needed. For the SOI devices to satisfy this condition while maintaining full depletion, a thin silicon film must be used. An initial blanket oxidation followed by wet etch was used to reduce $T_{\rm si}$ of the SOI wafers. After the final processing step $T_{\rm si}$ was 65 nm for the SOI test structures. LOCOS and MESA isolations were employed for bulk and SOI wafers, respectively. A 50-nm gate oxide was grown on all wafers by dry oxidation. The gate photoresist pattern was defined by I-line lithography, with a range of drawn lengths in 0.05-μm increments down to 0.5 μm. Effective channel lengths as short as 0.12 μm were obtained by "ashing" of the gate photoresist in oxygen plasma at 50 W [15]. Remainder of the process was typical, with the different process splits given below.

A. Nitridation of the Gate Oxide

Boron penetration from P^+-polysilicon gates into underlying silicon substrates associated with surface-channel PMOSFET's is a critical issue in dual-gate CMOS processes. It has been shown that nitridation of the gate oxide can provide a barrier to boron penetration [16], [17]. Nitrided gate oxides also have exhibited improved hot-carrier reliability, and reduced radiation degradation [16], [18]. Nitridation of the gate oxide has been shown to affect surface carrier mobility, but its effect on saturation velocity has not been studied. Thermal nitridation of the gate oxide in our samples was achieved by post-oxidation anneal at atmospheric pressure in N_2O at 950 °C for 20 min. A typical compositional profile of N, Si, and O in the gate oxide determined by Auger electron spectroscopy (AES) is shown in Fig. 2.

B. Surface Micro-Roughness

There have been conflicting reports on the influence of surface micro-roughness on inversion-layer carrier transport. To study the effect of surface micro-roughness, the silicon-oxide interface was intentionally roughened by prolonged DI-water rinsing after the HF clean and just before the gate oxidation [19]. The surface micro-roughness was measured on control samples by using Atomic Force Microscopy (AFM). The initial RMS roughness of about 0.5 nm increased to approximately 2 nm after 2000 min of DI water rinsing. Note that all surface roughness measurements were made before gate oxidation.

C. Doping Concentration

To study the effect of substrate doping level on the inversion-layer carrier transport the device doping concentrations were adjusted by ion implantation to three values of 8×10^{16} cm^{-3}, 1.5×10^{17} cm^{-3} and 2.5×10^{17} cm^{-3}.

V. Experimental Results and Discussion

A. Linear Mobility at Low Tangential Field

Mobility was measured using an I_d–V_g measurement, with channel charge determined by an integration of gate-to-source/drain/substrate capacitance, i.e., by a standard split C–V method. Fig. 3 shows the electron mobility as a function of effective vertical field. As seen, all samples match the "universal" mobility curve [20] fairly well, except for the nitrided sample. In particular, no mobility degradation is observed for the SOI wafer, or for the roughened bulk wafer. The behavior of electron mobility for the nitrided sample is in general agreement with other reports. Namely, at low

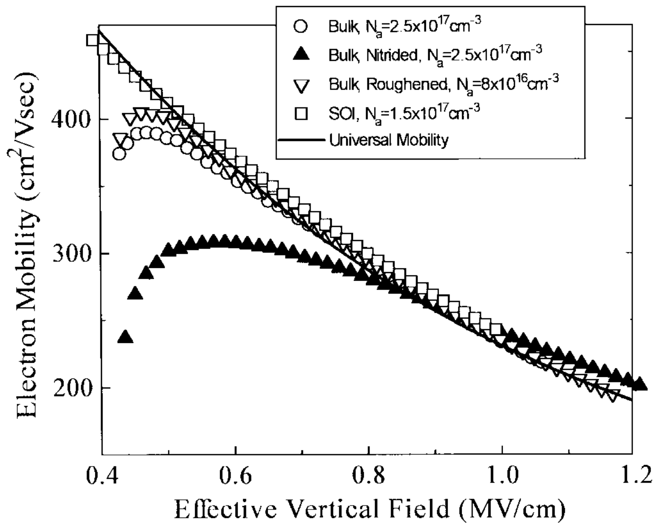

Fig. 3. The effective electron mobility versus effective vertical field. $E_{\rm eff}$ is calculated from $E_{\rm eff} = (0.5Q_n + Q_b)/\varepsilon_{\rm si}$, where Q_n is obtained from integrating the gate to channel capacitance against the gate voltage. The SOI wafer is unpolished SIMOX.

effective vertical fields a nitrided sample has electron mobility less than the "universal" value, while at high vertical fields the trend is reversed. The crossover point has been shown to be a function of N_2O anneal time and temperature [18]. Normally, shorter times and lower temperatures lead to crossovers at lower vertical fields. This behavior is attributed to extra trap generation in the nitrided oxide and Si/SiO_2 interface. At low $E_{\rm eff}$ they trap electrons and act as Coulombic scattering centers, while at high $E_{\rm eff}$ they screen surface roughness potential from channel electrons [23].

Fig. 4 illustrates the measured electron velocity as a function of tangential field. The test-structure length is approximately 0.3 μm for all of the samples. This figure indicates that the insensitivity of electron transport to doping level in the low field also extends to the high-field "saturation" regime for dopings used. The data shows also insensitivity to moderate surface microroughness, although it is not clear how rough is the surface after a 50-nm gate oxidation. Moreover, nitridation of the gate oxide has negative impact on both electron mobility and saturation velocity, at moderate vertical fields.

B. Effect of Oxide Nitridation

Fig. 5 shows the velocity-field behavior of samples with and without nitridation at different vertical fields. It is seen that the low-field mobility behavior is mirrored at high tangential fields, i.e., at a given vertical field the low-field mobility and high-field velocity of a nitrided sample are affected in the same direction. This is further illustrated in Fig. 6, where measured drift velocities at $E_x = 3.5 \times 10^4$ V/cm are plotted versus the effective vertical field. The crossover points are nearly the same in Figs. 3 and 6. Therefore, it seems attractive trying to move the crossover point to lower vertical fields, as this would lead to a better current drive in nitrided samples even at low gate voltages. As was mentioned earlier, this can be achieved by reducing the time and temperature of the N_2O

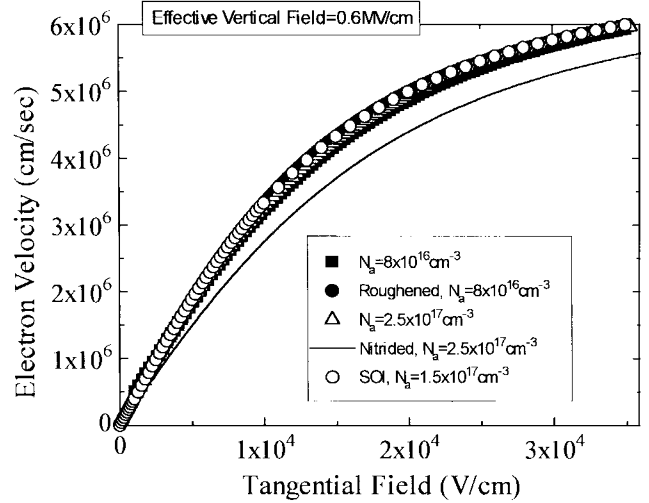

Fig. 4. The electron velocity versus tangential field. The test structure length is about 0.3 μm for all the samples.

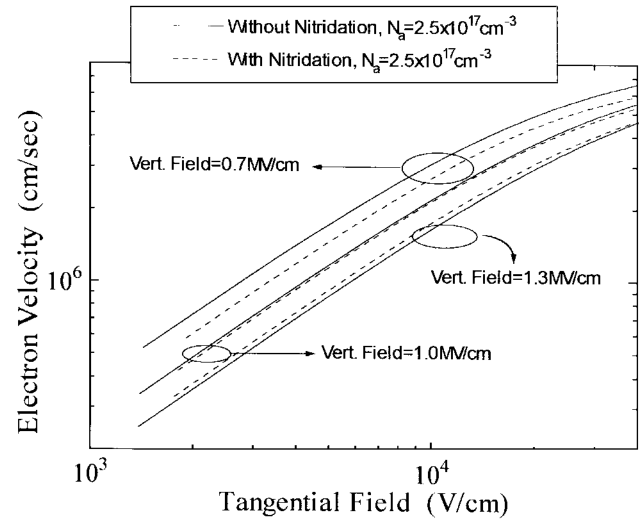

Fig. 5. The electron drift velocity versus tangential field for control and N_2O-annealed gate oxides on a bulk wafer. The effective vertical field is used as a parameter. Oxide thickness is 50 nm, and the test structure length is 0.3 μm.

anneal. However, this normally reduces the effectiveness of the nitrided oxide against boron penetration. Furthermore, as Fig. 6 shows nitridation has a weaker influence on the high-field drift velocity than on the low-field mobility. This is clearly seen in Fig. 7, where the ratio of drift velocity of a nitrided sample to that of a regular sample is plotted versus the tangential field.

C. Saturation Velocity

We have limited the drain voltage to about 1 V in our experiments. We believe that using larger drain voltages would make the approximations used in (5) and (6) less accurate. This will lead to an artificially stronger "saturation" behavior for the electron velocity, and will underestimate the saturation velocity. This may explain why very different saturation velocities, ranging from 4×10^6 cm/s to 9.2×10^6 cm/s,

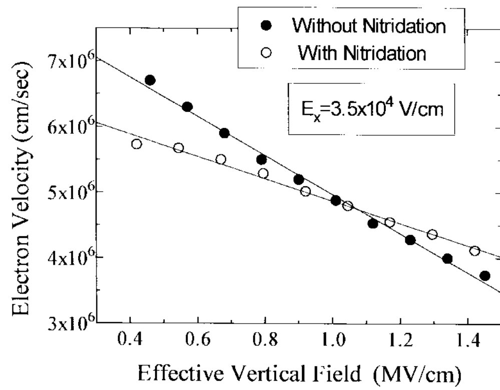

Fig. 6. The electron drift velocity at $E_x = 35$ kV/cm versus effective vertical filed for control and N_2O-annealed gate oxides grown on bulk wafers. Oxide thickness is 50 nm, and the test structure length is 0.3 μm.

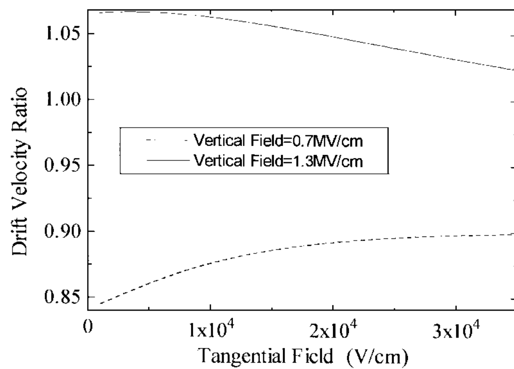

Fig. 7. Ratio of drift velocity of the N_2O-annealed sample to that of the control sample grown on bulk wafers, at two different vertical fields. The tangential field is 35 kV/cm and the test structure length is 0.3 μm.

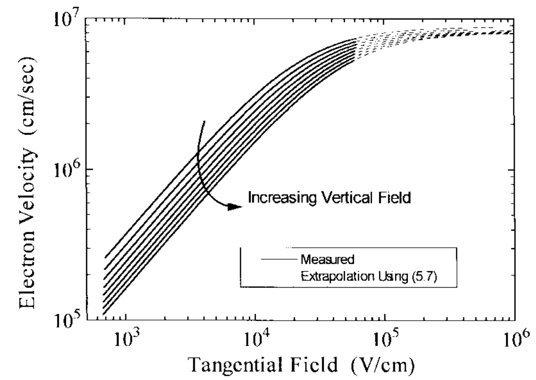

Fig. 8. Extrapolation of the measured electron velocity by using (7). Dashed lines are obtained through fitting of (7) to measured values. The bulk test structure length is 0.3 μm.

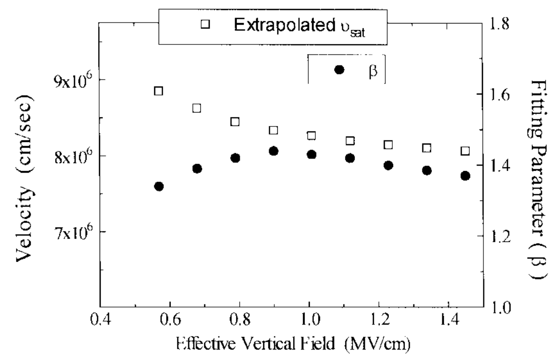

Fig. 9. The two fitting parameters of (7) as functions of the effective vertical field. The test structure was that of Fig. 11.

are reported in [1]–[5]. To obtain a semi-quantitative value for the electron saturation velocity, we have extrapolated the measured values by obtaining a two-parameter least-squares fit using the empirical equation

$$v = \frac{\mu_{\text{eff}} E_x}{\left(1 + \left(\frac{\mu_{\text{eff}} E_x}{v_{\text{sat}}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \quad (7)$$

where μ_{eff} is the effective mobility, and v_{sat} and β are fitting parameters. v_{sat} is the saturation velocity. Results of these extrapolations are shown as the dashed lines in Fig. 8. Fig. 6 indicates that at $E_x = 3.5 \times 10^4$ V/cm, drift velocity of the regular sample has a near linear dependence on the vertical field, with 3×10^6 cm/s reduction in the velocity for every 1 MV/cm increase of the vertical field. Fig. 9 shows that the final saturation velocity has a much weaker dependence on the vertical field. These extrapolated values are in the 8.1×10^6 cm/s to 8.9×10^6 cm/s range. An extrapolated v_{sat} value of 9.2×10^6 cm/s at vertical field of 0.1 MV/cm was reported in [3], which is in general agreement with our reported values at low vertical fields. We should emphasize that (7) is an empirical equation, and v_{sat} may not be the real "saturation" velocity. Nevertheless, use of v_{sat} is meaningful, since (7) and v_{sat} model the carrier velocity in the entire relevant field range correctly. That is why we believe that electron saturation velocity, i.e. velocity at a very high slowly varying tangential electric field, is dependent on E_{eff}. It is unclear however if this dependence is universal or not. Fig. 10 also shows the value of β used for fitting of (7) to the measured results. This value is nearly constant and about 1.4. This is quite different from the value of 2 (the bulk electron transport value) used in popular device simulators.

D. Velocity Overshoot

Fig. 10 points to another important finding, i.e., observation of electron velocity overshoot. As seen, for test structure lengths of 0.3 μm or longer electron velocity is nearly the same, but it increases for shorter lengths. Fig. 11 further illustrates this observation. Fig. 12 conveys similar information for $T = 85$ K, except that velocity saturation and velocity overshoot are more pronounced. In fact, average inversion-layer electron velocity exceeds bulk electron saturation velocity by nearly 40% at $L_{\text{eff}} = 0.12$ μm. Fig. 13 shows that for very short test structures the average electron velocity has a strong dependence on the vertical field, particularly at liquid nitrogen temperature. This is because velocity overshoot is weaker when the low-field mobility is lower, and that increased vertical field reduces the low-field mobility [12]. Note that in our test structures the field pattern is quite different from that in regular MOSFET's. In our structures the field is nearly uniform in the channel, and is very large at the source where cold electrons are injected to the channel. Once these data

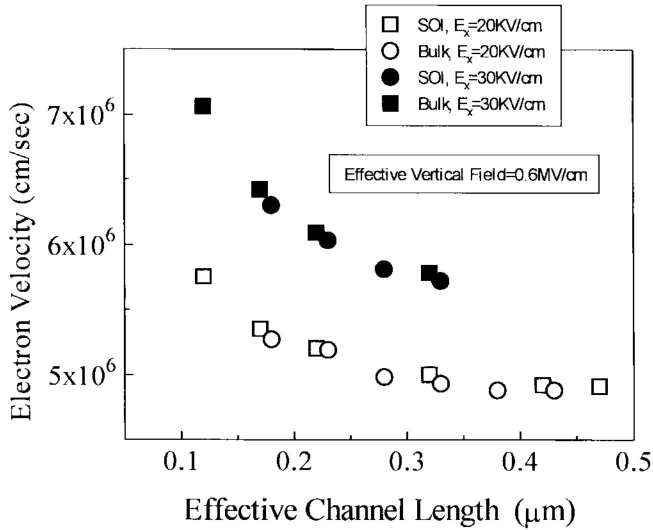

Fig. 10. The electron drift velocity as a function of test structure length, for two different tangential fields of 20 kV/cm and 30 kV/cm. SOI and bulk samples are compared.

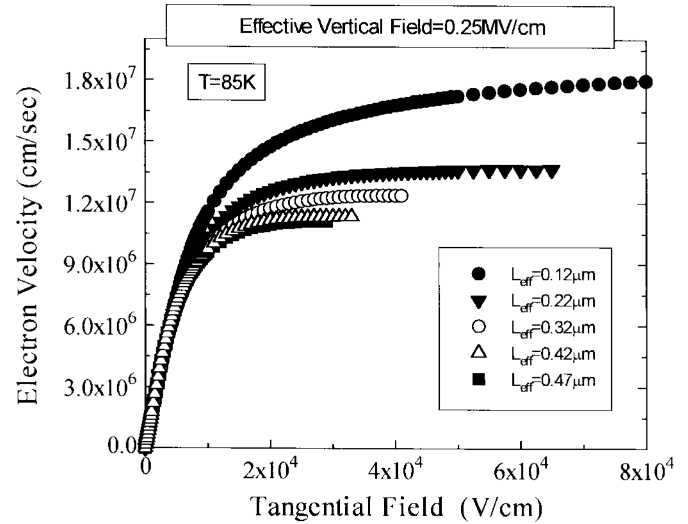

Fig. 12. The electron velocity as a function of tangential field at $T = 85$ K. Test structure length is used as a parameter.

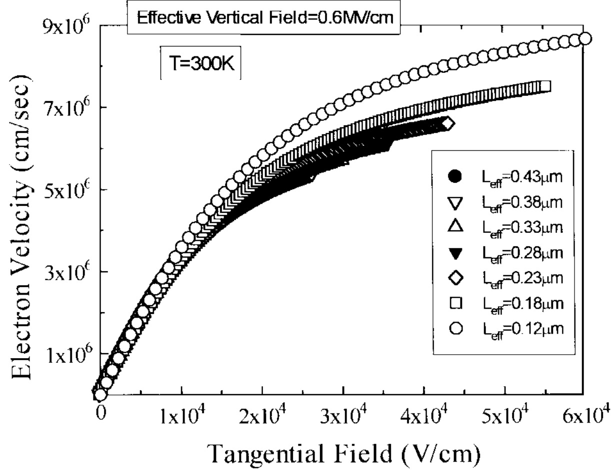

Fig. 11. The electron velocity as a function of tangential field, for several different test structure lengths.

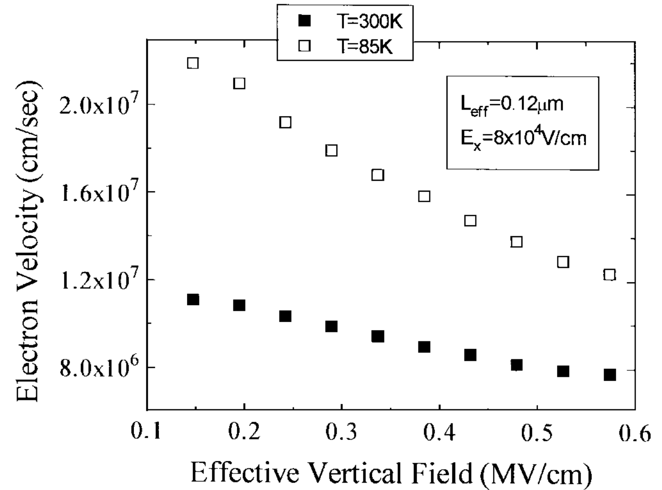

Fig. 13. Vertical field dependence of the electron velocity at room and liquid nitrogen temperatures for a 0.12-μm device. The tangential field is 80 kV/cm.

are understood, modeled, and used to calibrate simulators, the effect of velocity overshoot on MOSFET $I-V$ can be analyzed.

E. Hole Velocity

Fig. 14 shows the hole mobility versus effective vertical field. As seen, similar conclusion as in the case of electrons can be reached for holes: Only mobility of the nitrided sample is significantly lower than the universal mobility. Note also that in the case of holes no crossover point exists, as at all vertical fields nitrided sample exhibits a lower mobility. Fig. 15 illustrates hole velocity as a function of tangential field. The test-structure length is approximately 0.2 μm for all of the samples. The nitrided sample has a lower velocity, although the velocity reduction is fairly small. The hole drift velocity versus tangential field is shown in Fig. 16, for different vertical fields. The velocity-field behavior of holes is much more gradual than that of electrons. Consequently, very large tangential fields would be needed to observe the "saturation" behavior. If our measurement method or those reported in [1], [2], [4], and [5] are extended beyond their valid field limits, artificially low values for the hole saturation velocity will be obtained. On the other hand, extrapolation of measured results by using (7) indicates that $v_{\rm sat}$ of holes will be in the vicinity of 5×10^6 cm/s to 7×10^6 cm/s, depending on the vertical field. Note that the hole drift velocity shows a stronger vertical field dependence than the electron drift velocity. Fig. 17 shows the hole velocity as a function of tangential field, for different test structure lengths. No velocity overshoot is observed down to 0.14 μm.

VI. Conclusion

To study high-field transport of the inversion-layer carriers, deep sub-micrometer test structures were fabricated on bulk and SOI wafers varying doping concentration, surface

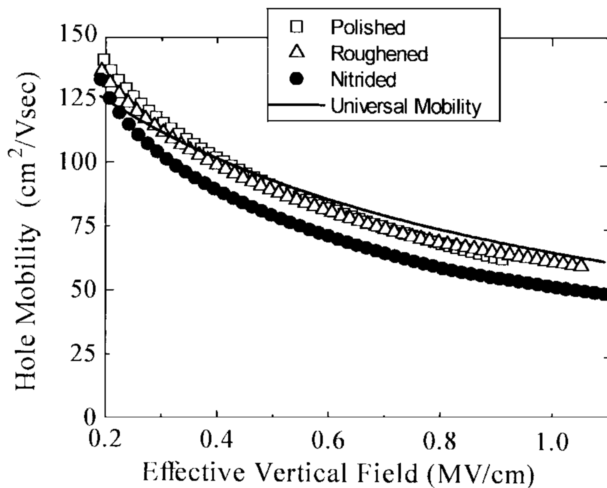

Fig. 14. The hole mobility as a function of effective vertical field. All the samples are SOI. The silicon film doping concentration is 2×10^{17} cm^{-3}.

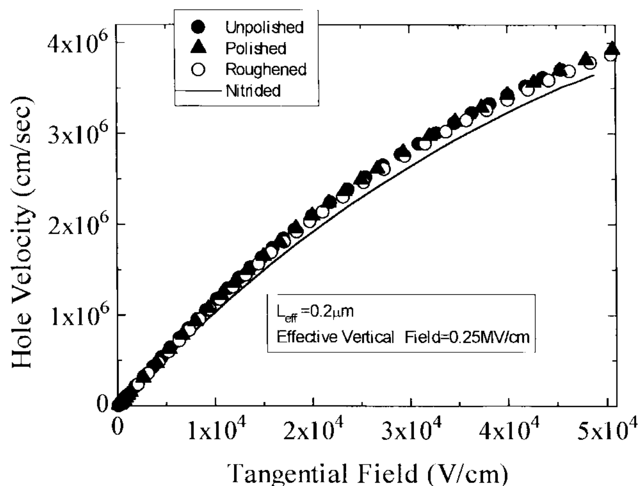

Fig. 15. The hole velocity versus the tangential field. The test structure length is 0.2 μm for all the samples.

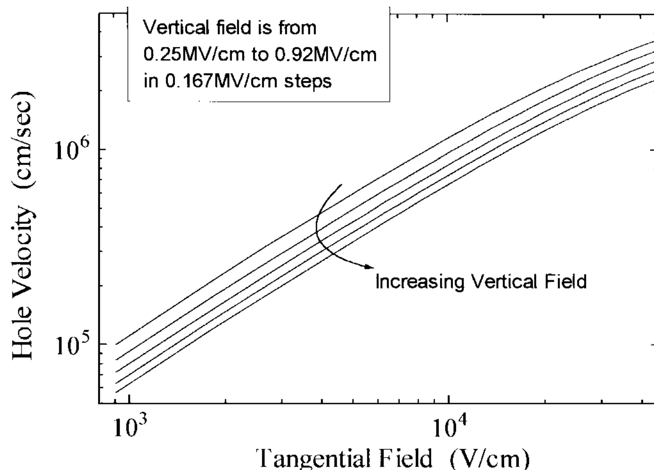

Fig. 16. The hole drift velocity versus the tangential field, with vertical field as a parameter. The sample is not nitrided. The test structure length is 0.2 μm.

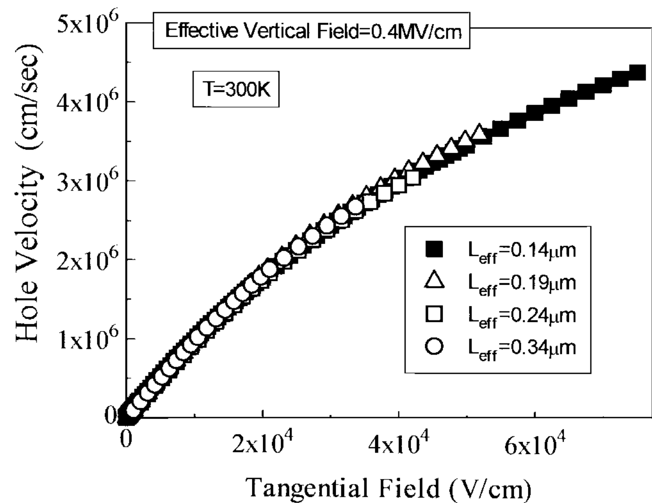

Fig. 17. The hole velocity as a function of tangential field at room temperature. Several different test structure lengths are shown and no velocity overshoot is detectable.

micro-roughness, nitridation of the gate oxide, and carrier type (electrons and holes). Several interesting phenomena were observed including: electron velocity overshoot at room temperature, dependence of the electron and hole high-field velocity on nitridation of the gate oxide.

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Fariborz Assaderaghi (S'86–M'96), for a photograph and biography, see p. 421 of the March issue of this TRANSACTIONS.

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