

AC Output Conductance of SOI MOSFET's and Impact on Analog Applications

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Abstract— We report a frequency-dependent output conductance of partially depleted SOI MOSFET's. For high-frequency analog applications, the output conductance is less than half and the dynamic range of V_d is two times higher than the dc I - V characteristics would indicate. A simple physical model for the phenomenon that involves a phenomenological body charging capacitance and can fit data within 10% is presented.

I. INTRODUCTION

RECENTLY, transient floating body effects in SOI MOSFET's have gained a lot of attention. The importance of these effects on digital circuit performance was verified by both simulations [1] and experiment [2], [3]. In this paper we discuss the impact of transient body charging on analog device performance and give a model explaining the results. The experimental setup is shown in the insert of Fig. 1. It is essentially the same as in [4] and [8]. We measure the ac output conductance of the device at the drain while applying a dc gate bias.

II. DEVICE FABRICATION

The four-terminal n- and p-channel SOI MOSFET's were fabricated on a single SIMOX wafer with a relatively thin buried oxide (850 Å) to minimize self-heating effect. We describe only NMOS process here. MESA isolation was created by etching a nitride/oxide/silicon stack, stopping at the buried oxide. A 1000 Å was grown on MESA sidewalls to prevent the low- V_t edge devices and gate oxide defects at MESA corners. Threshold implant was then performed resulting in channel doping about $2.0 \times 10^{17}/\text{cm}^3$. Dry oxidation was done to grow 70 Å of gate oxide which was followed by deposition of 3000 Å of polysilicon. Poly doping was realized by $5 \times 10^{15}/\text{cm}^2$ 25 KeV phosphorus implant. The photoresist ashing technique was used to define deep submicron gates [5]. A $3 \times 10^{15}/\text{cm}^2$ 30 KeV phosphorus implant was done to form source/drain. Consequent steps were conventional passivation, contact opening and metallization. The final Si film thickness of devices used was measured to be 1600 Å using nanospec.

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III. RESULTS AND DISCUSSION

The $G_{\text{out}}-V_d$ curves measured with a floating body at different frequencies as well as dc are shown on Fig. 1. From the $V_g = 1.1$ V series of G_{out} curves, one can see that the kink-related hump of output conductance is moving out as the frequency is increased: it occurs at about $V_d = 1.1$ V for dc case, 1.6 V for 11 kHz curve, 1.8 V for 110 kHz and 2.0 V for 1.1 MHz. The origin of the hump is the impact ionization current related body charging which gives a kink in a dc curve. The reason for the hump moving out with increasing frequency is that the impact ionization current change due to ac drain signal does not have time to charge the body, unless the drain dc bias is increased. After integrating the G_{out} with respect to V_d , the dc I - V characteristics are obtained [4] and shown in Fig. 2. The I - V curves also show the same shift of kink position as the frequency is increased.

We used 10 mV and 20 mV for drain signal ac amplitude. The obtained G_{out} curves agreed for both of them, so we assume "small signal" linear response of device currents to the ac signal.

Note that unlike [2], [3], the integrated I_d-V_d curve is a result of the drain pulsing, so it is immune to the V_g -induced transient effects. This condition is related to many analog circuits where V_g swing is small. The drain pulsing technique does not take gate-to-body coupling into account, which proved to be rather significant [6]. However, this condition is also relevant in the operation of a pass transistor.

All the transient response observed is due to impact ionization current taking time to charge the floating body. Note that drain-to-body coupling is independent of frequency. But we consider only the difference between measured output conductance G_{out} and the high-frequency output conductance, so capacitive coupling is subtracted out. Actually, high-frequency output conductance agreed well with the grounded body contact dc output conductance, which means that drain-to-body coupling is negligible and all high-frequency G_{out} is solely due to DIBL/channel length modulation.

The plot of G_{out} versus frequency is shown on Fig. 3. Note that at low frequency the output conductance is rather high due to the response of body voltage or body charging to the V_d signal. The ac output conductance can be modeled with a simple diode/capacitance model shown in Fig. 4. The I_{ii} current source is due to impact ionization, and the diode models the body-to-source junction current. Let us define $C_B (\equiv \frac{\partial Q_B}{\partial V_{bs}})$ —the small signal floating body capacitance to be charged. Here Q_B is total charge in the body, and V_{bs} is body-to-source potential. It depends on device geometry

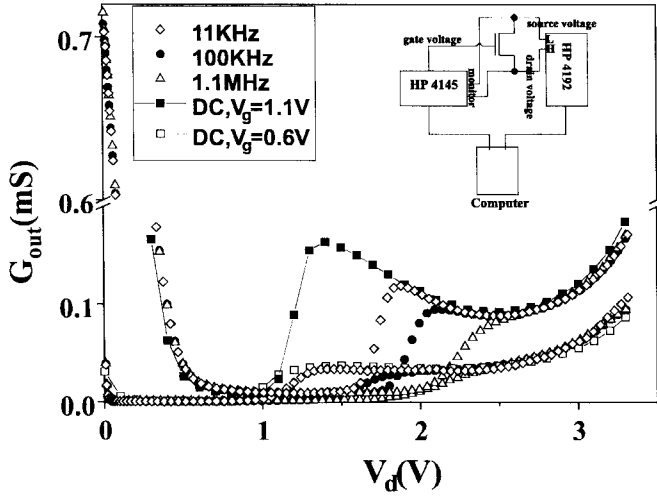


Fig. 1. The measured output conductance for a 10/5- μm device for gate biases of 0.6 and 1.1 V and different frequencies. LCR measurement setup scheme is shown in the insert.

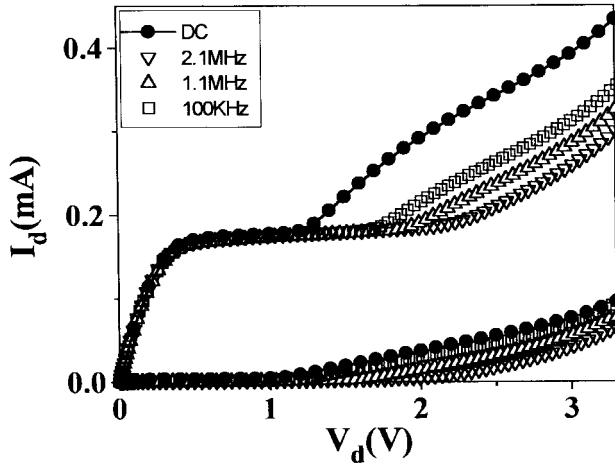


Fig. 2. The integrated curves showing $I_d(V_d) = \int_0^{V_d} G_{out} dV_d$. Kink position moves out as the frequency is increased. Gate bias is the same as in Fig. 1.

and bias conditions. The differential resistance of the diode $R_{diode} = \frac{\partial V_{bs}}{\partial I_{diode}} \approx \frac{nkT}{qI_{diode}}$ is fixed at each bias point. The dc bias point of V_{bs} is determined by $I_{ii}^{dc}(V_d, V_g) = I_{diode}(V_{bs})$. The ac V_{bs} is

$$\frac{\Delta V_{bs}}{\Delta I_{ii}} = Z \equiv \frac{R_{diode}}{j\omega C_B R_{diode} + 1}. \quad (1)$$

The expression for the output conductance can be written as $G_{out} = G_{DIBL} + G_{ii}$, and the output conductance due to body charging is

$$G_{ii} = \frac{\partial I_d}{\partial V_t} \frac{\partial V_t}{\partial V_{bs}} \frac{\partial V_{bs}}{\partial I_{ii}} \frac{\partial I_{ii}}{\partial V_d}. \quad (2)$$

Hence, the frequency-dependent component of the output conductance is proportional to the derivative $\frac{\partial V_{bs}}{\partial I_{ii}} = Z$. As can be seen from above, the Z dependence on ω resembles the G_{out} -frequency plot of Fig. 3. The theoretical model was fitted to the experimental data on Fig. 3, which shows good agreement with data. Note in Fig. 3 the high-frequency

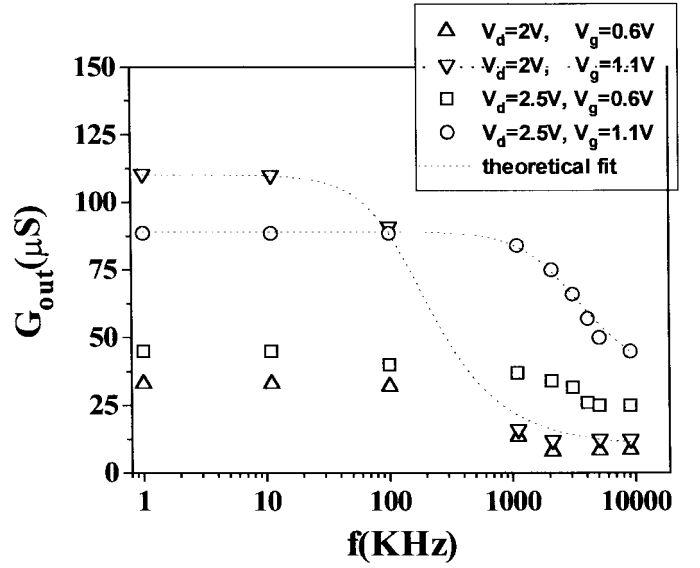


Fig. 3. The dependence of the output conductance G_{out} on frequency (symbols). Model fit to the experimental data (lines).

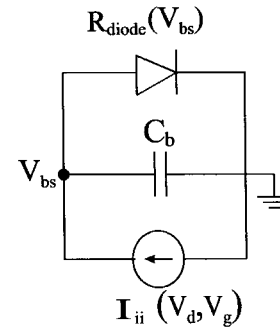


Fig. 4. The model circuit schematic. $R_{diode} = \frac{dI_{diode}}{dV_{bs}}$; and C_b represents body capacitance; I_{ii} is current source due to impact ionized holes in the body.

G_{out} 's agree well with the dc G_{out} 's measured with the body grounded.

Note that the values of C_B and R_{diode} cannot be directly extracted from Fig. 3. This is because a coefficient of proportionality between Z and G_{ii} is related to current drive, body coefficient and impact ionization parameters, as can be seen from (2). One can directly see however the -3 dB frequency f_c of body charging process. It is strongly dependent on bias, especially on V_d , because I_{ii} is exponentially dependent on V_d . For the case of $V_g = 1.1$ V we get $f_c = 100$ kHz ($V_d = 2.5$ V), and 4 MHz ($V_d = 2$ V).

IV. CONCLUSION

The frequency dependence of output conductance of PD SOI MOSFET was studied. At high enough frequency which depends on the bias point, the ac output signal becomes insensitive to floating body kink. Hence, PD SOI technology offers better voltage gain and drain voltage dynamic range for analog design than dc characteristics would suggest. The LCR technique presented can also be used in parameter extraction of a PD SOI device without a fourth body contact, since the quantities measured in the experiment are directly related to

source-body diode, body capacitance and the impact ionization current. Of course, a grounded body SOI MOSFET would be even more suitable for analog applications [7]; the additional body contact might also be used for SOI bipolar transistor.

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