Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI

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***Abstract*— In this paper, we propose a novel operation of a MOSFET that is suitable for ultra-low voltage (0.6 V and below) VLSI circuits. Experimental demonstration was carried out in a Silicon-On-Insulator (SOI) technology. In this device, the threshold voltage of the device is a function of its gate voltage, i.e., as the gate voltage increases the threshold voltage (V_t) drops resulting in a much higher current drive than standard MOSFET for low-power supply voltages. On the other hand, V_t is high at $V_{gs} = 0$, therefore the leakage current is low. We provide extensive experimental results and two–dimensional (2-D) device and mixed-mode simulations to analyze this device and compare its performance with a standard MOSFET. These results verify excellent inverter dc characteristics down to $V_{dd} = 0.2$ V, and good ring oscillator performance down to 0.3 V for Dynamic Threshold-Voltage MOSFET (DTMOS).**

I. Introduction

During the past few years demand for high-performance and low-power digital systems has grown rapidly. Several factors have contributed to this fast growth. First, laptop and notebook computers, and personal communication systems have gained popularity. Consequently, portable applications that traditionally required a modest performance (such as wrist watches and calculators), are now dominated by devices that demand a very high performance. The demand for portability of these new systems limits their battery weight and size, placing a severe constraint on their power dissipation. Second, speed, density, and size of nonportable CMOS based systems have increased considerably in recent years. Thus, power consumption that was not a concern in these systems, is now becoming a critical parameter.

The most common approach for reducing power is power supply scaling. This is due to the fact that in CMOS digital circuits, delivered power is proportional to the square of power supply voltage

$$P = C_L V_{dd}^2 f_d \tag{1}$$

where P is the power consumed by one gate, C_L is the total switching capacitance of the gate, V_{dd} is the power supply voltage, and f_d is the average cooperating frequency of that gate. Since power supply reduction below three times the threshold voltage (3 V_t) will degrade circuit speed significantly, scaling of the power supply should be accompanied by threshold voltage reduction [1]. However, the lower limit for threshold voltage is set by the amount of off-state leakage current that can be tolerated (due to standby power consideration in static circuits, and avoidance of failure in dynamic circuits and memory arrays), and ideally should be no less than 0.4 V. It is seen that if standard MOSFET's are used, a lower bound for power supply voltage or a larger leakage current become inevitable. To extend the lower bound of power supply to ultra-low voltages (0.6 V and below), we propose a **D**ynamic **T**hreshold Voltage **MOS**FET (DTMOS) having a high V_t at zero bias and a low V_t at $V_{gs} = V_{dd}$.

This paper is organized as follows: Section II describes device structure and fabrication. Section III provides DTMOS theory of operation, and experimental and simulation results comparing DTMOS and standard MOSFET. Section IV contains further discussion of DTMOS and concluding remarks.

II. Device Structure and Fabrication

The Silicon-On-Insulator (SOI) devices used in the study were built on SIMOX and BESOI wafers. The buried oxide thickness was 370–400 nm for SIMOX wafers and approximately 1 mm for BESOI wafers. The final SOI film thickness varied from 130 to 160 nm. Mesa active islands were created by plasma-etching a nitride/oxide/silicon stack stopping at buried oxide. A 100-nm oxide was grown on the mesa sidewalls to prevent low-V_t edge devices and gate oxide defects at the mesa corners. Threshold implants were then performed, resulting in concentrations of $1.5–3 \times 10^{17}$/cm^3. Gate oxides of 6.4 nm and 10 nm thickness were grown, followed by the deposition of 300 nm of undoped polysilicon. Oxygen plasma "ashing" was done to the gate photoresist to achieve effective channel lengths down to 0.2 μm [2]. High-dose arsenic and boron source/drain and polysilicon gate implants were used to create NMOSFET's and PMOSFET's with N$^+$ and P$^+$ poly gates, respectively. The combination of silicon film thickness, doping concentration, and gate type resulted in nonfully depleted (NFD) devices. Important parameters of the two resulting technologies are given in Table I.

Some test devices had a four-terminal layout to provide separate source, drain, gate, and body contacts, illustrated in Fig. 1. This allows for operation of the device in the standard MOSFET mode, or in DTMOS mode: the body is

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TABLE I
PARAMETERS FOR TECHNOLOGIES A AND B

	NMOS V_{to}(V)	PMOS V_{to}(V)	$N_{a,NMOS}$(cm^{-3})	$N_{a,PMOS}$(cm^{-3})	T_{ox}(nm)
Tech. A	0.70	-0.58	$2.5x10^{17}$	$2x10^{17}$	10
Tech. B	0.48	-0.46	$3x10^{17}$	$3x10^{17}$	6.4

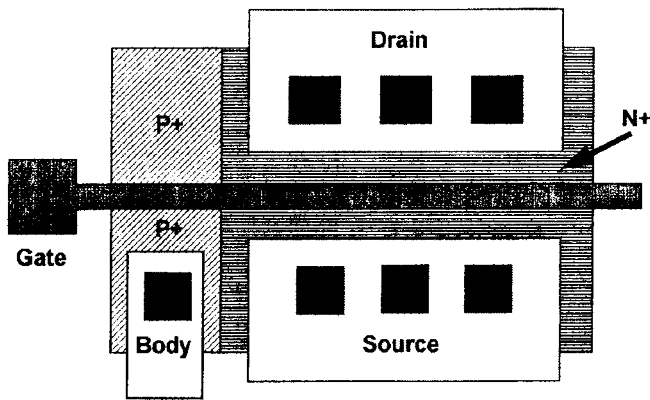


Fig. 1. Schematic of the body contact in SOI NMOS devices. A similar structure is used for SOI PMOS devices with N^+ and P^+ regions exchanged.

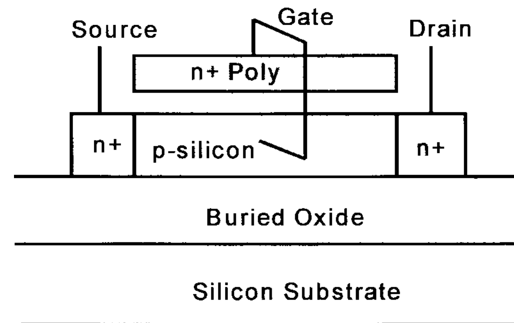


Fig. 2. Cross section of an SOI NMOSFET with body and gate tied together.

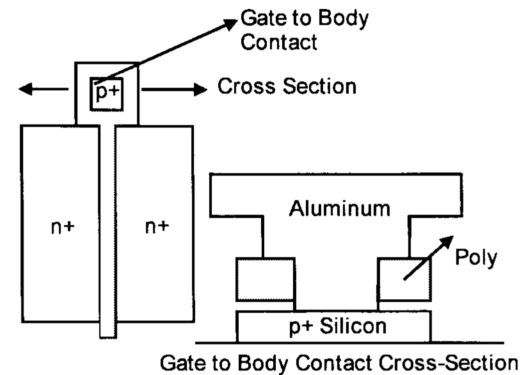


Fig. 3. Gate-to-body connection by using aluminum to short the poly gate to the P^+ region. A large metal-to-P^+ contact window is aligned over a "hole" in the poly gate. This contact requires no additional processing steps.

either floated or grounded in the MOSFET mode. The gate is tied to the body in the DTMOS mode, shown in Fig. 2. Besides the four-terminal test device, DTMOS devices with hard local gate-to-body connections were also fabricated as shown in Fig. 3. This connection uses an oversized metal-to-P^+ contact window aligned over a "hole" in the poly gate [3]. The metal shorts the gate and the P^+ region (for N-DTMOS). This contact requires minimal area and no additional processing steps. Standard CMOS, and DTMOS-based CMOS ring oscillators were also fabricated in the same process. All device processing was performed in the University of California Microfabrication Laboratory.

III. DTMOS ANALYSIS

A. Theory of Operation

The analysis provided here is for NMOS device, with its extension to PMOS device being straightforward. In DTMOS the floating body and gate of SOI MOSFET are tied together, as illustrated in Fig. 2. Although a similar configuration was proposed before by Colinge [3] and later in [4]–[6], all the authors tried to exploit the extra current produced by the lateral bipolar transistor. This requires the body voltage to be 0.6 V or larger. The extra drain (collector) current comes at the cost of a large input (base) current, which contributes much more to the standby current than the drain leakage current. We report large improvement in I_d over standard MOSFET even when gate (body) voltage is kept below 0.6 V. Although the same idea can be used in bulk devices, isolation of the MOSFET body can be accomplished more easily in SOI, where, because of very small junction areas, base current and capacitances can

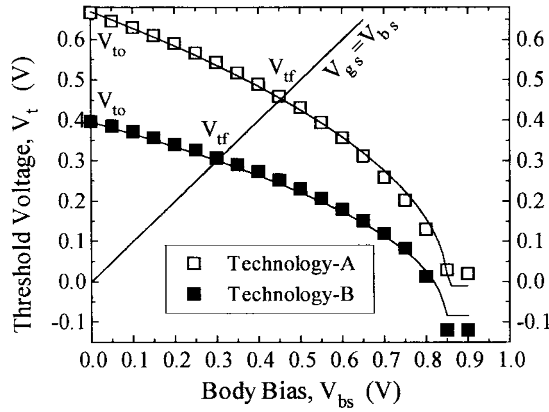


Fig. 4. Threshold voltage of SOI MOSFET as a function of body-source forward bias, for technologies A and B. Important parameters of these two technologies are given in Table I. Four terminal devices similar to Fig. 1 were used for these measurements.

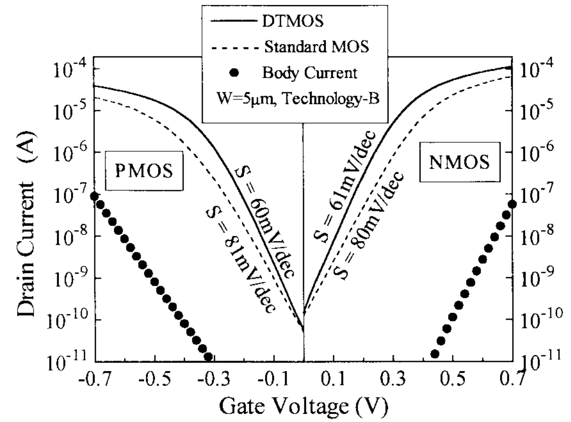


Fig. 5. Subthreshold characteristics of SOI NMOSFET and PMOSFET, operating in DTMOS and standard MOS regimes. Body (base) currents of DTMOS devices are also known.

be also much less than a bulk DTMOSFET. In [3]–[6], the increase of drain current over standard MOSFET at low gate voltages was interpreted as contribution of the lateral bipolar transistor with current gains as high as 10^4. As we will show below, a better explanation is the reduction of MOS threshold voltage because of forward body bias.

Body bias effect is normally studied in the reverse bias regime, where threshold voltage increases as body-to-source reverse bias is made larger. DTMOS operates in the exact opposite regime. Namely, the body-source junction is "forward biased" (at less than 0.6 V), forcing the threshold voltage to drop. Fig. 4 illustrates this behavior for NMOSFET, where a separate terminal is used to control the body voltage. In this figure V_{to} denotes the threshold voltage with body bias set to zero

$$V_{to} = 2\Phi_B + V_{FB} + \frac{\sqrt{2\epsilon_S q N_a (2\Phi_B)}}{C_{ox}}. \quad (2)$$

Here V_{FB} is the flat band voltage, $2\Phi_B$ is the inversion layer potential, ϵ_S is Si permitivity, q is the electron charge, N_a is the channel doping, C_{ox} is the gate oxide capacitance. V_t is given by

$$\begin{aligned} V_t &= V_{to} - \lambda(\sqrt{2\Phi_b} - \sqrt{2\Phi_b - V_{BS}}) \\ &= 2\Phi_B + V_{FB} + \lambda\sqrt{2\Phi_B - V_{BS}} \end{aligned} \quad (3)$$

where $\lambda = \sqrt{2\epsilon_S q N_a}/C_{ox}$. The loci of DTMOS operation is shown by $V_{gs} = V_{bs}$ line in Fig. 4. V_{tf} represents the point where the body (or gate) bias and the threshold voltage become identical. When V_{gs} is less than V_{tf}, DTMOS is in the subthreshold regime. Letting $V_{bs} = V_t$ in (3), we can determine V_{tf}

$$V_{tf} = 2\Phi_B + V_{FB} + \frac{\epsilon_S q N_a}{C_{ox}^2}\left(\sqrt{1 - \frac{2V_{FB}C_{ox}^2}{\epsilon_S q N_a}} - 1\right). \quad (4)$$

Thus, at $V_{gs} = V_{bs} = V_{tf}$, V_t is at a desirable and lower value than V_{to}. This lower threshold voltage does not come at the expense of higher off-state leakage current because at $V_{gs} = V_{bs} = 0$ DTMOS and the standard device have the same V_t. In fact, they are identical in all respects and consequently have the same leakage. Reduced V_{tf} compared to V_{to} is attained through an ideal subthreshold swing of 60 mV/dec. In a DTMOS transistor, the surface potential varies with the gate voltage mV for mV, and a subthreshold swing of 60 mV/dec is achieved. Fig. 5 demonstrates this for PMOS and NMOS devices operated in DTMOS mode and in the standard mode.

An equally important improvement is further obtained above V_{tf} (Fig. 4). As the gate of DTMOS is raised beyond V_{tf}, threshold voltage, which is now a function of gate bias, drops further. For example, for Tech-B in Fig. 4, at $V_{gs} = V_{bs} = 0.6$ V, the effective threshold voltage $V_t(V_{gs} = V_{bs} = 0.6\,\text{V}) =$ 0.2 V compared to $V_{to}(V_{gs} = V_{bs} = 0) = 0.4$ V. V_t reaches its minimum ($V_{t,\min}$) when $V_{gs} = V_{bs} = 2\Phi_B$

$$V_{t,\min} = 2\Phi_B + V_{FB}. \quad (5)$$

Comparison of (3) and (5) with (2), points to the fact that the reduced threshold voltage is due to the reduction of body charge. At $V_{t,\min}$ body charge is totally eliminated. In Fig. 4, to obtain the sharpest curve (due to body effect parameter dependence on N_a) and a curve shifted to the left (an hence the maximum V_t reduction), the highest acceptable doping, i.e., highest acceptable V_{to}, and a low work function gate material should be used (Fig. 6). Obviously, the net result of threshold voltage reduction is the increase of inversion charge or equivalently the gate capacitance

$$\begin{aligned} dQ_n &= C_{ox}\left(\partial V_g - \frac{\partial V_t}{\partial V_g}\partial V_g\right) \Rightarrow C_{eff} \\ &= C_{ox}\left(1 + \left|\frac{\partial V_t}{\partial V_g}\right|\right). \end{aligned} \quad (6)$$

This is demonstrated in Fig. 7, where C_{gds} and Q_n of DTMOS and standard MOSFET are compared. An interesting interpretation of (6) is that DTMOS provides an effectively thinner gate oxide, in addition to having a V_t that is larger at $V_g = 0$. Reduction of body charge in DTMOS leads to another advantage, namely higher carrier mobility, as seen in Fig. 8. This is due to the fact that body charge reduction leads to a lower effective normal field in the channel [7]. This statement

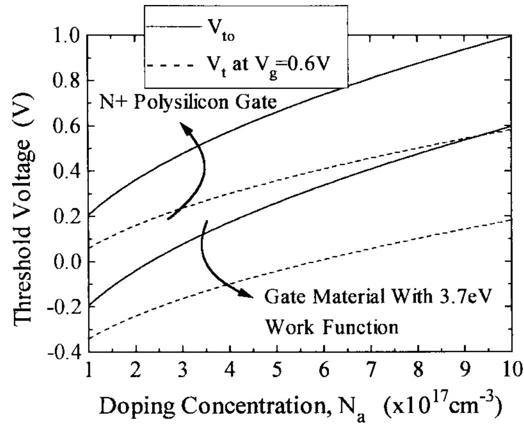


Fig. 6. Predicted threshold voltage of a N-DTMOS at $V_{gs} = 0$ and at $V_{gs} = 0.6$ V, as a function of silicon film doping concentration. Two different gate materials are considered. $t_{ox} = 6.4$ nm.

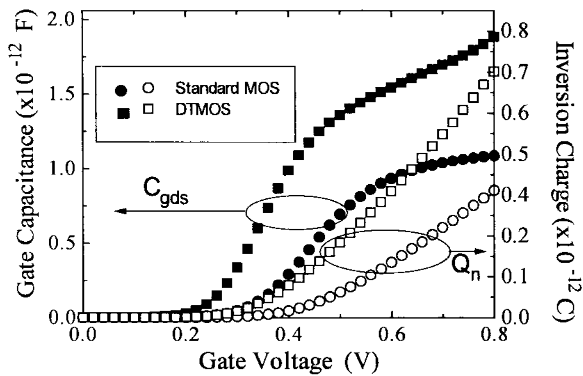


Fig. 7. Gate capacitance and inversion charge of an NMOSFET with body grounded (standard MOS) and body tied to the gate (DTMOS). The mobile charge Q_n is obtained by integrating the gate capacitance. $W/L = 20\,\mu$m/$20\,\mu$m, $t_{ox} = 6.4$ nm.

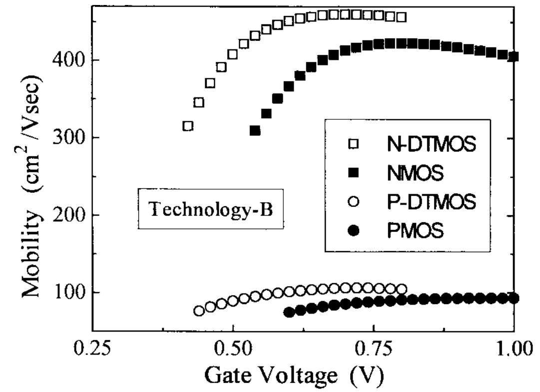


Fig. 8. Electron and hole effective mobility as a function of gate voltage, for standard MOSFET and for DTMOS. Devices from Tech-B were used in these measurements.

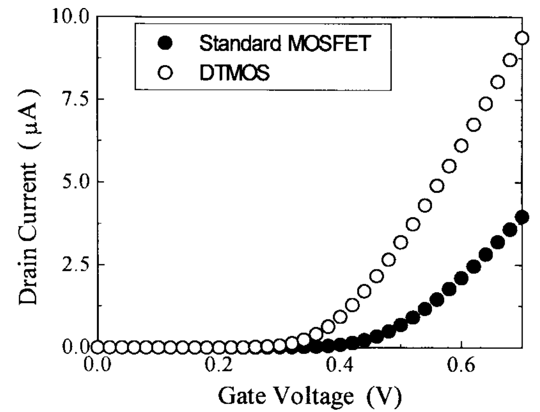


Fig. 9. Drain current of the NMOS device shown in Fig. 7 versus gate voltage, for standard MOSFET and for DTMOS. $V_{ds} = 50$ mV, $W/L = 20\,\mu$m/$10\,\mu$m.

becomes more evident when one realizes [8]

$$E_{eff,normal} \equiv \frac{Q_B + \frac{Q_n}{2}}{\epsilon_s} \approx \frac{V_{gs} + V_t}{6t_{ox}}. \tag{7}$$

Assuming $V_{FB} + 2\Phi_B = 0$ in (2) obviously, lower V_t leads to a lower E_{eff} and higher mobility. The higher mobility and larger inversion charge lead to a higher current drive in DTMOS as seen in Fig. 9.

In DTMOS operation the upper bound for applied $V_{gs} = V_{bs}$ is set by the amount of base current that can be tolerated for low-power VLSI circuits. This is illustrated in Fig. 5, where PMOS and NMOS device body (base) currents are shown. At $V_{gs} = 0.6$ V base currents for both PMOS and NMOS devices are less than 2 nA/μm. This current level is tolerable in most circuits, however V_{gs} can not be raised appreciably above 0.6 V due to the exponential rise of this leakage current. Consequently, exploiting the bipolar current might not be practical, as a sizable collector current would require $V_{bs} > 0.6$ V. The ratio of the drain current to the body (base) current of Fig. 5 can be interpreted as bipolar current gain, and hence the device would have a large current gain [3]–[6]. We believe a more precise interpretation is the threshold voltage reduction by means of forward body bias outlined above. Since for $0 < V_{gs}(= V_{bs}) < 0.6$ V, the surface potential is lower than the potential in the silicon film, the current is still confined to the inversion layer at the Si/SiO_2 interface in the standard MOSFET. This is verified by 2-D simulation of DTMOS device shown in Fig. 10, where $V_{gs} = V_{bs} = V_{ds} = 0.6$ V. In fact, if the device channel length is not ultra-short, current gain of the lateral bipolar device will be modest. We have demonstrated this with a four-terminal device in Figs. 11 and 12, where drain (collector) and base currents, and apparent β are plotted for several different gate voltages. For positive gate voltages, MOS current is added to the bipolar collector current and the apparent bipolar current gains are very high. However, as V_{gs} is made negative, the MOS current is eliminated and β drops to its true bipolar low value, independent of the gate voltage. Thus, for $V_{gs} > 0$ the ratio of drain current to base current can not be interpreted as bipolar current gain.

B. Experimental and Simulation Results

Devices based on technologies A and B were considered in this study. Important parameters of these two technologies are given in Table I. The interconnect load capacitance of each stage was assumed to be equal to total gate capacitance of a stage. The measured inverter dc transfer characteristics

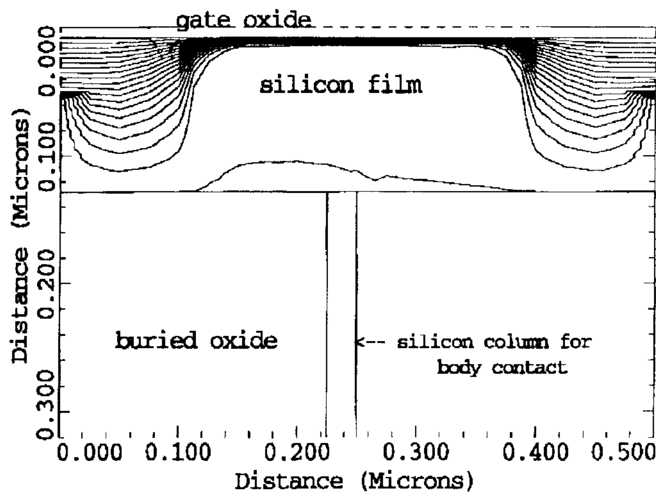


Fig. 10. TMA-MEDICI simulation of an NMOS SOI device with body and gate tied together. As in [4], the body contact is created below the device for ease of simulation only. The total buried oxide thickness is not shown here. $V_{gs} = V_{bs} = V_{ds} = 0.6$ V.

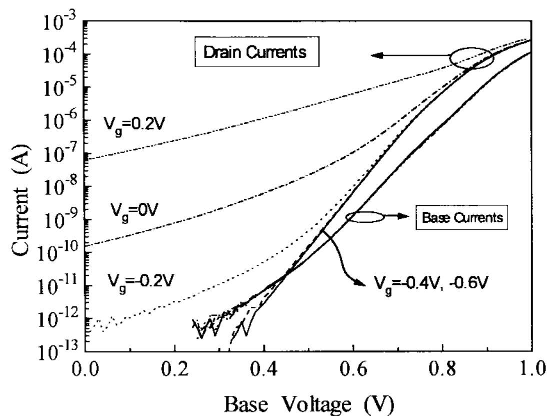


Fig. 11. Drain and base currents of a 4-terminal device versus its base voltage. The gate voltage is raised from −0.6 to 0.2 V in 0.2 V steps. Device base width (channel length) is 0.3 μm, $W = 5\ \mu$m.

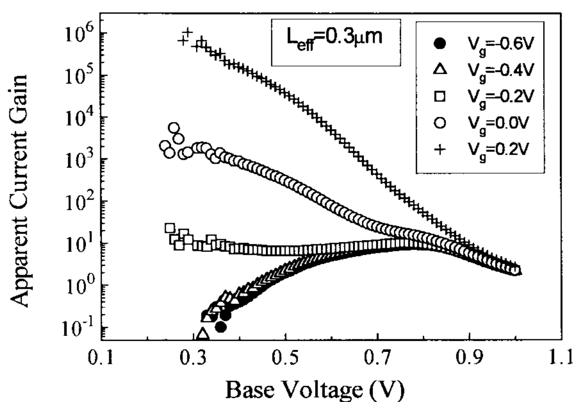


Fig. 12. Apparent β of the device reported in Fig. 11, obtained by dividing the drain (collector) current by the base current. Gate voltage is raised from −0.6 to 0.2 V in 0.2 V steps.

of Tech-B is shown in Fig. 13. If we adopt the criteria of noise margin being at least 0.4 V_{dd}, and the inverter gain being at least four, this inverter will stay operational down to $V_{dd} = 0.2$ V. Current drives of DTMOS and standard MOSFET are compared in Fig. 14 for Tech. B. DTMOS drain

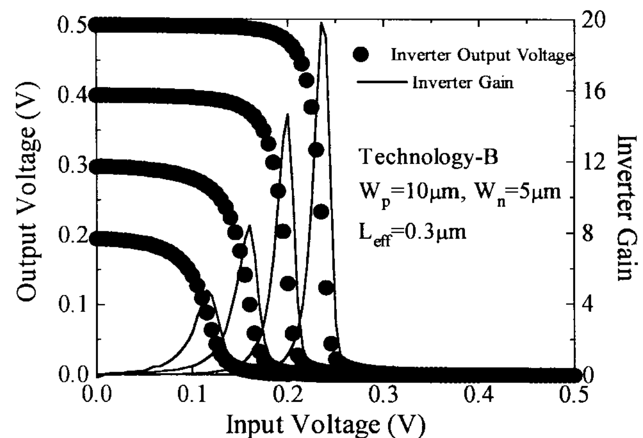


Fig. 13. Inverter dc transfer characteristics. PMOS and NMOS devices forming the inverter are DTMOS. Full power supply voltage swing is obtained down to $V_{dd} = 0.2$ V.

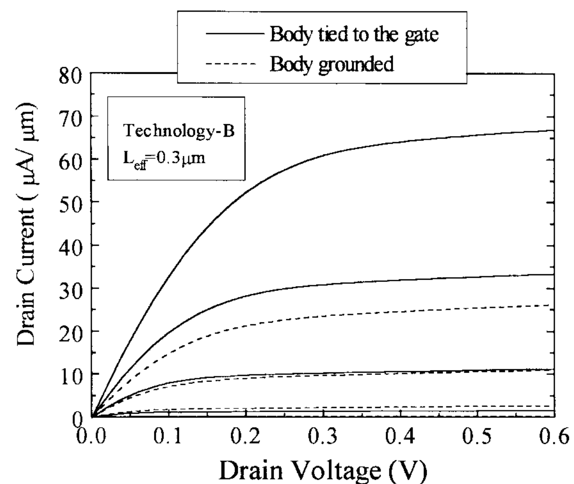


Fig. 14. Drain current of an SOI NMOSFET operated as a DTMOS (body tied to the gate) and as a standard MOSFET (body grounded). V_{gs} varies from 0.2 to 0.6 V in 0.1 V steps.

current is 2.5 times that of the standard device at $V_{gs} = 0.6$ V, and 5.5 times that of the standard device at $V_{gs} = 0.3$ V. Again, the subthreshold currents of these two devices are identical at $V_{gs} = 0$.

As was mentioned in Section III-A, DTMOS gate capacitance is larger than the standard MOSFET gate capacitance. However, gate capacitance is only a portion of total switching capacitance, and current drive of DTMOS is much higher than that of the standard MOSFET. Therefore, DTMOS gates are expected to switch faster than regular MOSFET's. A combination of experimental data and mixed-mode simulation results are used to evaluate the ac performance of DTMOS: standard CMOS, and DTMOS-based CMOS ring oscillators were fabricated by the same process, with the results shown in Fig. 15. Since threshold voltages of devices used in the ring oscillator were high in Tech-A ($V_{to} = 0.67$ V), optimum performance was not achieved for low power supply voltages. For Tech-B, ring oscillators are not available. We assume that gate capacitance in an older technology A amounts to one third of total capacitance, and $C_{ox}(\text{Tech-A})/C_{ox}(\text{Tech-B}) = 64/100$ (Table I), while junction and interconnect capacitances

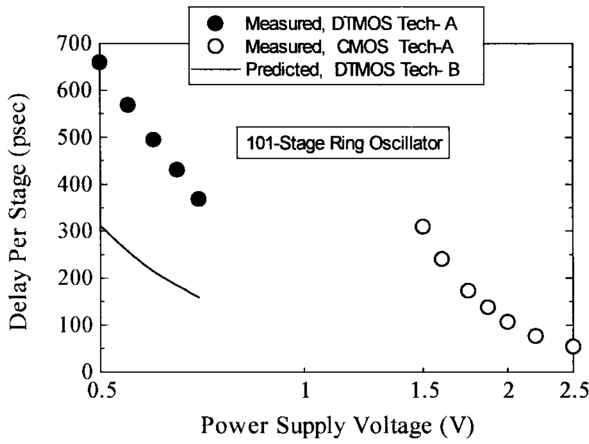
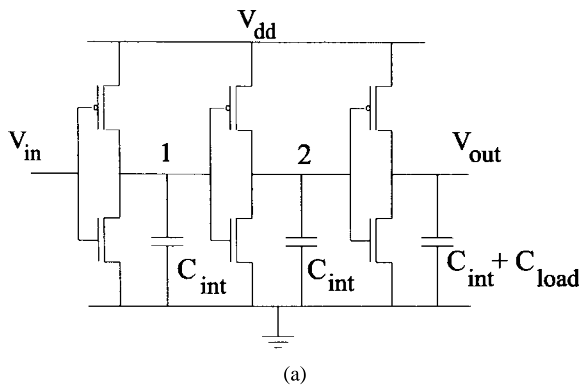
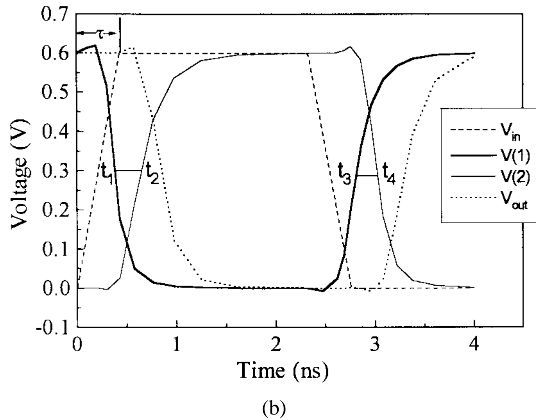


Fig. 15 . elay of a 101-stage ring oscillator. Solid line shows the predicted delay of Tech-B with $L_{eff} = 0.3\ \mu$m.



(a)



(b)

Fig. 16. (a) The inverter chain used in TMA-MEDICI mixed mode simulations. Gate delay is measured between nodes 1 and 2. C_{int} was chosen to be 70 fF. $(W/L)_n = (5\ \mu\text{m}/0.3\ \mu\text{m})$, and $(W/L)_p = (10\ \mu\text{m}/0.3\ \mu\text{m})$. (b) Typical waveforms of different nodes in (a). Initial rise time of the input signal is shown as τ. A unit gate delay is defined by $t_{pd} = (t_2 - t_1 + t_4 - t_3)/2$.

remain the same. The solid line in Fig. 15 shows the expected delay of a ring oscillator based on Tech-B devices, obtained by dividing the measured delay of Tech-A by the ratio of measured I_{dsat}'s of Tech-B and Tech-A, and then increasing it by a capacitance factor.

To further compare the ac performance of DTMOS with the standard device, mixed-mode simulations were carried out by employing the 2-D device simulator TMA-MEDICI [9]. The simulation is based on an inverter chain, as shown in Fig. 16(a). The delay time definition is shown in Fig. 16(b),

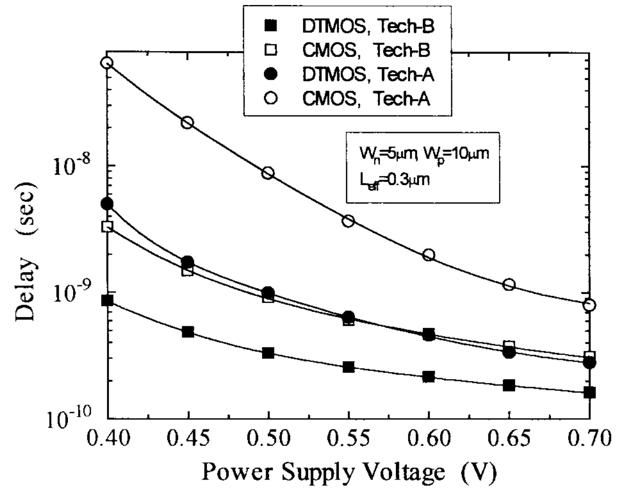
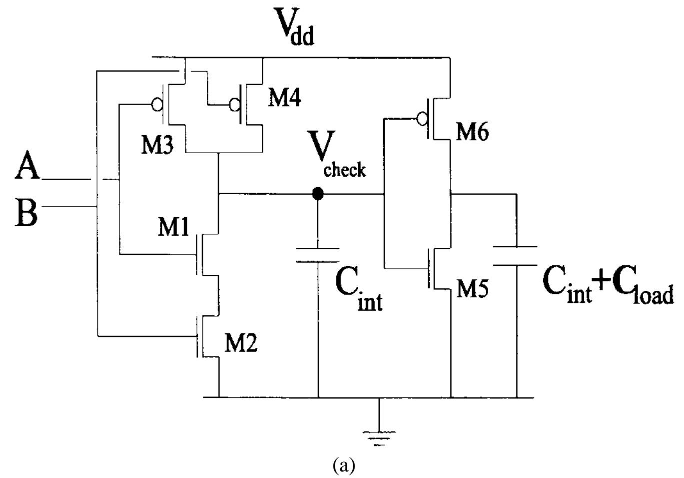
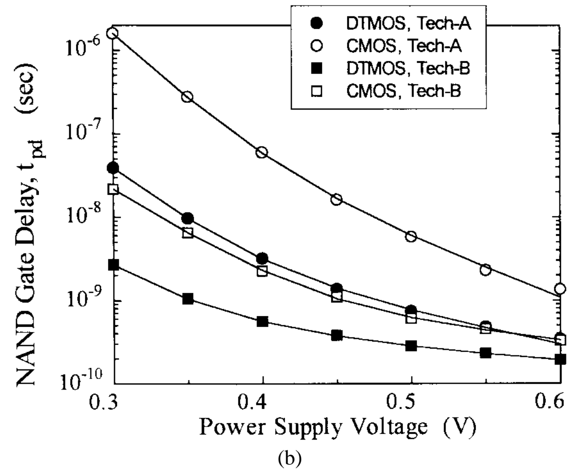


Fig. 17. Simulated delays obtained from the inverter chain of Fig. 16(a). The 2-D device simulator TMA-MEDICI used in this work.



(a)



(b)

Fig. 18. (a) A two-input NAND gate with an inverter as its load is used in MEDICI simulations. Device sizes are as follows: for the NAND gate $(W/L)_p = (8\ \mu\text{m}/0.3\ \mu\text{m})$ and $(W/L)_n = (5\ \mu\text{m}/0.3\ \mu\text{m})$, for the innovator $(W/L)_p = (10\ \mu\text{m}/0.3\ \mu\text{m})$and $(W/L)_n = (5\ \mu\text{m}/0.3\ \mu\text{m})$. The value of C_{int} is equal to the total stage gate capacitance. Node A was assumed to be high and node B was pulsed. (b) Simulated delays obtained using the NAND gate of (a). The reported delay is computed between input nodes and the node named V_{check}.

and described by the following formula [10]:

$$t_{pd} = \frac{t_2 - t_1 + t_4 - t_3}{2}. \tag{8}$$

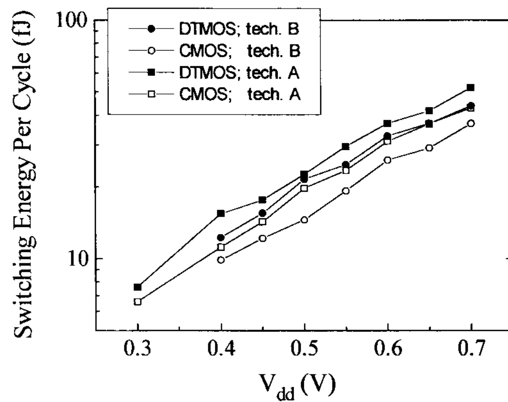


Fig. 19. Switching energy per cycle in a DTMOS and a standard CMOS inverter.

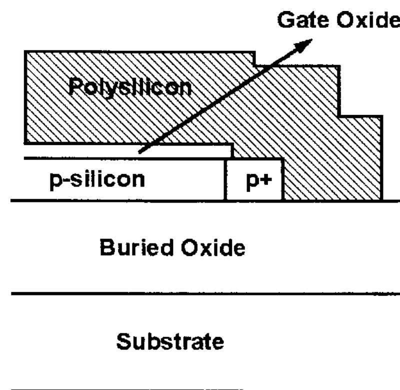
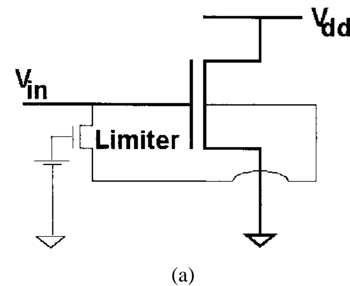
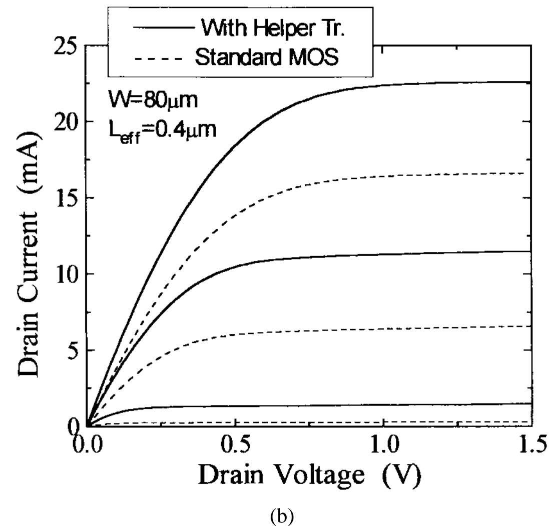


Fig. 20. A buried contact method suggested for shorting the gate to the body.



(a)



(b)

Fig. 21. (a) A small "limiter" transistor is used to provide forward bias for the large transistor. The "limiter" clamps the forward bias to only 0.6 V, independent of the power supply voltage. (b) Drain current of a large NMOS device with and without the "limiter" transistor. V_{gs} is varied from 0 to 1.5 V in 0.5 V steps. The limiter transistor width is 2 μm.

The first inverter in the chain is driven by a waveform with linear rise and fall shown in Fig. 16(b), with the initial rise time τ. Since the delay time is extracted from the second inverter, this initial rise time does not affect the result appreciably. Nonetheless, for higher accuracy, we iterated the simulation process and adjusted the value of τ to nearly match the output signal of the second inverter. We assume that the stage interconnect capacitance dominates and equal to 70 fF, which is respectively, 4.5 and 3 times larger than the total gate capacitance of a stage for Technologies A and B. Tech-A and Tech-B were both simulated, with the results shown in Fig. 17.

Employing a similar approach as above, a two-input NAND gate (with an inverter as the load) was simulated. The circuit diagram is shown in Fig. 18(a). In this case we assume the stage load interconnect capacitance C_{int} to be equal to the total stage gate capacitance, which explains why simulated NAND gate has a smaller delay than a simulated inverter. The worst case values of t_{pdHL} and t_{pdLH} were computed and averaged for DTMOS and standard CMOS cases, with the results shown in Fig. 18(b). All of the above results indicate that speed of DTMOS circuit is superior to that of the standard MOSFET by two to ten times. The improvement is the biggest if the interconnect capacitance dominates.

DTMOS has a slightly higher dynamic power dissipation due to a higher current drive, or a higher effective gate capacitance, as shown in (6). This is depicted in Fig. 19, where switching energy of DTMOS inverter is compared to the one of standard CMOS inverter. The dynamic power dissipation is marginal compared to speed enhancement. DTMOS however has a nonzero static power dissipation component. From the base current of Fig. 11, we can estimate that for 10^7 transistors (50% NMOS, 50% PMOS), each 1 μm wide, with $V_{dd} = 0.6$ V, total static power dissipation will be equal to 0.3 W which is small for a large microprocessor chip. Note that a process that can reduce forward biased diode current will further improve static power dissipation in DTMOS.

IV. Discussion and Conclusion

DTMOS devices described and analyzed in the previous sections by no means represent the optimum realization of DTMOS. These structures can be improved in several fronts, some of which are discussed below. The DTMOS structure depicted in Fig. 3 (and utilized in the ring oscillators) has extra parasitic capacitance around the gate-to-body contact. This capacitance adds to the total switching capacitance and degrades the DTMOS ac performance. Other methods of shorting the body to the gate that eliminate this capacitance are feasible. For example, it is not necessary to use the metal for shorting the body to the gate, as a buried contact concept can be exploited: after the gate oxidation a thin layer of polysilicon (approximately 20–30 nm) is deposited. Next, a mask is used to implant the selected area and to create a contact window by etching the polysilicon layer and the underlying oxide. Subsequently, a thick layer of polysilicon is deposited. This polysilicon layer will be shorted to the silicon film directly

in the contact window. Fig. 20 illustrates this configuration. Body-to-gate connection at the device edge (Fig. 3) has the drawback that a wide device may have nonuniform threshold voltage along its width. Providing this connection at both edges of the device, and implementing a wide device as several narrower transistors will alleviate this problem. Also, the n^+p^+ diode between the n^+-doped poly and p^+ Si film region poses no problem since the voltage across it will be equal to zero in DTMOS.

In DTMOS, power supply voltage is limited to about 0.6 V or less because of the base current. To mitigate this limitation, an external V_{bs}-limiting scheme can be used: a small transistor is employed to provide the forward bias for the large MOSFET, as illustrated in Fig. 21(a). The small "limiter" transistor clamps the forward bias to only 0.6 V. Although a harsh area penalty is imposed on minimum size devices, the proposed scheme works particularly well for large transistors, such as clock drivers and large buffers. Fig. 21(b) experimentally demonstrates the operation of this circuit for Tech-B. A separate bias voltage may be avoided for the transistor by making this device a depletion mode MOSFET and grounding its gate, or an enhancement device with the gate connected to V_{dd}.

In conclusion, we have shown that a MOSFET can have a high V_t at $V_{gs} = 0$ to achieve low leakage and a low V_t and $V_{gs} = V_{dd}$ to achieve high speed. This dynamic variability becomes more beneficial for low power operation at very low voltages. By tying the gate and the body of an SOI MOSFET together, a Dynamic Threshold Voltage MOSFET (DTMOS) is obtained. DTMOS has the theoretically ideal subthreshold swing and higher carrier mobility than the standard MOSFET. Furthermore, DTMOS threshold voltage drops as the gate voltage is raised, resulting in a much higher current drive than a conventional bulk or SOI MOSFET. As the ac and dc experimental and simulation results demonstrate, DTMOS is a good candidate for very low voltage operation. DTMOS also solves the floating body problems of SOI MOSFET's such as transient kink and V_t stability. DTMOS can also be implemented in a bulk technology.

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