A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operation

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Abstract— **A new mode of operation for Silicon-On-Insulator (SOI) MOSFET is experimentally investigated. This mode gives rise to a Dynamic Threshold voltage MOSFET (DTMOS). DTMOS threshold voltage drops as gate voltage is raised, resulting in a much higher current drive than regular MOSFET at low V_{dd}. On the other hand, V_t is high at $V_{gs} = 0$, thus the leakage current is low. Suitability of this device for ultra low voltage operation is demonstrated by ring oscillator performance down to $V_{dd} = 0.5$ V.**

I. Introduction

During the past few years demand for low power and high performance digital systems has grown rapidly. The main approach for reducing power has relied on power supply scaling. Since power supply reduction below $3V_t$ will degrade circuit speed significantly, scaling of power supply should be accompanied by threshold voltage reduction. However, the lower limit for threshold voltage is set by the amount of off-state leakage current that can be tolerated (due to standby power consideration in static circuits, and avoidance of failure in dynamic circuits and memory arrays). To extend the lower bound of power supply, we propose a **D**ynamic **T**hreshold voltage **MOSFET** (DTMOS) with the highest V_t at zero bias and the lowest value at $V_{gs} = V_{dd}$. In the remainder of this paper we will describe the operation of the device, and show its superiority over a regular MOSFET. We will also show some circuit performances using DTMOS.

II. Experiment and Results

The SOI devices used in the study are built on SIMOX wafers. Mesa active islands (MESA) were created by plasma-etching a nitride/oxide/silicon stack stopping at buried oxide. P+ polysilicon gate was used for PMOSFET's and N+ for NMOSFET's. The buried oxide thickness was 370 nm–400 nm, and the silicon film thickness was 130 nm–160 nm. A four-terminal layout was used to provide separate source, drain, gate, and body contacts. Besides the four-terminal layout, devices with local gate-to-body connections were also fabricated as illustrated in Fig. 1. This connection uses an oversized metal to P+ contact window aligned over a "hole" in the poly gate [1]. The metal shorts the gate and P+ region. Thus, there is no significant penalty in area.

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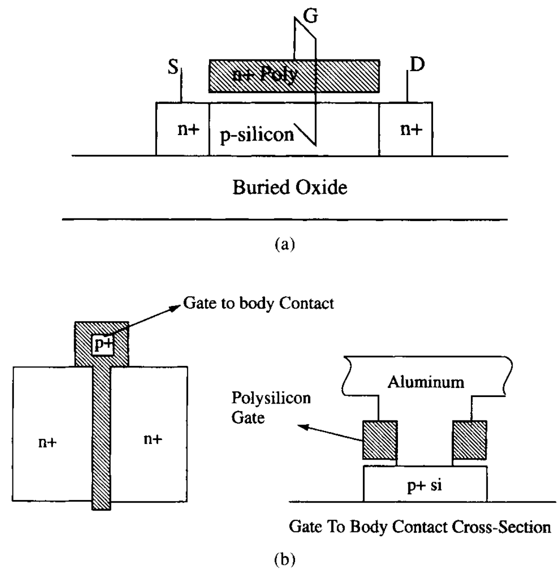

Fig. 1. (a) Cross section of an SOI NMOSFET with body and gate tied together. (b) Gate to body connection by using aluminum to short the gate and P+ region.

To operate the DTMOS, floating body and gate of a Silicon-On-Insulator (SOI) MOSFET are tied together. This is not a new configuration, as [1]–[3] have already suggested it. However, [1]–[3] all tried to exploit the extra current produced by the lateral bipolar transistor. This normally requires the body voltage to be larger than 0.6 V. Since current gain of the bipolar device is small, extra drain (collector) current comes at cost of excessive input (base) current, which contributes to the standby current. We will show that most of the improvement can be achieved when gate and body voltages are kept below 0.6 V. This also ensures that base current will stay negligible. Although the same idea can be used in bulk devices, better advantage is reached in SOI, where because of very small junction areas base current and capacitances are appreciably reduced.

Fig. 2 illustrates the NMOS behavior, with a separate terminal used to control the body voltage. The threshold voltage at zero body bias is denoted by V_{to}. Body bias effect is

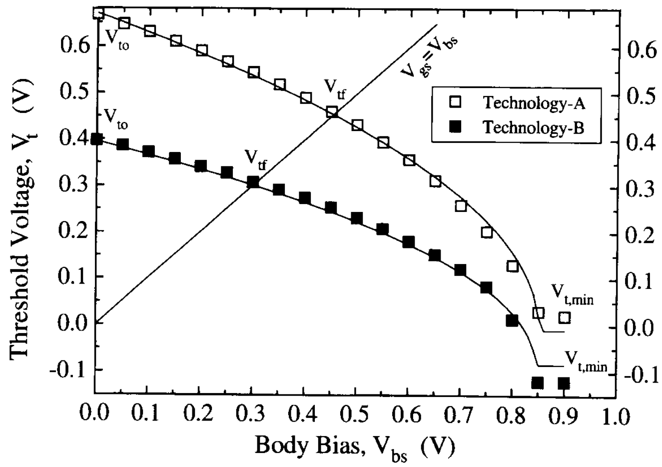

Fig. 2. Threshold Voltage of SOI NMOSFET as a function of body-source forward bias. For Technology-A $T_{ox} = 10$ nm, $N_a = 2.5 \times 10^{17}$ cm^{-3}. For Technology-B $T_{ox} = 6.4$ nm $N_a = 3 \times 10^{17}$ cm^{-3}.

normally studied in the reverse bias regime, where threshold voltage increases as body to source reverse bias is made larger. We propose to use the exact opposite regime. Namely, we "forward bias" the body-source junction (at less than 0.6 V), forcing the threshold voltage to drop.

Specifically, this forward bias effect is achieved by connecting the gate to the body. This is shown as $V_{gs} = V_{bs}$ line in Fig. 2. The intersect of V_t curve and $V_{gs} = V_{bs}$ line determines the point where gate and threshold voltages become identical. This point, which is marked as V_{tf}, is the DTMOS threshold voltage. This lower threshold voltage does not come at expense of higher off-state leakage current, as at $V_{bs} = V_{gs} = 0$ DTMOS and regular device have the same V_t. In fact, they are identical in all respects and consequently have the same leakage. This is clearly seen in Fig. 3. Reduced V_{tf} compared to V_{to} is attained through a theoretically ideal subthreshold swing of 60 mV/dec. Fig. 3 demonstrates this for PMOS and NMOS devices operated in DTMOS mode and in regular mode. Subthreshold swing is 80 mV/dec in the regular devices.

This is not the only improvement. As the gate of DTMOS is raised above V_{tf}, threshold voltage drops further. The threshold voltage reduction continues until $V_{gs} = V_{bs}$ reaches $2\Phi_b$, and threshold voltage reaches its minimum value of $V_{t,\min} = 2\Phi_b + V_{fb}$. For example, for technology-B in Fig. 2, at $V_{gs} = V_{bs} = 0.6$ V, $V_t = 0.18$ V compared to $V_{to} = 0.4$ V. In DTMOS operation the upper bound for applied $V_{gs} = V_{bs}$ is set by the amount of base current that can be tolerated. This is illustrated in Fig. 3, where PMOS and NMOS device body (base) currents are shown. At $V_{gs} = 0.6$ V base currents for both PMOS and NMOS devices are less than 2 nA/μm. For larger values of V_{gs} the body current can become excessive. Current drives of DTMOS and regular MOSFET are compared in Fig. 4, for technology-B of Fig. 2. DTMOS drain current is 2.5 times of regular device at $V_{gs} = 0.6$ V, and 5.5 times of regular device at $V_{gs} = 0.3$ V. The improved DTMOS current drive is due to

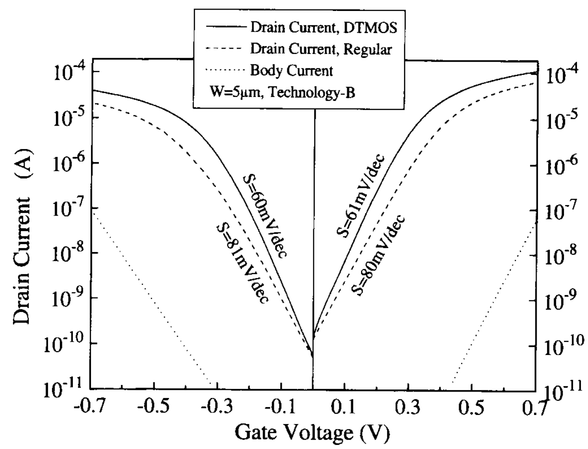

Fig. 3. Subthreshold characteristics of SOI NMOSFET and PMOSFET operated with body grounded and body tied to the gate. Body to source currents are also shown for the case of DTMOS (body tied to the gate).

the following: 1) Inversion charge is increased, as $dQ_n = C_{ox}\left(dV_g - \frac{\partial V_t}{\partial V_g} dV_g\right) \rightarrow C_{eff} = C_{ox}\left(1 + \left|\frac{\partial V_t}{\partial V_g}\right|\right)$. Thus, DTMOS leads to an effectively thinner oxide. 2) DTMOS carrier mobility is higher because the depletion charge is reduced and the effective normal field in the channel is lowered [4]. We realize that DTMOS gate capacitance is larger than regular MOS gate capacitance. However, gate capacitance is only a portion of total capacitance, and current drive of DTMOS is much higher than that of regular MOS. Thus, DTMOS gates are expected to switch faster than regular MOS gates.

AC performance of DTMOS is evaluated by an unloaded 101-stage CMOS ring oscillator. Fig. 5 plots the delay of each stage versus power supply. We emphasize that since the threshold voltages of devices used in the ring oscillator were high (technology-A), the optimum performance was not achieved. For technology-B, ring oscillators are not available.

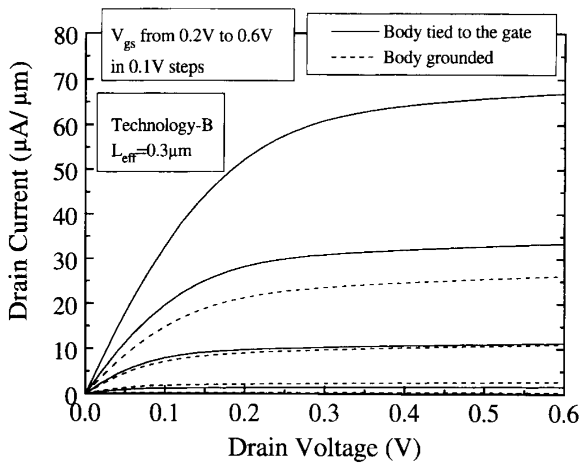

Fig. 4. Drain current of an SOI NMOSFET operated as a DTMOS and as a regular device.

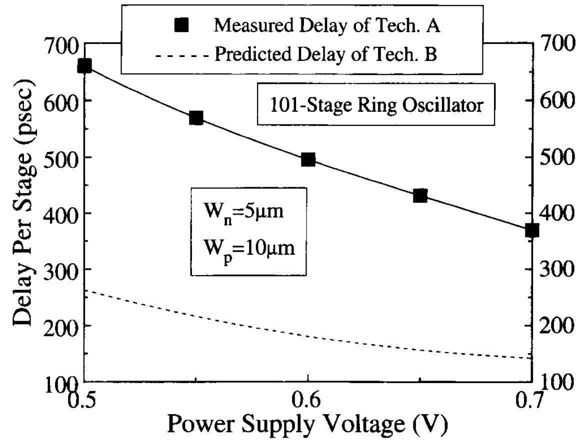

Fig. 5. Delay of a 101-stage ring oscillator. The PMOS and NMOS devices in the ring are DTMOS with $T_{ox} = 10$ nm, and $L_{eff} = 0.3\ \mu$m, $V_{to} = 0.6$ V. The dashed line is prediction of delay for a ring oscillator based on Technology-B ($T_{ox} = 6.4$ nm, $N_a = 3 \times 10^{17}$ cm^{-3}, $N_d = 3 \times 10^{17}$ cm^{-3}) with $L_{eff} = 0.3\ \mu$m.

If the devices based on technology-B are used, the expected delay for unloaded ring oscillator can be calculated by the following equation [5]: $\tau_{pd} = \frac{C}{4} V_{dd}\left(\frac{1}{I_{dsatn}} + \frac{1}{I_{dsatp}}\right)$. This is shown as the dashed line in Fig. 5, where C = 200 fF is used for $W_n = 5\ \mu$m and $W_p = 10\ \mu$m. This value for C was obtained by fitting the equation to the measured τ_{pd} of technology-A.

Finally, in the present form of body-gate connection (Fig. 1) a wide DTMOS may have non-uniform threshold voltage along its width. This warrants investigating other connection schemes.

III. Conclusion

For low power operation at very low voltages, a MOSFET should ideally have a high V_t at $V_{gs} = 0$ to achieve low leakage and low V_t at $V_{gs} = V_{dd}$ to achieve high speed. By tying body and gate of an SOI MOSFET together, a dynamic threshold voltage MOSFET (DTMOS) is obtained. This device has ideal 60 mV/dec subthreshold swing. DTMOS threshold voltage drops as gate voltage is raised, resulting in much higher current drive than regular MOSFET. DTMOS is ideal for very low voltage (< 0.6 V) operation, as demonstrated by ring oscillator data. DTMOS also solves the floating body problems of SOI MOSFET such as kinks and V_t stability. Furthermore, carrier mobility is enhanced.

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