A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation

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Abstract

To extend the lower bound of power supply to ultra-low voltages (0.6V and below), we propose a **D**ynamic-Threshold Voltage **MOS**FET (DTMOS) built on **S**ilicon-**O**n-**I**nsulator (SOI). The threshold voltage of DTMOS drops as the gate voltage is raised, resulting in a much higher current drive than standard MOSFET at low power supply voltages. On the other hand, V_t is high at V_{gs}=0, therefore the leakage current is low. We provide experimental results and 2-D device and mixed-mode simulations to analyze DTMOS and compare its performance with a standard MOSFET. These results verify excellent DC inverter characteristics down to V_{dd}=0.2V, and good ring oscillator performance down to 0.3V for DTMOS.

Introduction

In CMOS digital circuits delivered power is proportional to the square of power supply voltage. Thus, the main effort for reducing power in these systems has been focused on power supply scaling. Since reducing V_{dd} below three times the threshold voltage ($3V_t$) will significantly degrade circuit speed, scaling of V_{dd} should be accompanied by threshold voltage reduction. However, the lower limit of threshold voltage is set by the amount of off-state leakage current that can be tolerated (due to standby power consideration in static circuits, and avoidance of failure in dynamic circuits and memory arrays). It is seen that if standard MOSFETs are used, a lower bound for V_{dd} becomes inevitable. To extend the lower bound of power supply to ultra-low voltages (0.6V and below), we propose a **D**ynamic Threshold Voltage **MOS**FET (DTMOS) with the highest V_t at zero bias and the lowest value at $V_{gs}=V_{dd}$.

Device Fabrication

The SOI devices used in the study were built on SIMOX and BESOI wafers. The buried oxide thickness was 370-400nm for SIMOX wafers and approximately 1µm for BESOI wafers. The final SOI film thickness varied from 130nm to 160nm. Mesa active islands were created by plasma-etching a nitride/oxide/silicon stack stopping at buried oxide. A 100-nm oxide was grown on the mesa sidewalls to prevent low-V_t devices and gate oxide defects at the mesa corners. Threshold implants were then performed, resulting in concentrations of 1.5-3x10^{17}cm^{-3}. Gate oxides of 6.4nm and 10nm were grown, followed by the deposition of 300nm of undoped polysilicon. Oxygen plasma "ashing" was done to the gate photoresist to achieve effective channel lengths down to 0.2µm [1]. High-dose arsenic and boron source/drain and polysilicon gate implants were used to create NMOSFETs and PMOSFETs with N^+ and P^+ poly gates, respectively. The combination of silicon film thickness, doping concentration and gate type resulted in non-fully depleted (NFD) devices.

A four-terminal layout was used to provide separate source, drain, gate, and body contacts. This allows for operation of the device in the standard mode, or in DTMOS mode: The body is either floated or grounded in the standard MOSFET mode. The body is tied to the gate in the DTMOS mode, shown in Fig. 1a. Besides the four-terminal layout, DTMOS devices with local gate-to-body connections were also fabricated as shown in Fig. 1b. This connection uses an oversized metal-to-P^+ contact window aligned over a "hole" in the poly gate [2]. The metal shorts the gate and the P^+ region (for N-DTMOS). This contact requires minimal area and no additional processing steps. Standard CMOS and DTMOS-based CMOS ring oscillators were also fabricated in the same process. All device processing was performed in the UC Berkeley Microfabrication laboratory.

Experimental and Simulation Results

In DTMOS the floating body and gate of a Silicon-on-Insulator (SOI) MOSFET are tied together, as illustrated in Fig. 1a. Even though [2-4] also proposed to tie the gate to the body, they all tried to exploit the extra current produced by the lateral bipolar transistor. This requires the body voltage to be **larger than 0.6V**. The extra drain (collector) current comes at the cost of excessive input (base) current, which contributes to the standby current. We report large improvement over standard MOSFET when gate (body) voltage is kept **below 0.6V**. Although the same idea can be used in bulk devices, stronger advantage is reached in SOI, where because of very small junction areas base current and capacitances are appreciably reduced.

Fig. 2 illustrates the NMOS behavior, with a separate terminal used to control the body voltage. The threshold

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voltage at zero body bias is denoted by V_{to}. Body bias effect is normally studied in the reverse bias regime, where threshold voltage increases as body-to-source reverse bias is made larger. We propose to use the exact opposite regime. Namely, we "*forward bias*" the body-source junction (at less than 0.6V), forcing the threshold voltage to drop. At V_{gs} (=V_{bs}) =V_{tf}, V_t is at a desirable and lower value than V_{to}. This lower threshold voltage does not come at the expense of higher off-state leakage current, because at V_{bs}=V_{gs}=0 DTMOS and the standard device have the same V_t. In fact, they are identical in all respects and consequently have the same leakage. Reduced V_{tf} compared to V_{to} is attained through an ideal subthreshold swing of 60mV/dec. Fig. 3 demonstrates this for PMOS and NMOS devices operated in DTMOS mode and in the standard mode.

An equally important improvement is reached above V_{tf} (Fig. 2). As the gate of DTMOS is raised beyond V_{tf}, threshold voltage drops further. For example, for Tech-B in Fig. 2, at V_{gs}=V_{bs}=0.6V, V_t=0.18V compared to V_{to}=0.4V. In Fig. 2, to obtain the sharpest curve (and hence the maximum V_t reduction), the highest acceptable doping should be used. V_{to} then can be adjusted to the desired value by selecting a thin gate oxide or a low work function gate material (Fig. 4). A further advantage of DTMOS is its higher carrier mobility, as seen in Fig. 5. This is due to the fact that in DTMOS the depletion charge is reduced and the effective normal filed in the channel is lowered [5]. In DTMOS operation the upper bound for applied V_{gs}=V_{bs} is set by the amount of base current that can be tolerated. This is illustrated in Fig. 3, where PMOS and NMOS device body (base) currents are shown. At V_{gs}=0.6V base currents for both PMOS and NMOS devices are less than 2nA/μm.

The inverter DC transfer characteristics for DTMOS of Tech-B is shown in Fig. 6. If we adopt the criteria of noise margin being at least $0.2V_{dd}$, and the inverter gain being at least four, this inverter will stay functional down to V_{dd}=0.2V. Current drives of DTMOS and standard MOSFET are compared in Fig. 7 for Tech-B of Fig. 2. DTMOS drain current is 2.5 times that of the standard device at V_{gs}=0.6V, and 5.5 times that of the standard device at V_{gs}=0.3V.

To evaluate the AC performance of DTMOS, standard CMOS and DTMOS-based CMOS ring oscillators were fabricated by the same process, with the results shown in Fig. 8. We emphasize that since the threshold voltages of devices used in the ring oscillator were high (Tech-A) the optimum performance was not achieved for low supply voltages. For Tech-B, ring oscillators are not available. The solid line in Fig. 8 shows the expected delay of a ring oscillator based on Tech-B devices. To further compare the AC performance of DTMOS with the standard device, mixed-mode simulations were carried out by employing the 2-D device simulator TMA-MEDICI [6]. The simulation is based on an element inverter coming from an inverter chain, as shown in Fig. 9. The delay time definition is also shown in Fig. 9, and is described by $t_{tpd}=(t_2-t_1+t_4-t_3)/2$. The first inverter in the inverter chain is driven by a waveform with the initial time τ. Since the delay is calculated from the second inverter, this initial value does not affect the result appreciably. Nevertheless, we iterated the simulation process and adjusted the value of τ to nearly match the input signal to the third inverter. Tech-A and Tech-B were both evaluated, as shown in Fig. 10.

In DTMOS, power supply voltage is limited to about 0.6V. To mitigate this limitation, an external V_{bs}-limiting scheme can be used: A small transistor is used to provide the forward bias for the large transistor, illustrated in Fig. 11. The small "limiter" transistor limits the forward bias to only 0.6V regardless of power supply voltage. This scheme works particularly well for circuits where large transistors are needed, such as clock drivers and large buffers.

Conclusion

A MOSFET should ideally have a high V_t at V_{gs}=0 to achieve low leakage, and low V_t at V_{gs}=V_{dd} to achieve high speed. These requirements become more important for low power operation at very low voltages. By tying gate and body of an SOI MOSFET together, a **D**ynamic **T**hreshold voltage **MOS**FET (DTMOS) is obtained. DTMOS has steeper subthreshold swing and higher carrier mobility than the standard MOSFET. Furthermore, DTMOS threshold voltage drops as the gate voltage is raised, resulting in a much higher current drive than the standard device. As the AC and DC experimental and simulation results demonstrate, DTMOS is a good candidate for very low voltage operation. DTMOS also solves the floating body problems of SOI MOSFETs such as kink and V_t stability.

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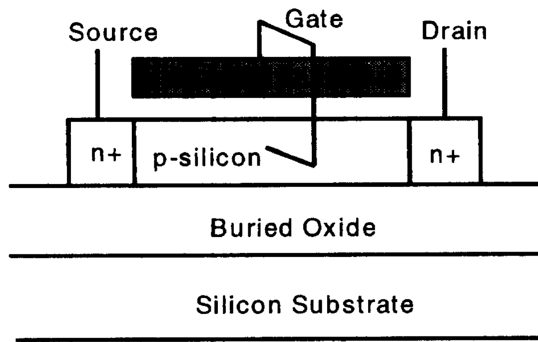

Fig. 1a) Schematic of an SOI NMOSFET with body and gate tied together.

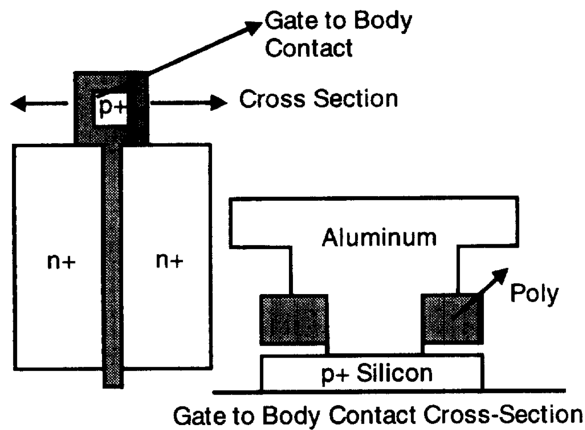

Fig. 1b) Cross section of body-to-gate connection using aluminum to short the gate and the P^+ region. A large contact is aligned over the opening in the polysilicon gate.

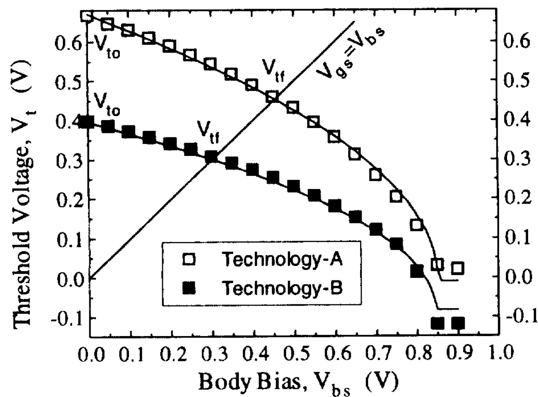

Fig. 2 Threshold voltage of SOI NMOSFET as a function of body-source forward bias. For Tech-A T_{ox}=10nm, N_a=2.5x10^{17}cm^{-3}. For Tech-B T_{ox}=6.4nm, N_a=3x10^{17}cm^{-3}.

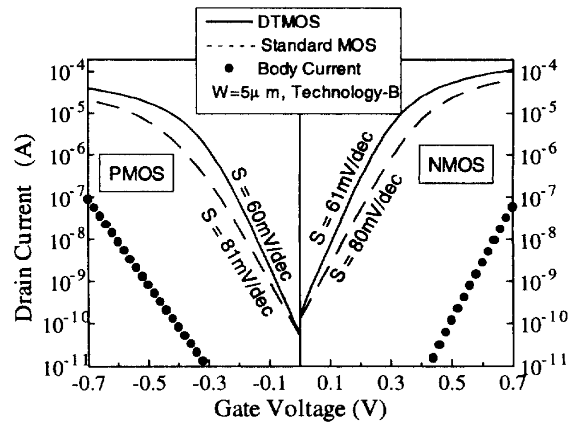

Fig. 3 Subthreshold characteristics of SOI NMOSFET and PMOSFET, with body grounded and body tied to the gate. Body (base) currents for DTMOS devices are also shown.

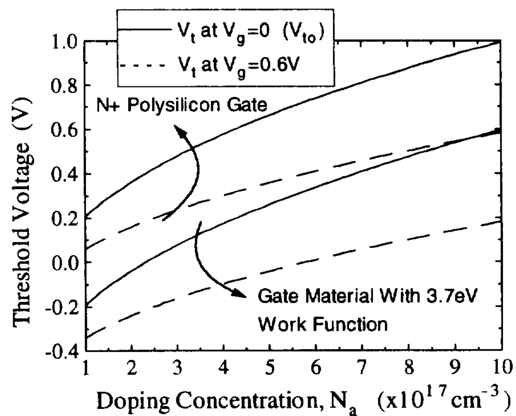

Fig. 4 Threshold voltage of a N-DTMOS at V_{gs}=0 and at V_{gs}=0.6V, as a function of silicon film doping concentration. Two different gate materials are considered. T_{ox}=6.4nm.

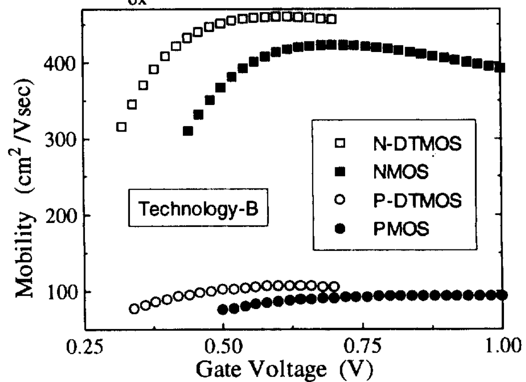

Fig. 5 Electron and hole surface mobility as a function of gate voltage, for standard MOSFET and for DTMOS. T_{ox}=6.4nm, N_a=3x10^{17}cm^{-3}, and N_d=3x10^{17}cm^{-3}.

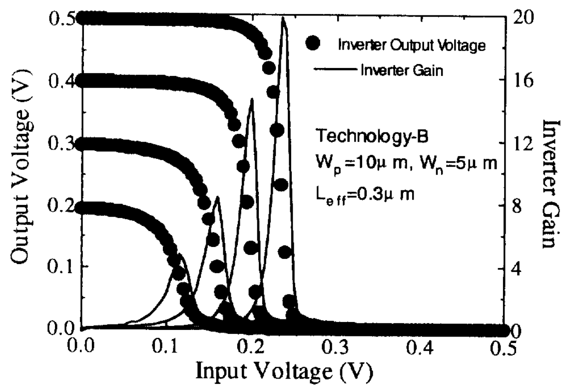

Fig. 6 Inverter DC transfer characteristics. PMOS and NMOS devices forming the inverter are DTMOS.

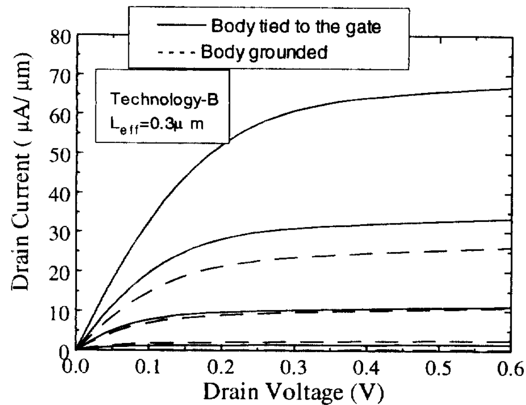

Fig. 7 Drain current of an SOI NMOSFET operated as a DTMOS and as a standard MOSFET. V_{gs} varies from 0.2V to 0.6V in 0.1V steps.

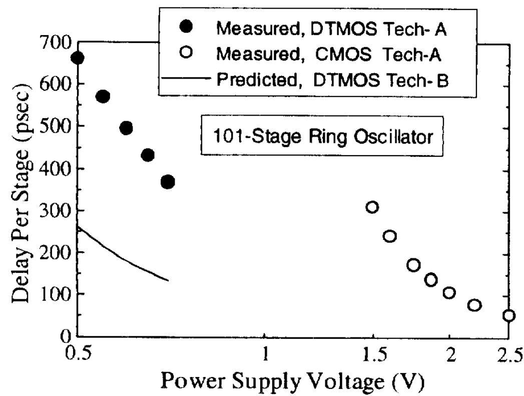

Fig. 8 Delay of a 101-stage ring oscillator. For Tech-A T_{ox}=10nm, L_{eff}=0.3μm, and V_{to}=0.6V. Solid line shows the predicted delay for Tech-B with L_{eff}=0.3μm.

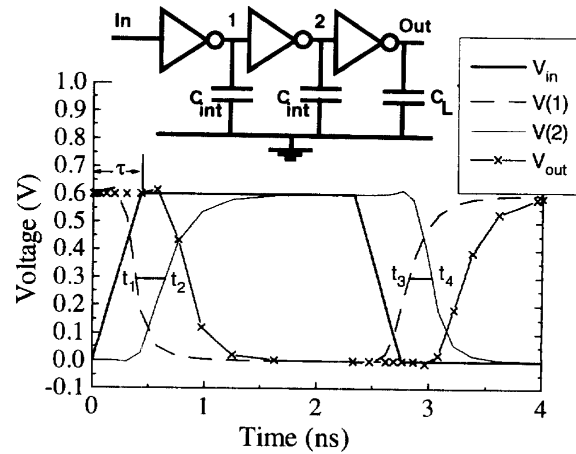

Fig. 9 Typical waveforms of different nodes of the inverter chain used in TMA-Medici mixed mode simulations. Gate delay is measured between nodes 1 and 2. Value of C_{int} was adjusted such that the simulated and measured delays of Tech-A were close.

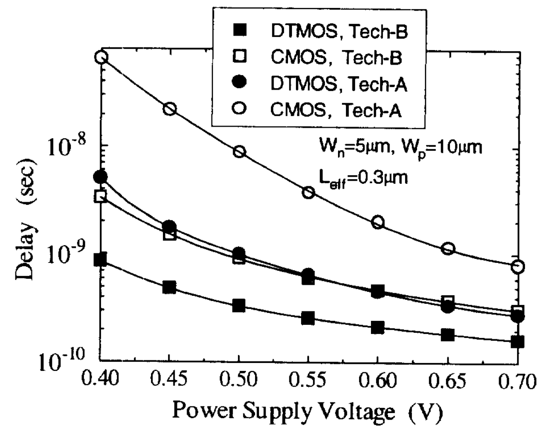

Fig. 10 Simulated delay obtained from inverter chain of Fig. 9. Tech-A and Tech-B parameters are those reported earlier.

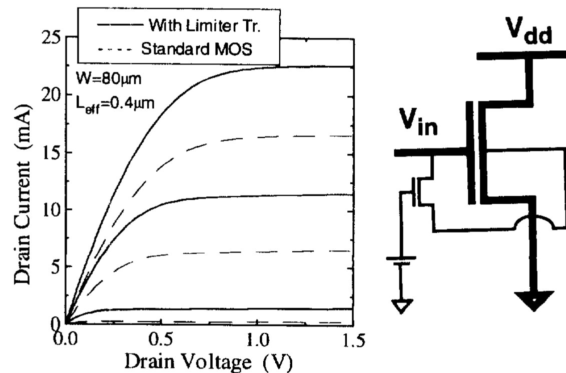

Fig. 11 A small "limiter" transistor is used to provide up to 0.6V of forward bias for the large transistor. V_{gs} is varied from zero to 1.5V in 0.5V steps. The "limiter" transistor width is 2μm.