Saturation Velocity and Velocity Overshoot of Inversion Layer Electrons and Holes

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Abstract

In this paper we address the effect of a wide range of parameters on the high-field transport of inversion layer electrons and holes. The studied parameters include substrate doping level, surface micro-roughness, nitridation of the gate oxide, and device channel length. Our findings point to electron velocity overshoot at room temperature, dependence of electron and hole saturation velocity on nitridation of the gate oxide, and relative insensitivity of electron and hole mobility and saturation velocity to moderate surface roughness.

Introduction

Saturation velocity plays a significant role in MOSFET performance. This role becomes more important as the device channel length shrinks to deep-submicron regime. Widely used simulators employ 1×10^7 cm/sec as the saturation velocity of electrons in the inversion layer even though many direct measurements have indicated a lower value [1-4]. There is even a greater discrepancy for hole inversion-layer velocity. Furthermore, these so called "Drift-Diffusion" simulators do not take velocity overshoot into account. Recent reports have shown that this effect should not be ignored in very short devices [2, 5]. On the other hand, "Energy-Balance" simulators, which can correctly simulate this effect, employ parameters (such as relaxation times) that need calibration and should be adjusted by comparison with experimental results. We employ special test structures built on Silicon-On-Insulator (SOI) and bulk wafers to accurately measure the high-field drift velocity of inversion layer electrons and holes. We report the effect of several important process and device parameters on the inversion-layer carrier velocity.

Experiment Setup

A) Measurement Condition

Uniformity of the tangential field and inversion charge concentration is necessary for the study of high-field or "saturation" regime. To achieve this condition we use the method reported in [1, 2]. Namely, very thick gate-oxide MOSFETs are utilized in the study, and the drain voltage is limited to small values (below 1V). By setting the gate voltage much larger than the drain voltage, uniformity of the inversion charge and field is assured. Since deep-submicrometer devices are used in the study (L_{eff} from 0.5μm to 0.1μm), this drain voltage is sufficient for creating large tangential electric fields. Both bulk and SOI MOSFETs with T_{ox}=50nm are fabricated. In case of bulk MOSFETs, a large reverse body bias is used to improve the charge and field uniformity. For SOI devices, due to the full depletion of silicon film, and the large thickness of buried oxide layer, the tangential field is very uniform and reverse body bias is not needed. We found it important to use extensive 2-D device simulations to verify the uniformity of charge and field. A typical case is shown in Fig. 1, where conduction and valence bands are shown for a 0.4μm SOI device. The linearity of conduction band at the interface points to the uniformity of the tangential field. For this device the gate oxide thickness, the silicon film thickness, and the buried oxide thickness are 50nm, 70nm, and 400nm, respectively. Gate voltage is 30V and drain voltage is 1V.

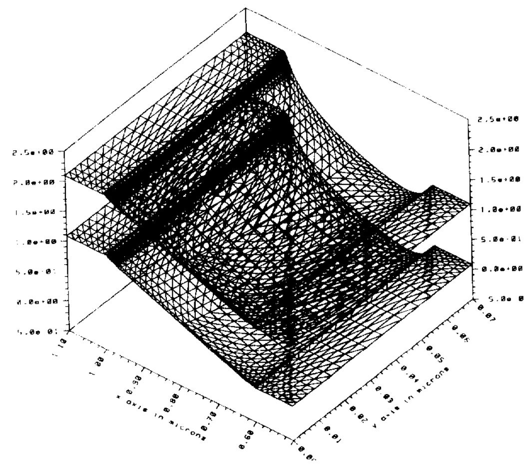

Fig. 1 Conduction and valence bands in the SOI test structure with V_g=30V and V_d=1V. The linearity of potential (and thus uniformity of field) in the inversion layer (closer boundary) is obvious.

Because of charge and field uniformity, the current can be simply written as $I=C_gW(V_g-V_t)\upsilon$, where C_g is the gate

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oxide capacitance, V_t is the threshold voltage, W is the channel width, and υ is the drift velocity. Since υ is the only unknown in this relation, it can be determined from the measured current. The tangential field is given by $E_y=(V_d-IR_{sd})/L_{eff}$, where R_{sd} is the source and drain series resistance. Using above relations drift velocity can be obtained as a function of tangential field. For ultra-short devices, correction of V_t as a function of drain voltage is required, due to drain-induced barrier lowering (DIBL).

B) Nitridation of Gate Oxide

Boron penetration from P^+ polysilicon gates into underlying silicon substrate associated with surface-channel PMOSFETs is a critical issue in dual-gate CMOS processes. It has been shown that nitridation of the gate oxide can provide a barrier to boron penetration [6-7]. Nitirided gate oxides also have exhibited improved hot-carrier reliability, and reduced radiation degradation [6, 8}. Surface mobility has been shown to be lowered by nitridation, but the effect of oxide nitridation on saturation velocity has not been studied. Thermal nitridation of the gate oxide in our samples was achieved by post-oxidation anneal at atmospheric pressure in N_2O at 950C for 20 minutes. A typical compositional profile of N, Si, and O in the gate oxide determined by Auger electron spectroscopy (AES) is shown in Fig. 2.

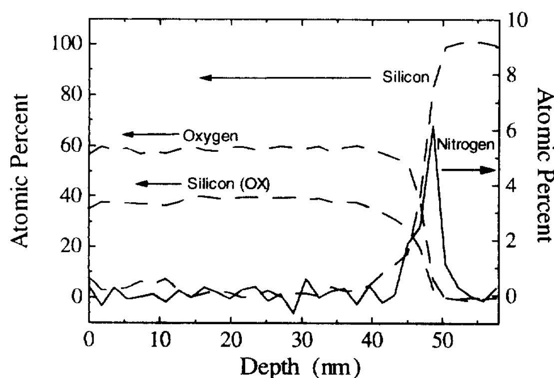

Fig. 2 Depth compositional profile for a 50nm N_2O-annealed oxide. Note the nitrogen pile up at the silicon-oxide interface.

C) Surface Micro-Roughness

There have been conflicting reports on the influence of surface micro-roughness on inversion-layer carrier transport. To study the effect of surface micro-roughness on the transport of carriers, the silicon-oxide interface was intentionally roughened by prolonged DI-water rinsing after the HF clean and just before the gate oxidation [9]. The surface micro-roughness was measured on control samples by using Atomic Force Microscopy (AFM). The initial RMS roughness of about 0.5nm increased to approximately 2nm after 2000 minutes of DI water rinsing.

D) Doping Concentration

To study the effect of substrate doping level on the inversion carrier transport the device doping concentrations were adjusted to three values of $8x10^{16}cm^{-3}$, $1.5x10^{17}cm^{-3}$ and $2.5x10^{17}cm^{-3}$.

Experimental Results

Fig. 3 shows the effective electron mobility as a function of effective vertical field. As seen, all samples match the "universal" mobility curve [10] fairly well, except for the nitrided sample. In particular, no mobility degradation is observed for the SOI wafer, or for the roughened bulk wafer. The behavior of electron mobility for the nitrided sample is in general agreement with other reports. Namely, at low effective vertical fields a nitrided sample has electron mobility less than the "universal" value, while at high vertical fields the trend is reversed. The crossover point has been shown to be a function of N_2O anneal time and temperature [8].

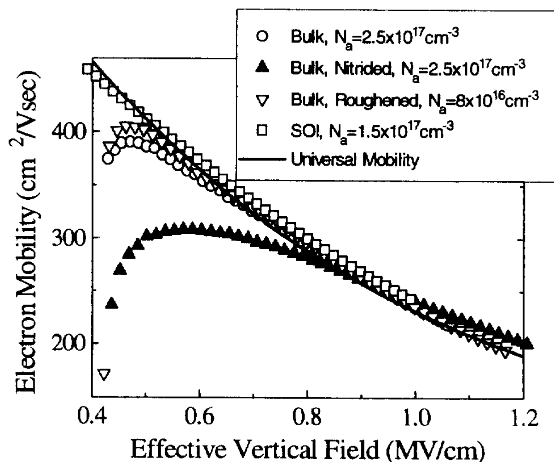

Fig. 3 The effective electron mobility versus effective vertical field. E_{eff} is calculated from $E_{eff}=(0.5Q_n+Q_b)/\varepsilon_{si}$, where Q_n is obtained from integrating the gate to channel capacitance against the gate voltage. The SOI wafer is unpolished SIMOX.

Fig. 4 illustrates the measured electron velocity as a function of tangential field. The test structure length is approximately 0.3µm for all of the samples. Fig. 4 indicates that insensitivity of electron transport to roughness and doping level in the low field, also extends to the high-field

"saturation" regime. Moreover, nitridation of the gate oxide has negative impact on both electron mobility and saturation velocity, under moderate effective vertical fields.

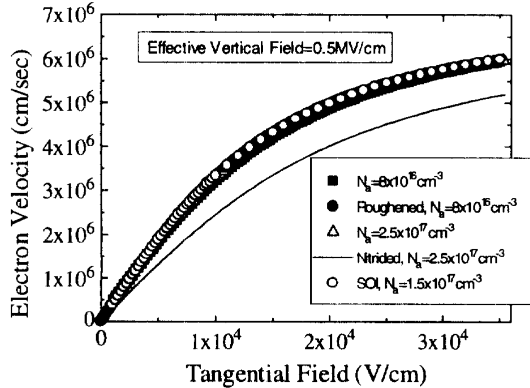

Fig. 4 The electron velocity versus applied tangential field. The test structure length is about 0.3μm for all of the samples.

Fig. 5 points to another important finding; namely, observation of velocity overshoot. As seen, for test structure lengths of 0.3μm or longer, electron velocity is nearly the same, but it increases for shorter lengths. Fig. 6 further illustrates this fact.

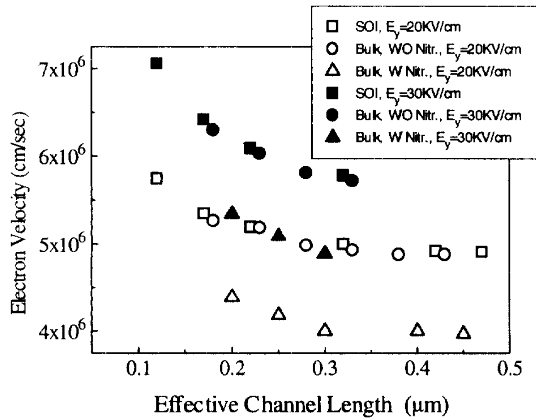

Fig. 5 The electron drift velocity as a function of test structure length, for two different tangential fields of 20KV/cm and 30KV/cm. SOI, bulk, and nitrided bulk samples are compared.

Fig. 7 conveys similar information for T=85K, except that velocity overshoot is more pronounced. In fact, average *inversion-layer* velocity exceeds *bulk* electron saturation velocity by nearly 40% at L_{eff}=0.12μm. Fig. 8 shows that for very short devices average electron velocity has a strong dependence on the vertical field, particularly at liquid nitrogen temperature. This is due to the fact that velocity overshoot is weaker when the low-field mobility is lower, and that the vertical field reduces the low-field mobility.

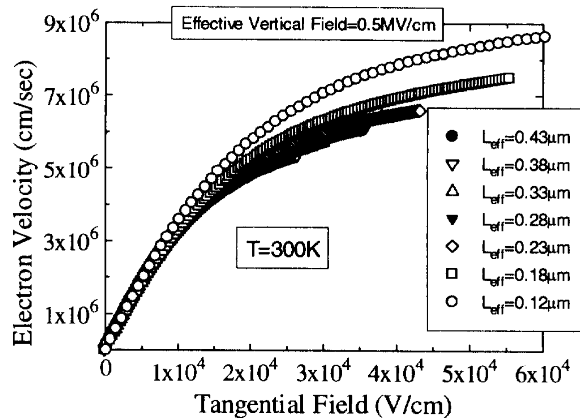

Fig. 6 The electron velocity as a function of applied tangential field, for several different test structure lengths. The samples used in the measurement are not nitrided. T=300K.

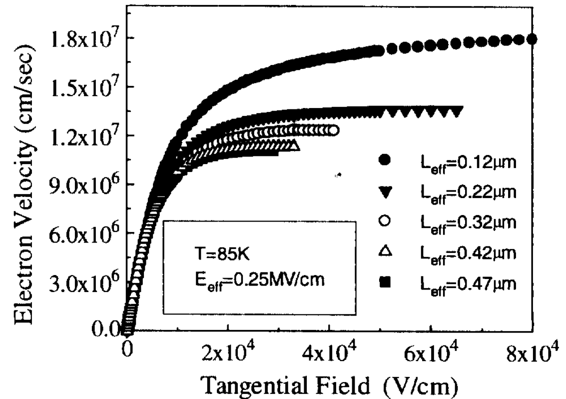

Fig. 7 The electron velocity as a function of applied tangential field at T=85K. Test structure length is used as a parameter. Samples are not nitrided.

Fig. 9 illustrates hole velocity as a function of applied tangential field. The test structure length is approximately 0.2μm for all of the samples. The nitrided sample has lower velocity, although the velocity reduction is not as significant as in the case of electrons. Fig. 10 shows the hole velocity as a function of tangential field, for different channel lengths. No velocity overshoot is observed down to 0.14μm channel length.

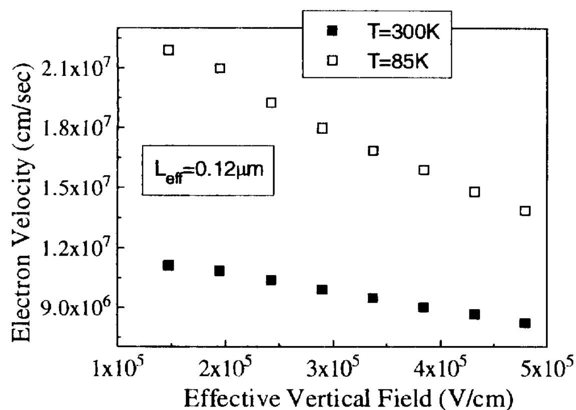

Fig. 8 Vertical field dependence of the average electron velocity at room and liquid nitrogen temperature for a 0.12μm device. The applied tangential field is 80KV/cm.

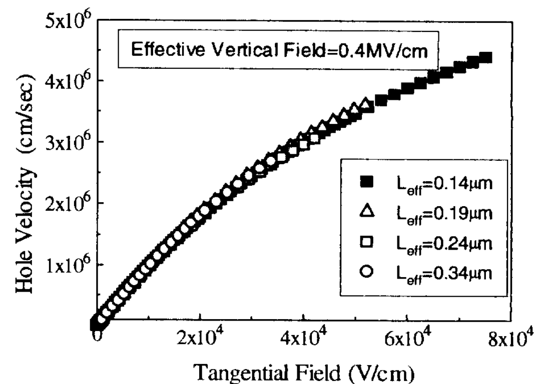

Fig. 10 The hole velocity as a function of applied tangential field at room temperature. Several different test structure lengths are shown. Unpolished SIMOX wafer is used in this measurement.

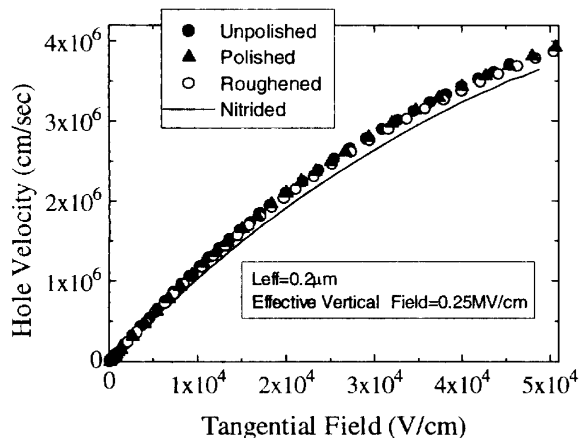

Fig. 9 The hole velocity as a function of applied tangential field. All of the samples are SOI.

Conclusion

To study high-field transport of inversion-layer carriers deep sub-micrometer test structures were fabricated on bulk and SOI wafers varying doping concentration, surface micro-roughness, nitridation of the gate oxide, and carrier type (electrons and holes). Several interesting phenomena were observed including: electron velocity overshoot at room temperature, dependence of electron and hole saturation velocity on nitridation of the gate oxide, and relative insensitivity of electron and hole mobility and saturation velocity to moderate surface roughness.

Acknowledgment

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