High Performance 0.1-µm Room Temperature Si MOSFETs

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ABSTRACT

We report the design and implementation of 0.15 µm channel N-MOSFETs with very high current drive and good short channel behavior at room temperature. Measured subthreshold characteristics show a slope of 84 mV/dec and a shift of 75 mV for $\Delta V_{ds}=1$ V. A peak g_m of 570 mS/mm was recorded, leading to a unity-current-gain cutoff frequency (f_T) of 89 GHz. Key process steps include the formation of 40Å gate oxides and sub-500Å junctions.

INTRODUCTION

One of the key challenges in scaling the Si MOSFET into the deep submicron regime is maintaining good short channel behavior (e.g. I_{off}, ΔV_{th}) without speed penalty for operation at 300K. Initial attempts at deep submicron devices designed for good short channel behavior used high substrate doping, leading to high V_{th}, large junction capacitance, and degraded mobility, with consequent speed degradation [1]. Conversely, high speed operation for 0.1µm devices has been reported [2], but adequate subthreshold behaviour was only obtained at 77K. Low-impurity-channel transistor structures alleviate problems associated with high threshold voltage and degraded mobility, but the junction capacitances remain large [3]. Elevated source and drain structures have been proposed to minimize the junction capacitance, but the fabrication procedure exposes the channel area to dry etching, and makes control of junction diffusion difficult [4].

Junction capacitance and channel doping can be simultaneously minimized by locating the doping peak at an intermediate depth t_{Si} between the surface and junction depth [5,6] (Figure 1). In such *vertically engineered* structures, the device is free of short channel effects if the effective channel length (L_{eff}) meets the following scaling rule [6]:

$$L_{eff} \geq \gamma \sqrt{t_{ox}\, t_{Si}}\,, \qquad (1)$$

where t_{ox} is the gate oxide thickness and γ is a constant determined by the required device characteristics. A γ of 10 is normally sufficient for most applications. In this work, shallow junctions, thin gate oxide and a vertically engineered channel profile were used to ensure long channel behavior and steep subthreshold slopes[6,7].

EXPERIMENT AND RESULTS

MOSFETs were fabricated on p-type 10-15 Ω·cm resistivity wafers with e-beam lithography for gate definition and self-aligned $TiSi_2$ silicides to reduce parasitic resistances. The extended shallow junction device structure uses shallow junctions to control the short-channel effects and deep junctions to facilitate source/drain contacts. The vertically engineered channel profile was realized with a 90 keV 1×10^{13} cm^{-2} BF_2^+ implant, followed by a thermally-grown 40 Å gate oxide at 800 °C in dry O_2 for 18 min. Shipley negative e-beam resist SAL-603 was used to define small gate features. These consist of a 2000 Å thick poly-gate, topped by a 1000 Å thick silicon nitride. Large gate features and all other levels were defined by Nikon g-line lithography. The shallow junction was formed by implanting 10 keV 4×10^{14} cm^{-2} As_2^+, and the deep junction was implanted with 20 keV 5×10^{15} cm^{-2} As^+, annealed at 950-1050 °C for 10-20 sec and 800 °C for 80 min., after 2000 Å TEOS sidewall spacer formation. Figure 2 shows SIMS data for a shallow source/drain annealed at 950°C, indicating a junction depth of 300 Å for a substrate doping of 10^{18} cm^{-3}.

Figure 3 shows the subthreshold behavior for a fabricated 0.2 µm channel NMOS device. All measurements are made at room temperature. The turn-on characteristics for L_{eff}=0.15 µm NMOS are shown in Figure 4, indicating a g_m as high as 570 mS/mm. The intrinsic value is even higher due to a ~9 % reduction in g_m by series resistance. Channel length dependences of threshold voltage and transconductance are shown in Figure 5. Capacitance measurements show the doping beneath the junction to be ~4×10^{16} cm^{-3}.

The small-signal frequency response displays a cut-off frequency of 89 GHz for 0.15 µm channel devices (Figure 6). The devices were measured in the common-source configuration with pad parasitics corrected by the Y-parameter subtraction technique [8].

SUMMARY

High performance and good subthreshold deep submicron MOS devices have been designed and fabricated for room temperature operation. Vertical doping engineering was used to minimize doping at the surface and beneath the junctions, while maintaining good turn-off characteristics. Transconductances of 570 mS/mm, subthreshold slopes of 84 mV/dec, and unity-current-gain cut-off frequencies of 89 GHz were obtained for 0.15 µm channel NMOS devices.

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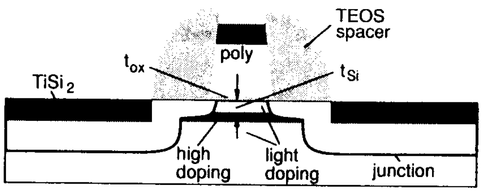

Figure 1 Schematic cross section of the MOS device structure, with *vertically-engineered* doping profile.

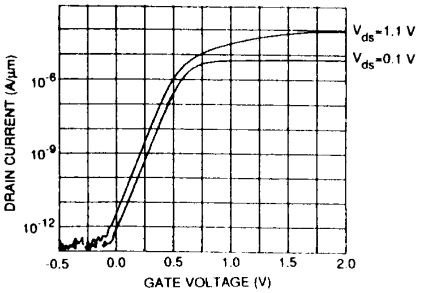

Figure 3 Subthreshold characteristics for 0.2 μm channel NMOS prior to final metalization.

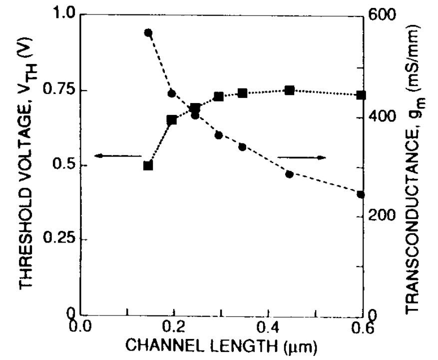

Figure 5 Channel length dependence of threshold voltage and transconductance for NMOS devices.

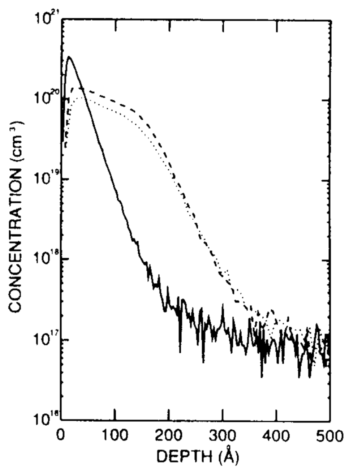

Figure 2 SIMS profile of the arsenic shallow junction. The solid curve is for as-implanted, the dashed for a 10 sec annealing at 950 °C, and the dotted for an additional 2 hr annealing at 800 °C.

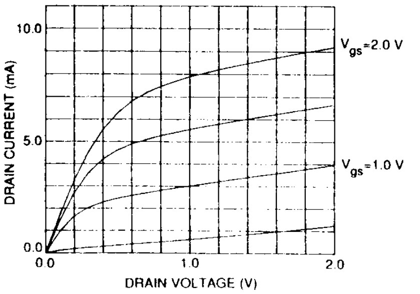

Figure 4 Linear I-V characteristics for 0.15 μm channel NMOS. The effective device width is 9.5 μm.

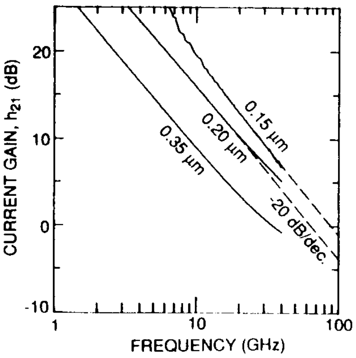

Figure 6 Small signal current gain (h_{21}) as a function of frequency for L_{eff}=0.15, 0.2, and 0.35 μm channel NMOS devices.