Ultrashallow Junctions for ULSI Using As_2^+ Implantation and Rapid Thermal Anneal

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***Abstract*—Using As_2^+ ion implantation and rapid thermal anneal, 40-nm n^+-p junctions are realized. The junction formed with p^- substrate shows very low leakage current (< 0.5 nA/cm^2) up to 2-V reverse bias. The introduction of a heavily doped (10^{18} cm^{-3} level) p region generates a significantly higher leakage current due to the onset of band-to-band tunneling. Using varied geometry devices with a given area, the major tunneling current is shown to be confined in the perimeter of the device, and a method to suppress this leakage is suggested.**

I. Introduction

As lateral MOSFET design rules shrink, vertical dimensions must also shrink; otherwise, short-channel effects degrade the subthreshold characteristics and the threshold voltage stability against the gate-length variation. General scaling rules [1]–[3] prescribe shallow source/drain (S/D) junctions and high channel doping as an antidote to the short-channel effect. When the gate length enters the 0.1-μm regime [4], [5], the required junction depth becomes a few tens of nanometers while the required channel doping reaches low 10^{18}cm^{-3} level for room-temperature operation. The junction depth is controlled by the implantation energy and subsequent diffusion steps. A lower limit on implantation energy is imposed by reduced beam current, and the lower limit on the diffusion temperature is set by the necessity to anneal implantation damage, activate dopants, and avoid transient diffusion [6]. Junctions of 50-nm Sb and 80-nm As have been shown in moderately doped substrates [7], [8]. The requirement of heavy channel doping raises a serious concern about the drain junction leakage, since band-to-band tunneling is known to dominate at these doping levels [9].

In this letter, we describe a method of ultrashallow n^+-p junction formation using As_2^+ ion implantation. The electrical characteristics of such junctions in conjunction with various doses of B^+ implantation are systematically studied.

II. Experimental

The fabrication of diode test structures was initiated with the definition of isolation patterns by a polybuffered LOCOS process on 10-cm-diameter (100) p-type Si wafers with 6 ~ 8-$\Omega \cdot$cm resistivity. After the active area was defined, a 4-nm screen oxide was thermally grown at 800°C. As_2^+ ion implantations were performed at 10 keV with 4×10^{14} cm^{-2} dose. B^+ ions were implanted at 10 keV with doses of 0 cm^{-2} (Type A), 1×10^{13} cm^{-2} (Type B), 2×10^{13} cm^{-2} (Type C), and 3×10^{13} cm^{-2} (Type D). The boron dose emulates various possible channel implantations of the MOSFET devices in 0.1-μm gate-length regime [3]–[5]. In order to activate the dopants and suppress transient diffusion, the wafers were annealed at 1030°C for 10 s in an AG Associate's Heatpulse 2101 rapid thermal processing system. The junctions were then protected by a 300-nm TEOS layer and only a small portion of the active area was open as a contact window. To separate the leakage of the shallow junctions from the contact leakage, a relatively deep junction was formed in the window area. Some wafers of a given type incorporated a deep junction using $CoSi_2$ combined with As^+ implantation/outdiffusion (total junction depth of ~ 150 nm); the others received simple P^+ implantation (30 keV, 2×10^{15} cm^{-2}, junction depth of ~ 500 nm). The deep junction was annealed at 800°C for 120 min. Metallization was done with TiW (50 nm)/Al (500 nm) layers. All of the results reported here were found to be independent of the choice of deep junction.

The dopant profiles were measured by secondary ion mass spectrometry (SIMS) with a 3-keV Cs^+ primary beam on a Phi 6300 spectrometer. The concentration and the sputtering rate were calibrated with standard samples and a depth profilometer. The electrical characteristics were measured in the dark with a Hewlett-Packard 4142 system.

III. Results and Discussions

Fig. 1(a) shows the SIMS profiles of the dopants after the complete diode fabrication. The junction depths are about 40 nm for Type B, C, and D wafers. Due to the sensitivity limit (~ 1×10^{17} cm^{-3}) of the As signal, the junction depth for Type A wafers cannot be directly read out from the data, but, if we extrapolate from the slope in the higher concentration region, we can estimate it to be about 60 nm. In Fig. 1(b), the As profile measured at various process steps is compared with simulations using standard diffusion coefficients [10]. The normal diffusion behavior during the furnace anneal step (800°C, 120 min) demonstrates the effectiveness of the RTA treatment for the suppression of transient diffusion. The As dose mea-

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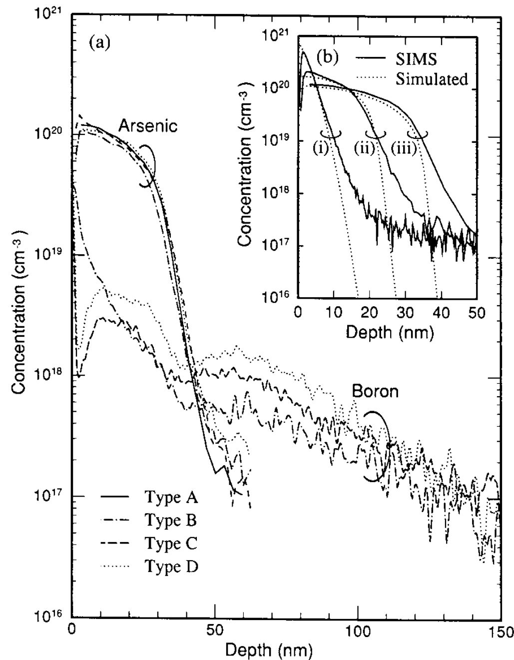

Fig. 1. (a) SIMS profiles of dopants after the complete diode fabrication, and (b) the evolution of As profiles through major thermal steps ((i) as implanted, (ii) after 1030°C 10-s anneal, and (iii) after the completion of fabrication).

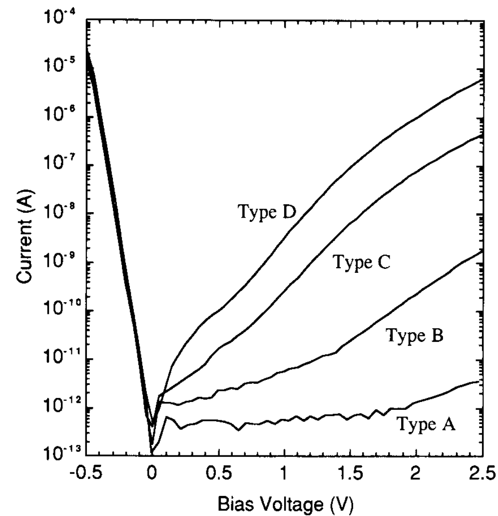

Fig. 2. I–V characteristics of $500 \times 500\text{-}\mu m^2$ diodes.

sured from the SIMS profile is about 2×10^{14} cm^{-2}, which is only 25% of the implanted dose. Some part of this loss ($\sim$ 30% of the implanted dose) can be attributed to the ions which ended up in the screen oxide, and the rest is probably due to segregation at the oxide–silicon interface [11]. The sheet resistance of the n^+ layer measured on Van der Pauw structures was about 470 $\Omega/\square$ for all types of wafers. Assuming an effective mobility of 70 $cm^2/V \cdot s$, we can estimate that about 95% of the As profile measured by SIMS is activated.

Fig. 2 shows the I–V characteristics of $500 \times 500\text{-}\mu m^2$ diodes. The ideality factor obtained from forward I–V characteristics is about 1.04. In the reverse-bias region, Type A wafers maintain very low leakage (< 0.5 nA/cm^2) up to 2 V, indicating the absence of the residual damage in the depletion region. The incorporation of high-concentration boron introduces a strongly voltage-dependent leakage component in the reverse I–V characteristics of Type B, C, and D wafers. The strong voltage and doping dependence suggests that the leakage mechanism is tunneling.[1] Measuring the temperature dependence of the leakage current, we have confirmed that it is indeed tunneling current. However, simulations with one-dimensional tunneling models [12] predict a few orders of magnitude less leakage than observed for the profiles of Type B and C wafers, while resulting in a better fit for Type D. One possible source of the extra leakage current is the perimeter of the device, since the perimeter often bears a significantly higher electric field strength.

In order to investigate the issue of area versus perimeter tunneling, we have plotted the current through junctions with various perimeters and areas in Fig. 3. For Type B and C wafers, the current is almost exactly proportional to the perimeter length regardless of area, which establishes that the perimeter component dominates the leakage. Type D wafers show dependence on both perimeter and area, revealing that the two components are comparable. Evidently, the doping underneath the whole area is now high enough to generate considerable tunneling leakage.

The possible causes of large perimeter tunneling are: 1) the junction curvature effect, 2) the higher lateral p doping due to a two-dimensional implantation effect and channel stop implantation (with peak concentration of 2×10^{17} cm^{-3}), and 3) the stress-induced bandgap narrowing [13] around the bird's beak. We have calculated the combined effect of 1) and 2) by using 2D process (PROPHET [14]) and device (PADRE [15]) simulators, and found that such a 2D effect alone does not account for the total perimeter leakage. To check the effect of 3), we have performed an oxide strip experiment, measuring the I–V characteristics at various oxide thicknesses. Even though the leakage current at low voltage (< 1.5 V) increased due to surface unpassivation, the tunneling current at higher bias showed more than an order of magnitude reduction in Type B and C wafers (about factor of 2 reduction in Type D) after oxide removal. This result suggests that, if we avoid placing the shallow junction at the isolation edge, the tunneling current can be significantly reduced (except for Type D, where the areal com-

[1] The rapid increase in leakage current at > 2-V reverse bias for Type A wafers is also attributable to tunneling. Even though no channel boron implantation is done for this type, the channel stop implant in the field produces a boron concentration of $\sim 2 \times 10^{17}$ cm^{-3} around the perimeter.

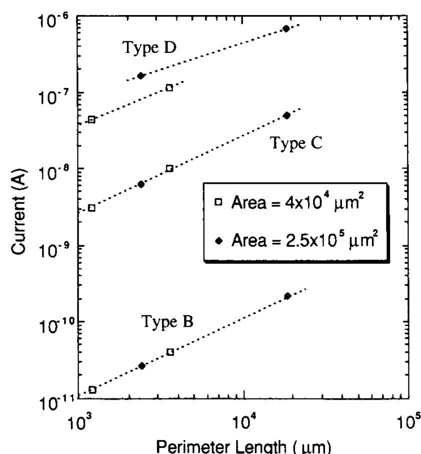

Fig. 3. Leakage current at 1.5-V reverse bias versus perimeter length.

ponent is not negligible). This is usually the case in practical devices, where the shallow junction is an extension to a deeper contact junction [5].

IV. Conclusion

We have developed a 40-nm n^+-p shallow junction process that can be readily integrated into MOSFET devices with a gate length of 0.1 μm. Extremely shallow As profiles were achieved using As_2^+ instead of As^+ ions, and the robustness of these profiles throughout the subsequent thermal steps was demonstrated. Two main leakage components were identified: tunneling due to the relatively heavy p doping for good RT short channel behavior, and a perimeter component due to the oxidation-induced stress effects.

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