89-GHz f_T Room-Temperature Silicon MOSFET's

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Abstract—**We report the implementation of deep-submicrometer Si MOSFET's that at room temperature have a unity-current-gain cutoff frequency (f_T) of 89 GHz, for a drain-to-source bias of 1.5 V, a gate-to-source bias of 1 V, a gate oxide thickness of 40 Å, and a channel length of 0.15 μm. The fabrication procedure is mostly conventional, except for the e-beam defined gates. The speed performance is achieved through an intrinsic transit time of only 1.8 ps across the active device region.**

MINIATURIZATION improves the speed of devices and the packing density of integrated circuits. For Si MOSFET's, scaling the channel length into the deep-submicrometer regime leads to better performance, for example, higher cutoff frequency f_T, due to reduced carrier transit time across shorter device active regions [1]. Previously, a standard 0.5-μm process has demonstrated f_T of 19 GHz [2], while a 0.35-μm silicon-on-sapphire (SOS) process has produced f_T of 23 GHz [3]. Although MOSFET's with 0.1-μm channel lengths have been fabricated [4]–[6] with ring-oscillator delays of 17.7 ps at room temperature [7], no f_T data with these dimensions appear to have been reported. In this paper, we report the highest f_T transistors realized in Si technology to date: 89-GHz f_t for a 0.15-μm channel length MOSFET. With very different device structures, bipolar transistors have previously achieved 64-GHz f_T with polysilicon emitters [8] and 75-GHz f_T with $Si_{1-x}Ge_x$ bases [9].

MOSFET's were fabricated on p-type 10–15-$\Omega \cdot$ cm resistivity wafers with e-beam lithography for gate definition and self-aligned $TiSi_2$ silicides to reduce parasitic resistances. The extended shallow junction device structure uses shallow junctions to control the short-channel effects and deep junctions to facilitate source/drain contacts. The channel was implanted with 90-keV $1 \times 10^{13}/cm^2$ BF_2^+, followed by a thermally grown gate oxide at 800°C in dry O_2 for 18 min. The gate oxide thickness was measured by ellipsometer to be 40 Å, with a leakage current density of less than 10 nA/cm^2. The thickness determined by ellipsometer correlates quite well with electrical measurements. Shipley negative e-beam resist SAL-603 was used to define small gate features. These consist of a 2000-Å-thick poly-gate, topped by a 1000-Å-thick silicon nitride. Large gate features and all other levels were defined by Nikon g-line lithography. The shallow junction (~ 500 Å deep) was formed by implanting 10-keV $4 \times 10^{14}/cm^2$ As_2^+, and the deep junction was implanted with 20-keV $5 \times 10^{15}/cm^2$ As^+, annealed at 1050°C for 20 s and 800°C for 80 min, after 2000-Å TEOS sidewall spacer formation. A 400-Å layer of Ti was deposited and annealed at 600°C for 60 s in nitrogen. Titanium nitride was then removed, followed by additional annealing at 900°C for 20 s. The sheet resistance of silicides on gate and source/drain is measured to be ~ 3–4 Ω/□ on large patterns.

Fig. 1 shows the dc characteristics of a 0.15-μm channel length (L_{eff}) device. All results reported here were measured at room temperature. The effective device width in Fig. 1 is about 9.5 μm, determined by comparing the current levels with a nominally 50-μm-wide device. The obtained small-signal transconductance g_m is 570 mS/mm, with a threshold voltage of 0.45 V. These data are comparable to previously reported room-temperature results [5]. The output conductance g_D, calculated from Fig. 1 at $V_{gs} = 1.5$ V, is 114 mS/mm, leading to a device voltage gain g_m/g_D of ~ 5.

The channel length L_{eff} is electrically determined by measuring the linear region channel resistance (R_{on}) for devices with coded gate lengths (L_{coded}) varying from 0.05 to 0.4 μm [10]. Fig. 2 shows the measured channel resistance as a function of coded gate length with gate to source biased at 0.3 and 0.4 V above the threshold voltage. The drain-to-source bias is 50 mV. Linear fits are obtained, with the shortest (0.05 μm) coded gate lengths excluded. The intersect point of the two fitted lines yields $\Delta L = L_{eff} - L_{coded} = 0.10$ μm and a series resistance of 24 Ω. The device in Fig. 1 has $L_{coded} = 0.05$ μm and $L_{eff} = 0.15$ μm. This series resistance would degrade the transconductance from the intrinsic value by ~ 7%, for the 0.15-μm channel length device. Due to level-to-level registration requirements, the beam current and

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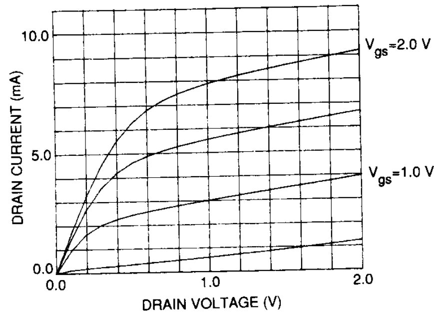

Fig. 1. Room-temperature $I-V$ characteristics of a 0.15-μm channel length (L_{eff}) MOSFET with a 9.5-μm width (W_{eff}). The gate voltage varies from 0 to 2 V, in 0.5-V steps.

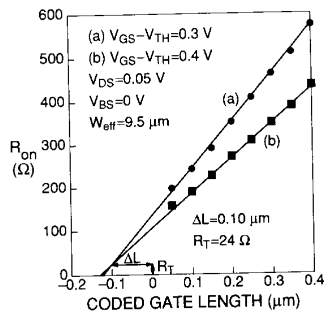

Fig. 2. Measured channel resistance versus coded gate length. The intersection of the two linear fits determines the series resistance and the difference between the effective channel length and the coded gate length.

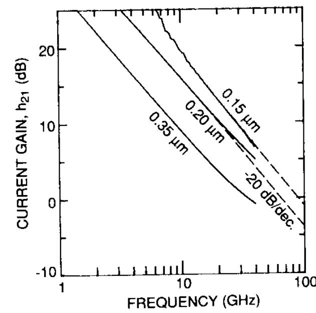

Fig. 3. Current gain h_{21} versus frequency, showing cutoff frequencies of 89, 64, and 34 GHz for devices with channel lengths of 0.15, 0.20, and 0.35 μm, respectively (V_{ds} = 1.5 V, V_{gs} = 1 V). The device width is 40 μm.

therefore the beam size for the e-beam lithography were increased, producing larger gate dimensions than the designs. The cross section of a separate wafer going through the same gate definition steps revealed that the 0.05-μm coded gate length device has a poly-gate dimension of 0.18 μm. The shallow junction extends approximately 200–250 Å under the gate, with ~ 100-Å protective thermal oxide on each side of the poly-gate taken into account. The electrically determined channel lengths agree well with the mechanical cross section and shallow junction data. Details of the shallow junction formation experiments will be reported separately.

The frequency response of these transistors was measured in the common-source configuration using a Hewlett-Packard vector network analyzer with Cascade Microtech 2.4-mm ground–signal–ground coplanar waveguide probes. The pad parasitics were corrected by the Y-parameter subtraction technique [9], [11]. Calibrated using Impedance Standard Substrates, the devices with two 20-μm-wide "fingers" were first measured. Open structures with only metal pads and interconnections were also measured with the same calibration method. The S parameters were then converted to Y parameters, and the intrinsic device characteristics calculated in the Y domain, by subtracting the open structure's Y parameters from those of the device [11]. Fig. 3 shows the corrected magnitude of current gain h_{21} versus frequency for MOSFET's with channel lengths of 0.15, 0.20, and 0.35 μm, which display f_T of 89 (extrapolated), 64 (extrapolated), and 34 GHz respectively, at the nominal drain-to-source bias of 1.5 V and the gate-to-source bias of ~ 1 V.

The effects of parasitics correction are shown in Fig. 4. Without pad extraction, the f_T peaks for the 0.20-μm channel length device because of its relatively large device input capacitance and high intrinsic f_T. For accurate parasitics extraction, the pad capacitance (~ 40 fF) was designed to be comparable to or smaller than the device input capacitance (~ 50 fF for 0.15-μm devices). The noise in the 0.15-μm channel length device data may be due to its small input capacitance, compared to the other two devices with different channel lengths. However, the current gain still shows a −20-dB/decade slope, which was used to determine the cutoff frequency. The average electron velocity in the channel, calculated simply from $v = L_{\text{eff}} \cdot 2\pi f_T$, is about 7.5, 8.1, and 8.4 × 10^6 cm/s, for the 0.35-, 0.20-, and 0.15-μm channel length devices, respectively. These values agree with previously reported room-temperature measurements [12], although they are still less than the saturation velocity of 10^7 cm/s in bulk Si.

Although high-speed advantages can be realized by reducing the device dimension as we have shown above, one of the key requirements for deep-submicrometer devices operating at room temperature is low standby power consumption, i.e., good subthreshold behavior [13], [14]. Our device structure, designed specifically to meet these requirements, displays subthreshold slopes of 84/88 mV/decade for NMOS/PMOS at room temperature (details will be reported separately). These devices are fabricated using essentially conventional processing techniques with no need for nontraditional approaches such as epitaxy or silicon-on-insulator structures, although these nontraditional approaches could improve the performance furthermore. This clearly establishes that conventional processing may be used to fabricate deep submicron devices with good dc and ac characteristics at room temperature.

In summary, we have fabricated deep-submicrometer Si MOSFET's using a combination of e-beam and optical lithography, with conventional processing procedures modified for small dimension devices. The 0.15-μm n-channel device has a unity-current-gain cutoff frequency of 89 GHz. Such high-speed performance is achieved through the short transit time across the active device region.

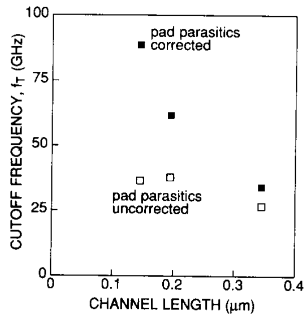

Fig. 4. Effect of extracting pad parasitics. The open squares show the pre-extracted f_T values and the closed squares the extracted f_T values, for three different channel length devices.

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