Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs

Leland Chang, Stephen Tang, Tsu-Jae King, Jeffrey Bokor, and Chenming Hu
Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA
Phone: (510) 643-2637, Fax: (510) 643-2636, E-mail: leland@eecs.berkeley.edu

Abstract

In the nanoscale regime, the double-gate MOSFET can provide superior short-channel behavior. For this structure, device scaling issues are explored. Gate length scaling will be limited by the ability to control off-state leakage current due to quantum tunneling and thermionic emission between the source and drain as well as band-to-band tunneling between the body and drain. Lateral S/D doping abruptness requirements for gate length scaling are examined. V_T control will be challenging as a single gate material for both NMOS and PMOS devices cannot provide low yet symmetrical V_T's. CMOS integration will thus require dual gate workfunction tuning, channel doping, or asymmetrical double-gates to adjust V_T. Advantages of using alternative channel materials to facilitate scaling are investigated.

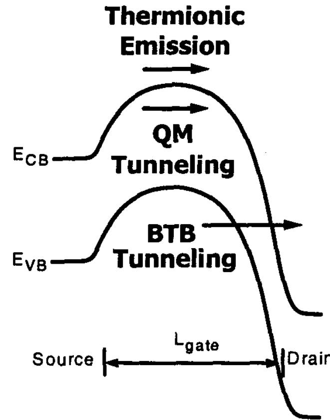

Figure 2: Off-state leakage is comprised of thermionic emission above and quantum mechanical tunneling through the channel potential barrier as well as band-to-band tunneling from the body to the drain.

Introduction

Future transistor scaling will require the incorporation of new device structures [1]. The symmetric double-gate MOSFET (Fig. 1) has been the focus of much attention due to its inherent robustness to short-channel effects [2] and improved current drive capability [3,4]. Short-channel effects can be controlled by using a thin silicon body on the order of $0.7{*}L_{GATE}$ [4]. With light channel doping, statistical dopant fluctuation concerns are eliminated and impurity scattering is minimized. The prospect of double-gate device technologies will depend on the ability to overcome physical and process limitations for gate length scaling and threshold voltage control. In this work, we identify challenges in the design of double-gate MOSFETs and evaluate possible solutions through simulation, including the incorporation of new channel materials.

Gate Length Scaling

Scaling of transistor gate lengths will ultimately be limited by off-state leakage concerns. Because scattering in the channel can be ignored at very small channel lengths, I_{off} will be comprised of thermionic emission above the channel potential barrier, quantum mechanical tunneling between the source and drain, and band-to-band tunneling between the body and drain (Fig. 2). To study I_{off} in double-gate MOSFETs, thermionic emission and band-to-band tunneling leakage components were obtained from a 2-D device simulator [5]. Using 2-D channel potential profiles, quantum mechanical tunneling was estimated by numerical integration.

As T_{body} is reduced, leakage paths far from the gate are eliminated (Fig. 3). Off-state leakage current thus decreases, and short-channel effects are minimized at small gate lengths (Fig. 4). At the limit of T_{body}=5nm (due to series resistance

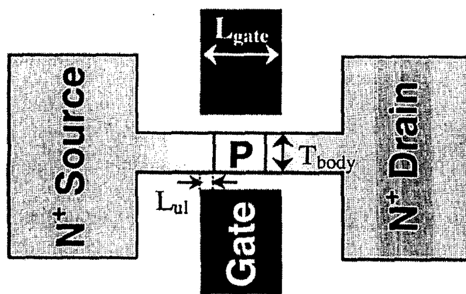

Figure 1: Symmetrical double-gate MOSFET structure. The gate material is assumed to have a tunable workfunction (chosen to achieve the appropriate V_T). $T_{ox,eq}$=10Å. N_A=1e16 cm^{-3}.

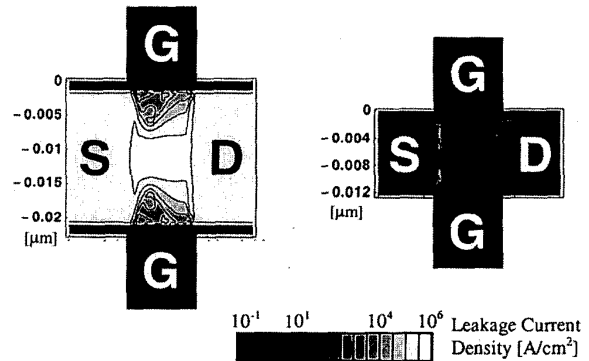

Figure 3: Thinning T_{body} eliminates leakage paths far from the gate, thus improving short-channel effects and allowing for reduced gate lengths. In this example (L_{gate}=25nm, $T_{ox,eq}$=12Å), reducing T_{body} from 20nm to 10nm decreases I_{off} from 19μA/μm to 2.1nA/μm.

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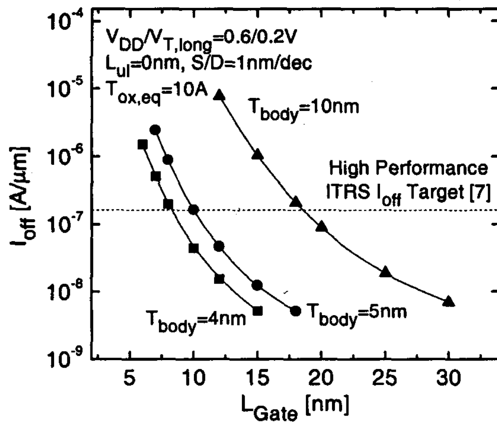


Figure 4: DIBL improves as T_{body} is thinned, thus reducing I_{off}. At T_{body}=5nm, L_{min}~10nm can meet the ITRS [7] I_{off} criteria. Device width is assumed to be twice the gate width to account for the double gate.

[6]) and $T_{ox,eq}$=10Å (due to gate leakage), the ITRS [7] high performance I_{off} specification can be met at L_{gate}~10nm. Lateral abruptness of the source/drain doping profile and underlap of the gate edge can have a profound impact on device scalability (Fig. 5). Because non-abrupt S/D profiles can improve DIBL by depleting into the S/D regions, a smaller physical L_{gate} can be sustained at a constant gate underlap. However, this, along with a thin T_{body}, introduces series resistance at the source and drain which may severely degrade the on-state drive current. Despite this, intrinsic performance (CV/I_{on}) can still be maintained through capacitance reduction from gate length scaling (Fig. 6). As V_T is scaled down to accommodate reduced power supplies, the off-state barrier height in the lateral channel potential profile is lowered, thus exacerbating leakage and increasing the minimum acceptable L_{gate} (Fig. 7). Further reduction of V_{DD} only slightly alleviates this problem.

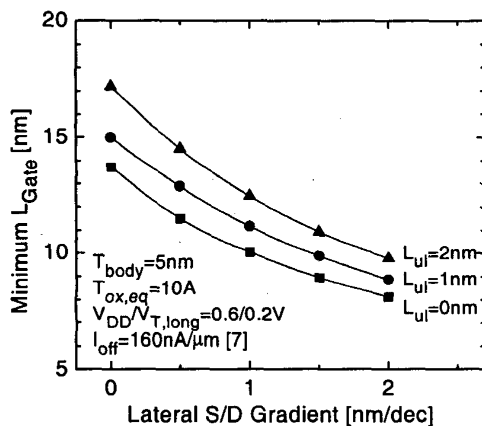


Figure 5: An abrupt S/D doping (S/D gradient = 0) is not critical to scaling in the double-gate structure. Conversely, a non-abrupt S/D improves short-channel effects and allows a smaller L_{Gate} at the cost of series resistance.

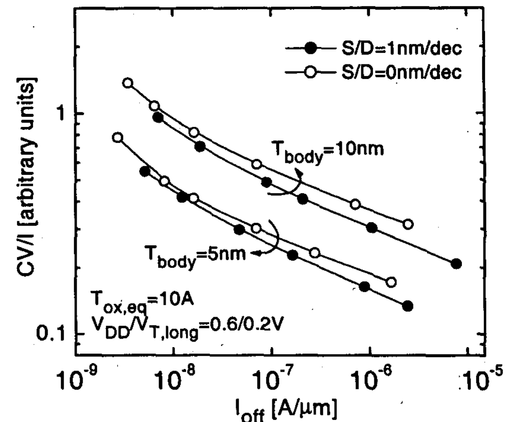


Figure 6: The CV/I performance metric is relatively unaffected by the abruptness of the S/D gradient.

Threshold Voltage Control

Due to scaling of power supply voltages, it is desirable to achieve low (~0.2V) and symmetrical (V_{Tn}= $-V_{Tp}$) threshold voltages for both transistor types. In the double-gate structure, long-channel V_T is primarily controlled by the gate workfunction. With a single midgap material for both NMOS and PMOS, symmetrical V_T's can be achieved, but the value is too large [8]. $V_{Tn}+(-V_{Tp})$ is roughly pinned to $E_{g,Si}$ since V_T is determined by ϕ_M and χ_{Si} (Fig. 8). Because of the V_T definition used (constant current, often lower than linear extrapolation), $V_{Tn}+(-V_{Tp})$~0.8V, allowing for symmetric V_T's only at ~0.4V (Fig. 9). To achieve V_T=0.2V, separate gate workfunctions slightly above and below midgap are needed. This would require dual-metal gate processes [9], tunable metal gate workfunctions (e.g. Mo [10], TiN [11]), or small-bandgap semiconductor gate materials (e.g. CrSi[12]).

Another option is the continued use of N^+ and P^+ polysili-

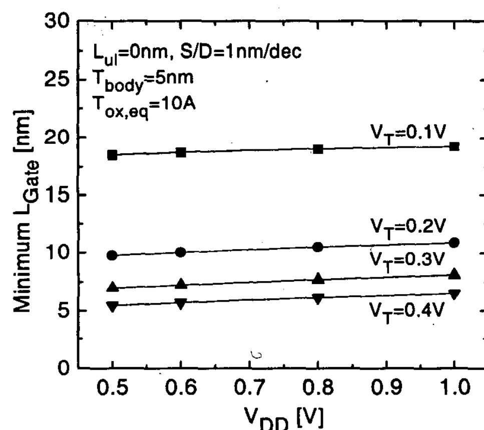
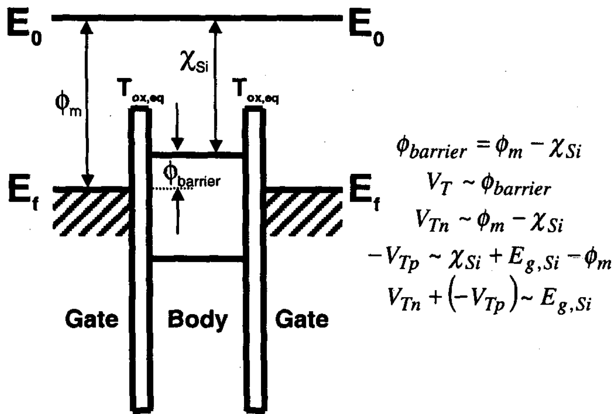


Figure 7: I_{off} will increase as V_T is scaled down because the channel potential barrier height is reduced. Leakage is only somewhat improved at low V_{DD}. Long channel V_T is defined at I_{ds}=100nA/μm when V_{ds}=50mV.



$$\phi_{barrier} = \phi_m - \chi_{Si}$$
$$V_T \sim \phi_{barrier}$$
$$V_{Tn} \sim \phi_m - \chi_{Si}$$
$$-V_{Tp} \sim \chi_{Si} + E_{g,Si} - \phi_m$$
$$V_{Tn} + (-V_{Tp}) \sim E_{g,Si}$$

Figure 8: Flatband condition band diagram for a symmetric double-gate NMOSFET (vertically through Fig. 1). V_T is roughly equal to the potential barrier height between the source (aligned to E_f of the gate at V_{GS}=0) and the channel.

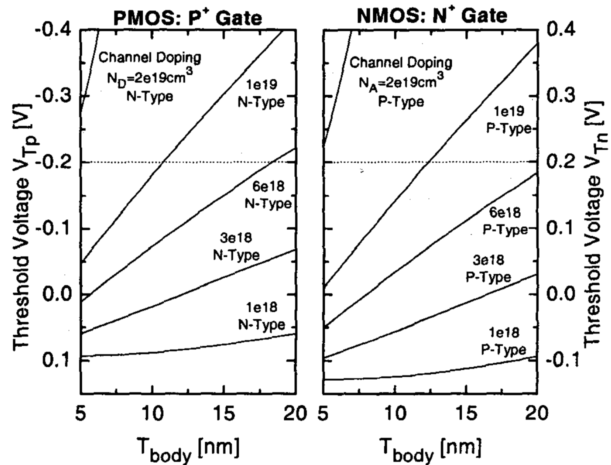


Figure 10: To achieve low and symmetrical V_T's with N^+ and P^+ polysilicon gates for NMOS and PMOS transistors, a large channel doping is needed to raise the threshold voltage. With $T_{ox,eq}$=10Å, >6e18 cm^{-3} is needed. Assuming a 10% variation in T_{body}, V_T control can be kept to within ±30mV.

con gates. With lightly-doped channels, V_{Tn} and $-V_{Tp}$ would both be slightly negative. Channel doping would thus be required (Fig. 10) to raise each threshold voltage by approximately 0.3V. However, as T_{body} and $T_{ox,eq}$ are scaled, large channel dopings (~$10^{19}cm^{-3}$) would be required. This would enhance dopant fluctuation effects, degrade subthreshold swing, reduce carrier mobility, and make V_T sensitive to variations in T_{body}. For a 10% variation in T_{body} throughout the range of interest, a ±30mV shift in V_T is observed. Alternatively, a single midgap gate material may be used for both NMOS and PMOS devices. The opposite type channel doping would then be needed to lower both V_{Tn} and $-V_{Tp}$ [1]. With a single midgap gate, V_T needs only to be lowered by 0.2V, thus requiring a more modest channel doping than if N^+/P^+ polysilicon gates were used (Fig. 11). This would help to minimize the increase in subthreshold swing and reduce mobility degradation. However, V_T would still be sensitive to T_{body} variation and dopant fluctuation effects.

An additional solution may be to use an asymmetric double gate, in which the two gates are of different workfunctions [3]. This is advantageous in that the familiar N^+/P^+ poly gates may be used. Furthermore, neglecting small differences in effective mass and density of states, V_{Tn} and $-V_{Tp}$ are automatically symmetrical. The value of V_T will depend on T_{body} and T_{ox} (Fig. 12) and is essentially determined by the capacitative divider between the N^+ and P^+ gates. For $T_{ox,eq}$=10Å and V_T=0.2V, the required T_{body} is approximately 6nm. As with channel doping, variation in T_{body} or T_{ox} will affect V_T. However, this scheme is less sensitive to T_{body} fluctuations (±15mV shift in V_T for a 10% T_{body} variation).

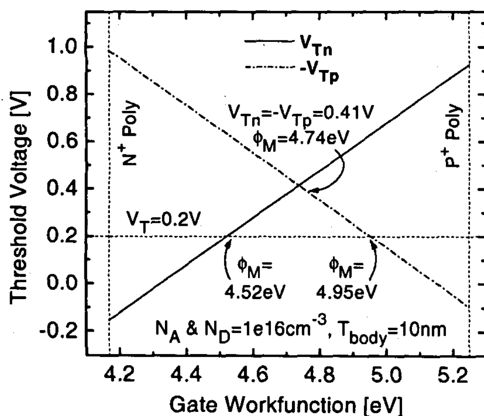


Figure 9: Using a single gate material for both NMOS and PMOS devices can yield symmetric but large V_T's. Achieving low and symmetric V_T's will require two different midgap gate materials.

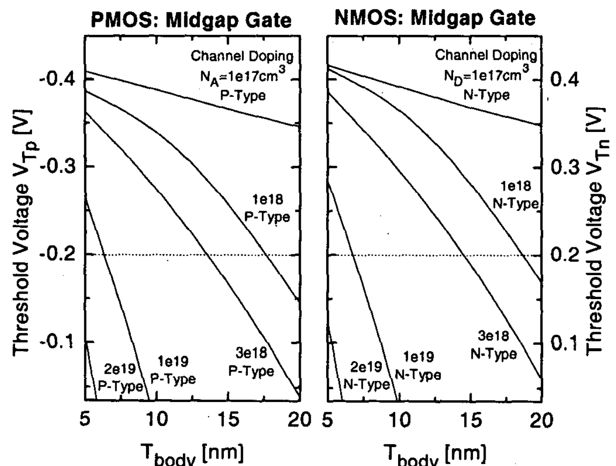


Figure 11: Using a single midgap gate for both transistor types and $T_{ox,eq}$=10Å, slightly lower channel doping levels are needed. For a 10% variation in T_{body}, V_T control can be kept to within ±30mV.

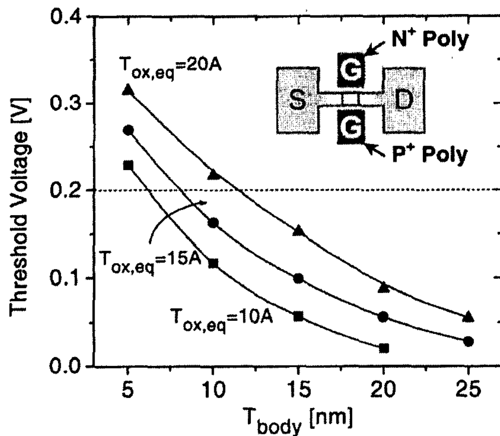


Figure 12: The asymmetric double-gate structure, in which N^+ and P^+ poly gates are used, can yield symmetric V_T's for NMOS and PMOS. The value of V_T depends on T_{body} and $T_{ox,eq}$. Assuming a 10% variation in T_{body}, V_T control can be kept to within ±15mV.

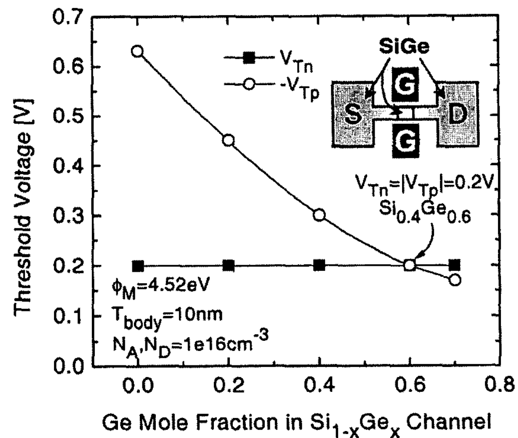


Figure 14: Using $Si_{1-x}Ge_x$ as the channel material will lower $|V_{Tp}|$, while leaving V_{Tn} relatively unaffected. Using a single midgap gate material, this can be used to achieve low V_T's for both transistor types.

Incorporation of New Channel Materials

Further reduction of L_{gate} may be possible by shifting away from silicon to other semiconductor materials. By lowering the dielectric constant of the channel, depletion regions can be reduced, thus alleviating DIBL. A material such as diamond can shrink the minimum L_{gate} to ~7nm (Fig. 13).

New channel materials can also facilitate V_T control. If $Si_{1-x}Ge_x$ is used, the valence band offset between Si and SiGe works to lower $-V_{Tp}$. This offset can be tuned by more than 0.4V by adjusting the Ge mole fraction [13]. V_{Tn} is unaffected since the conduction band offset is small. A single gate workfunction for both transistor types can thus be chosen such that V_{Tn} is the appropriate value. $-V_{Tp}$, which would otherwise be too large, can then be lowered by choosing the Ge mole fraction (0.6 for V_T=0.2V) in the channel (Fig. 14). An added advantage with this technique is that carrier mobility may be improved [14].

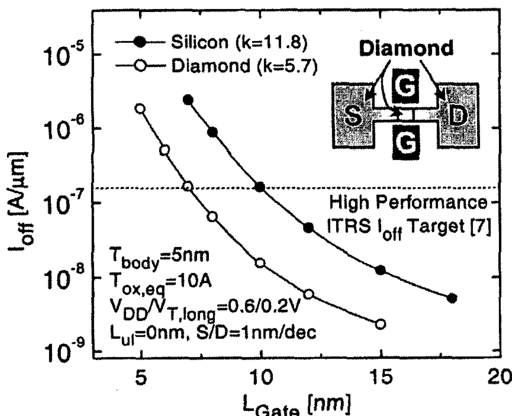


Figure 13: A semiconductor material with a lower *k* (e.g. diamond) reduces DIBL and off-state leakage. This may allow for continued device scaling. Diamond material parameters: *k*=5.7, E_g= 5.4eV, m*=0.2.

Summary

Limitations and challenges in gate length scaling and threshold voltage control of double-gate MOSFETs have been investigated. The minimum L_{gate} that can still meet the ITRS I_{off} criterion becomes smaller as T_{body} is reduced, but is raised by an abrupt S/D doping profile and a low threshold voltage. Achieving desired values of V_T will be a serious challenge for double-gate CMOSFET technology. Dual-metal or N^+/P^+ small-E_g gates require advances in processing and materials technology, whereas channel doping and asymmetric double-gates require accurate control of T_{body}. The use of alternative channel materials can help to facilitate scaling. Low-k materials (e.g. diamond) reduce DIBL and allow for further scaling of L_{gate}. Channel materials with different bandgaps or electron affinities (e.g. SiGe) offer an attractive method of adjusting V_T.

Acknowledgements

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