Transistor Characteristics with Ta$_2$O$_5$ Gate Dielectric

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Abstract—As the gate oxide thickness decreases below 2 nm, the gate leakage current increases dramatically due to direct tunneling current. This large gate leakage current will be an obstacle to reducing gate oxide thickness for the high-speed operation of future devices. A MOS transistor with Ta$_2$O$_5$ gate dielectric is fabricated and characterized as a possible replacement for MOS transistors with ultra-thin gate silicon dioxide. Mobility, $I_d-V_d$, $I_c-V_c$, gate leakage current, and capacitance-voltage (C-V) characteristics of Ta$_2$O$_5$ transistors are evaluated and compared with SiO$_2$ transistors. The gate leakage current is three to five orders smaller for Ta$_2$O$_5$ transistors than SiO$_2$ transistors.

I. INTRODUCTION

As the channel length of the MOSFET is reduced, the gate dielectric thickness must be reduced proportionately in order to maintain acceptable short-channel effects. Thinning of the gate dielectric results in larger drain current, which in turn leads to increased circuit speed. One limit to the scaling of thin SiO$_2$ (oxide) is the large leakage current due to direct tunneling.

When the voltage across a thin oxide layer is reduced below 3.2 V, the tunneling barrier for electrons changes from triangular to trapezoidal. For a trapezoidal tunneling barrier, the oxide current, known as direct tunneling current, is much larger and less sensitive to the voltage than for a triangular barrier, known as the Fowler–Nordheim tunneling current. Direct tunneling current remains high at even 1 V and is very sensitive to gate oxide thickness [1]. Because logic circuits can tolerate large gate leakage (on the order of 1 A/cm$^2$) [2], the oxide scaling limit for 1 V operation is 2 nm (physical oxide thickness) or slightly less. Dynamic random access memory (DRAM) tolerates less oxide leakage and typically the gate potential is boosted up above $V_{DD}$. Therefore, the oxide scaling limit for DRAM may be 3 nm.

According to the National Technology Roadmap for Semiconductors (1997 edition), gate dielectric scaling below 2 nm is desired from 2006 onward. When the SiO$_2$ thickness is reduced below 2 nm, alternative high-permittivity dielectrics such as Ta$_2$O$_5$ must be considered. Ta$_2$O$_5$ has been studied for application as the capacitor dielectric in gigabit DRAM’s [3]–[6]. Ta$_2$O$_5$ has also been proposed as a MOSFET gate dielectric for high-speed circuits in a simulation study [7]. An aluminum-gate P-channel MOS transistor with Ta$_2$O$_5$ gate dielectric has been reported recently [8]. In this paper, we present the characteristics of Poly-Si over TiN stacked gate n-channel MOS transistors with Ta$_2$O$_5$ gate dielectric equivalent to 1.8 nm SiO$_2$.

II. EXPERIMENT

N-channel MOSFET’s were fabricated on p-type 10–20 Ω-cm Si wafers using LOCOS (LOCal Oxidation-of-Silicon) isolation. After active area patterning and LOCOS processing, the wafers proceeded through the gate-stack formation process. First, nitridation of the silicon surface was performed in a Heatpulse 8108 system with a rapid thermal process (RTP) in NH$_3$ ambient at 800 °C for 30 s. Then, the 6-nm Ta$_2$O$_5$ film was deposited by chemical vapor deposition (CVD) with Ta(OC$_2$H$_5$)$_5$ and O$_2$ at 420 °C, 400 mT by DSM9800 (Lam Research). After Ta$_2$O$_5$ deposition, the samples were annealed at 800 °C for 30 s using RTP in O$_2$ ambient [9]. In situ N$^+$-doped CVD polysilicon over sputter-deposited 60-nm TiN was used for the gate electrode formation. After the polysilicon deposition, the wafers were annealed by RTP. After gate poly patterning, the source and drain regions were formed with an arsenic ion implant of 5 × 10$^{15}$/cm$^2$ at 60 keV followed by a 30-min anneal in N$_2$ at 800 °C.

N-channel MOSFET’s with 3.8 and 2.4 nm SiO$_2$ gate dielectric were also fabricated for comparison with the Ta$_2$O$_5$ transistors. Gate leakage current, capacitance, $I_d-V_d$, and $I_d-V_g$ characteristics, and mobility were characterized and evaluated.

III. RESULTS AND DISCUSSION

As shown in Fig. 1, the equivalent physical SiO$_2$ thicknesses of the SiO$_2$ and Ta$_2$O$_5$ gate dielectrics were determined with the aid of a C–V simulator which accounts for quantum confinement of the inversion layer at the silicon surface and the poly-gate depletion effect [10]. Using this method, it was found that after gate-electrode formation and source/drain-region formation, the 6-nm Ta$_2$O$_5$ was equivalent to 1.8-nm SiO$_2$. We believe that the annealing processes after Ta$_2$O$_5$ deposition caused oxidation at the silicon substrate interface, to form 0.8–1-nm SiO$_2$ layer. So, the 6-nm Ta$_2$O$_5$ with relative permittivity, $\varepsilon_r$, of 25 (generally known value) results in only 1.8 nm of equivalent SiO$_2$ [6], [9]. Using the C–V simulator and measurement data, we could also determine the work function of TiN to be 4.8 eV, which is similar to previously reported values [11]. Without a threshold-voltage adjustment
Fig. 1. C–V characteristics of SiO₂ and 1.8-nm Ta₂O₅ transistors. Lines represent theory including quantum effect in the inversion layer and the gate depletion. The C–V model is a useful tool for extracting the equivalent oxide thickness.

Fig. 2. Gate leakage current of Ta₂O₅ and SiO₂ MOSFET’s. The lower leakage current of the Ta₂O₅ device is a major benefit, especially for memory applications.

implant, the Ta₂O₅ transistor threshold voltage was 0.66 V, due to this large gate work function. The threshold voltage of the comparison SiO₂ transistors with N⁺ polysilicon gate was adjusted to be ~0.4 V by BF₂ ion implantation before the gate SiO₂ growth.

Fig. 2 shows that less tunneling current flows through the Ta₂O₅ than SiO₂ for the same equivalent oxide thickness. Therefore, the large leakage current problem due to the direct tunneling of ultra-thin SiO₂ can be palliated using high permittivity Ta₂O₅ as a gate dielectric material.

Fig. 3 shows the Iₕ–Vₜ and Iₙ–Vₜ characteristics of a Ta₂O₅ transistor with channel width of 100 µm and channel length of 30 µm. Subthreshold swing of this Ta₂O₅ transistor is 87 mV/dec, similar to thin-SiO₂ transistors. Drain current at V₉ = Vₜ = 1.5 V is 0.316 mA.

Fig. 4 shows the mobility data for two SiO₂ and one Ta₂O₅ transistors as a function of effective electric field, compared with an universal mobility model [12]

\[
\mu_{eff} = \frac{500}{1 + (E_{eff}/0.9)^{1.25}} \text{cm}^2/V \cdot s.
\]

The inversion charge was directly measured from the integration of Cₛₜₛₒₙ gate to source/drain capacitance, of the transistors. From this figure, it can be seen that Ta₂O₅ transistor mobility behavior is similar to that of SiO₂ transistors. Regardless of the gate-dielectric material, the MOSFET carrier mobility is well modeled by taking into account the effective electric field, which is larger for equivalently thinner gate-dielectric layers.

IV. CONCLUSION

MOS transistors with Ta₂O₅ gate dielectric were fabricated using well-established techniques such as LOCOS isolation,
TiN/N⁺-polysilicon stacked gate, and self-aligned source/drain formation. The use of a 6-nm-thick Ta₂O₅ film, equivalent to 1.8-nm SiO₂ thickness, suitable for the 100 nm technology, was demonstrated. Ta₂O₅ transistors provide significantly lower gate leakage current than SiO₂ transistors. The mobility behavior in Ta₂O₅ transistors follows that of SiO₂ transistors. Therefore, Ta₂O₅ is a promising alternative gate-dielectric material for future MOSFET technologies. Further work is underway to study short-channel device performance and reliability issues such as hot carrier resistance, process-induced damage immunity, and oxide lifetime.

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REFERENCES