

FinFET and other New Transistor Technologies

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Univ. of California

May 4 2011 NY Times Front Page

NY Times news article:

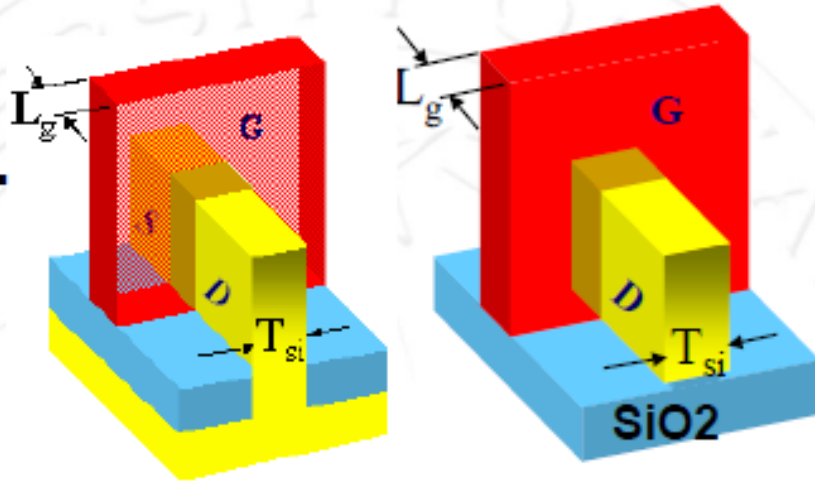
- **Intel will use 3D FinFET for 22nm**
- **Most radical change in decades**
- **There is a competing SOI technology**

Other Background Info

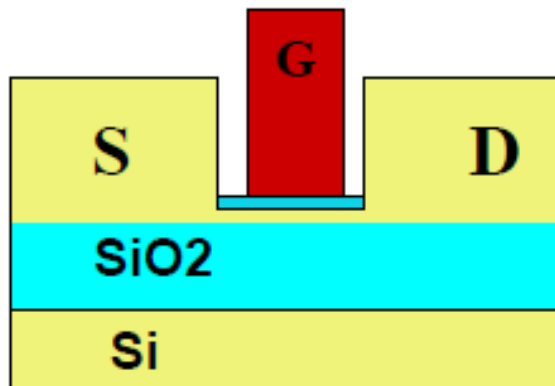
- **TSMC, IBM...new transistors soon**
- **Since 2001 ITRS shows FinFET and ultra-thin-body UTB-SOI as the two successor MOSFETs**
- **SOITEC UTB-SOI recently available**
- **IBM 2009 5nm UTB SOI paper**

New MOSFET Structures

FinFET

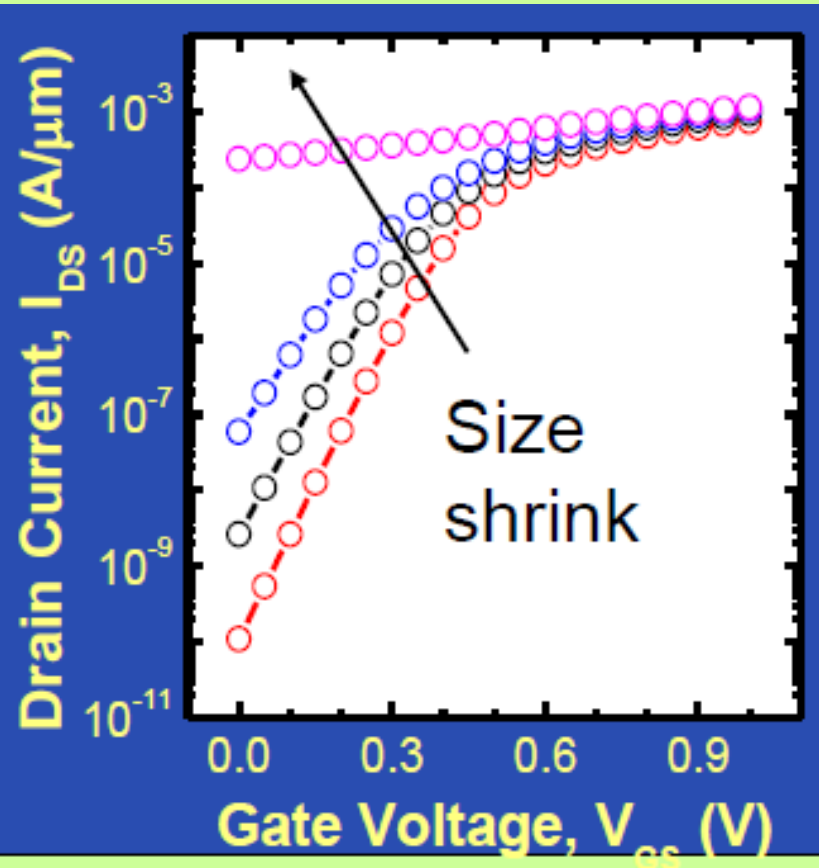


UTBSOI



Ultra Thin Body SOI

Good Old MOSFET Nearing Limits



V_t , S (swing) and I_{off} are sensitive to L_g & dopant variations.

- high design cost
- high V_{dd} , hence high power usage

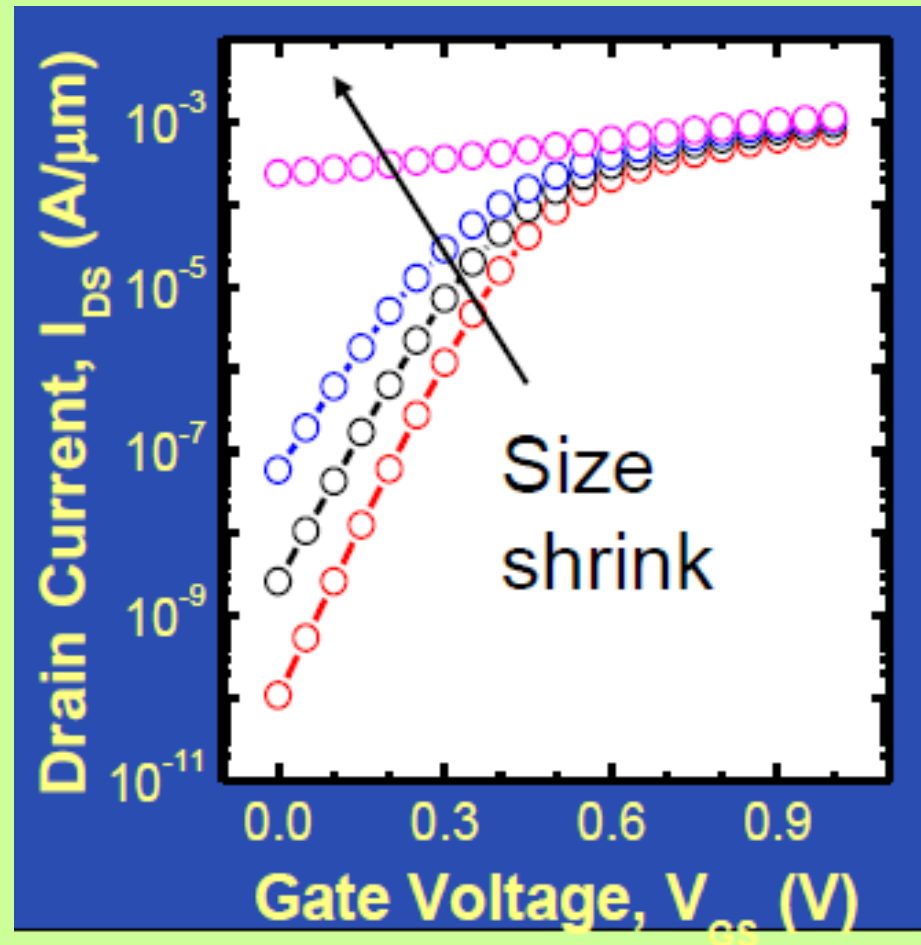
Finally painful enough for change.

Power Consumption Problems

1. Not just a chip and package thermal issue.
2. ICs use a few % of world's electricity today and
 - Power per chip is growing.
 - IC units in use also growing.
3. If power consumption is not reduced, industry future growth is at risk.

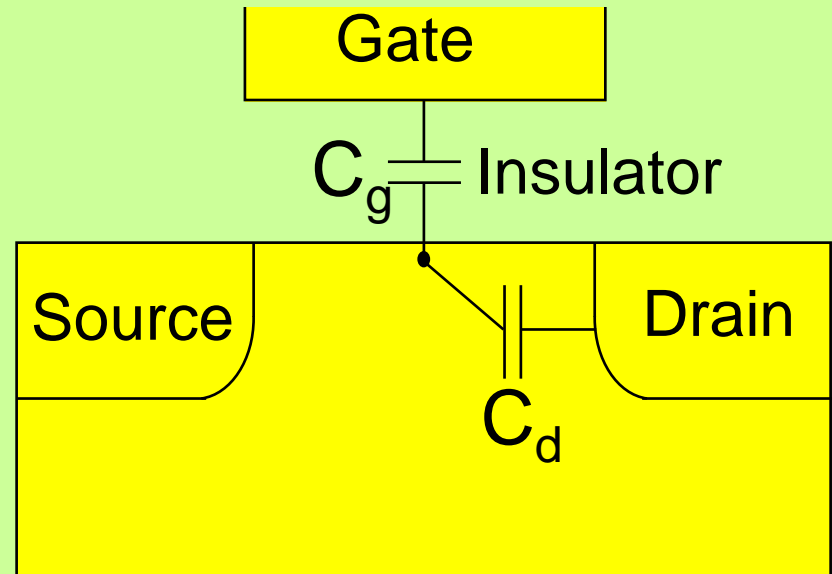
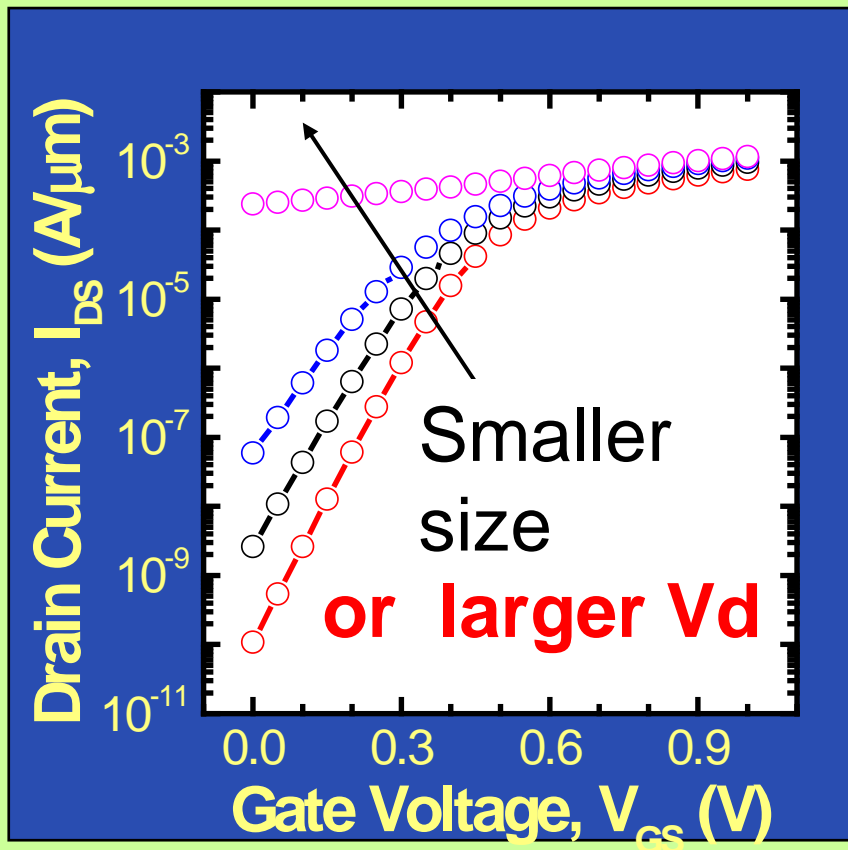
Want Low V_t and Low I_{off}

Need smaller S and less variations of S and V_t

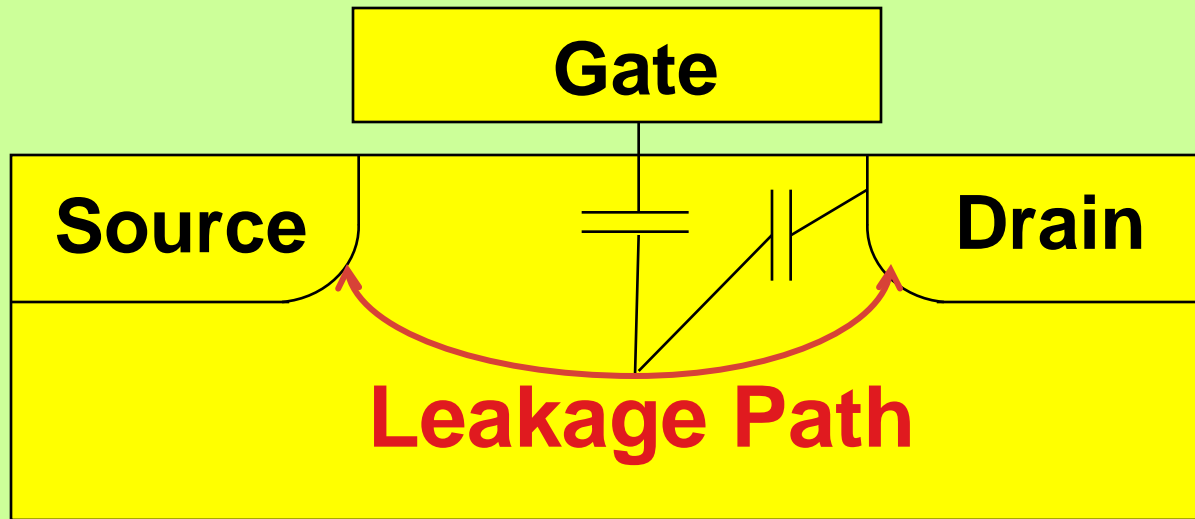


How V_t Variation & S Got So Bad

MOSFET becomes “resistor” at very small L -- Drain competes with Gate to control the channel barrier.



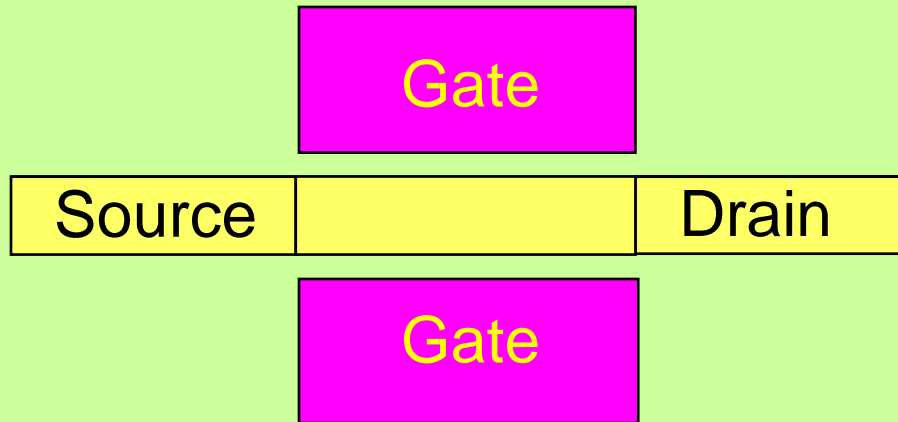
Reducing EOT is Not Enough



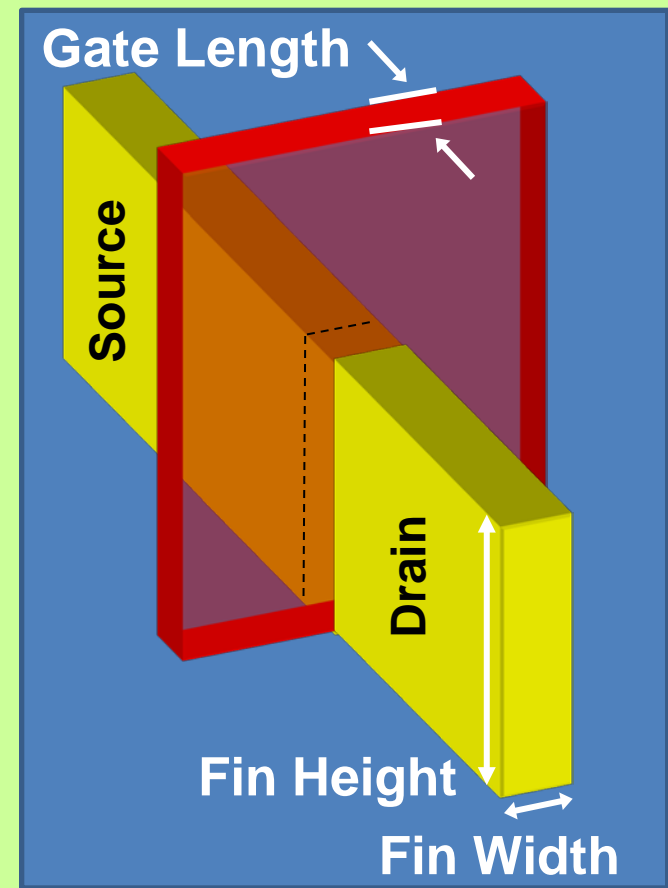
Gate cannot control the leakage current paths that are far from the gate.

One of Two Ways to Better V_t and S

The gate controls a thin body from more than one side.



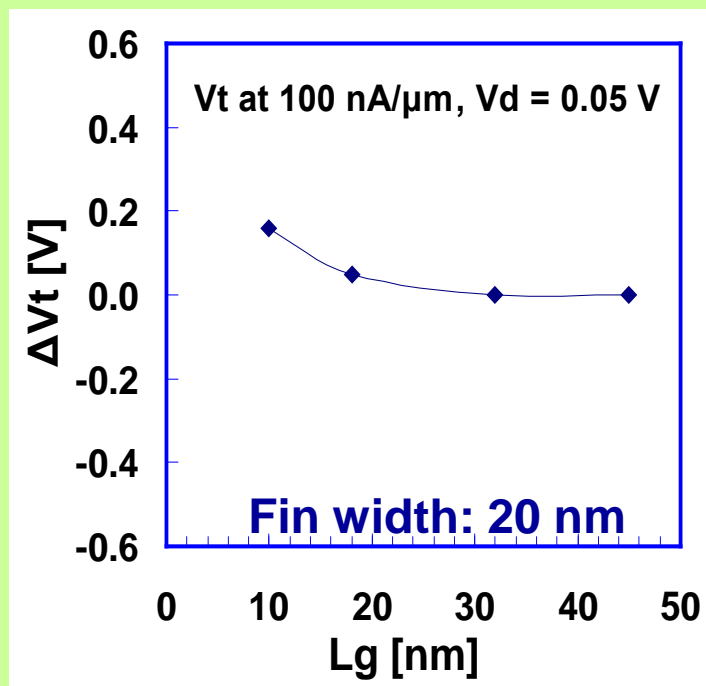
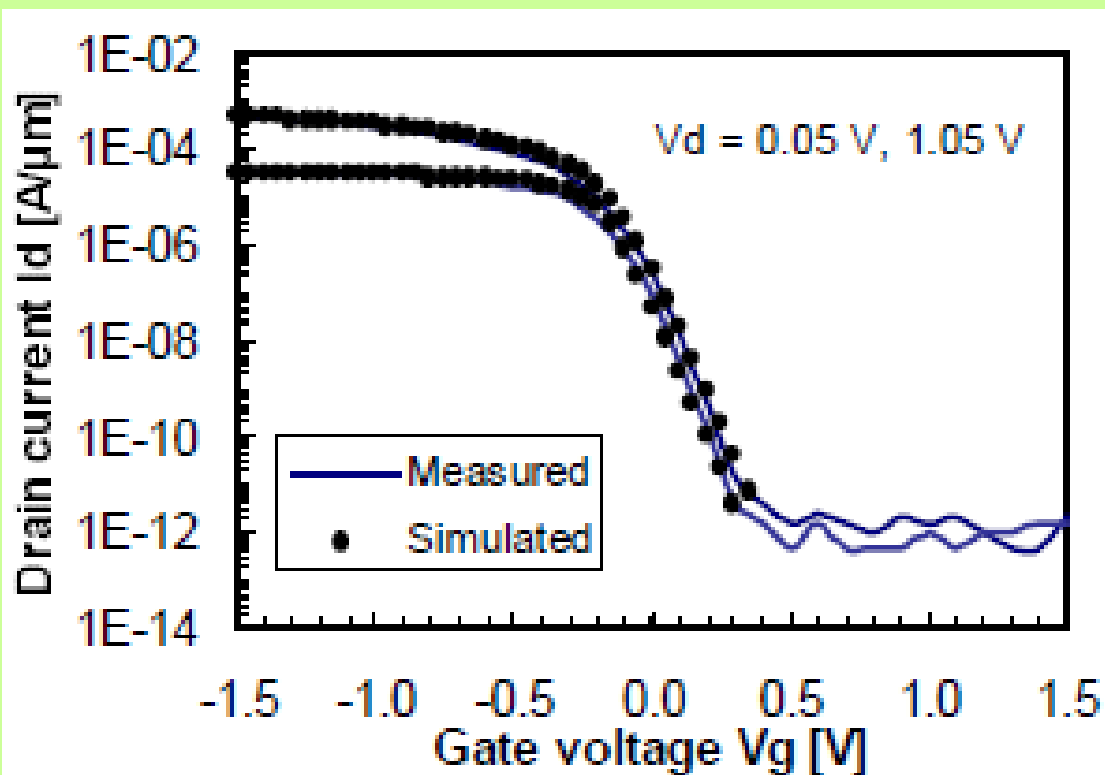
FinFET body is a thin fin



N. Lindert et al., DRC paper II.A.6, 2001

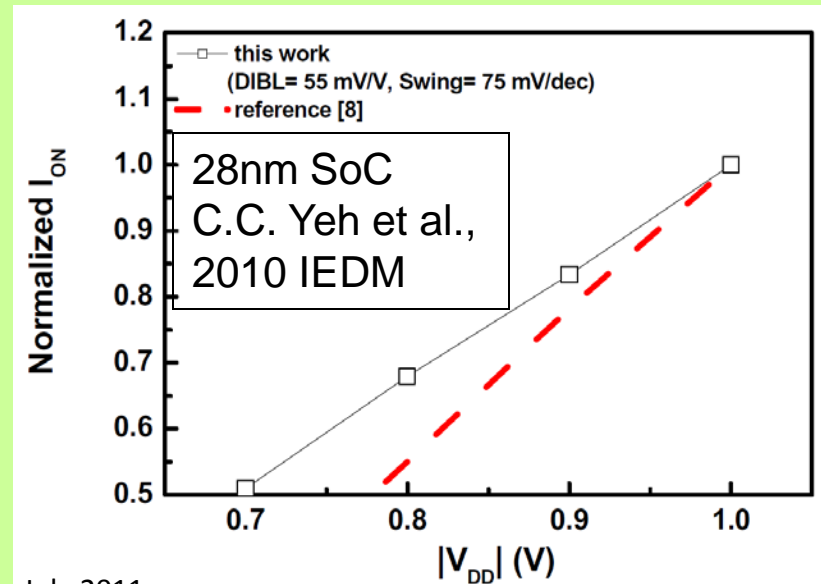
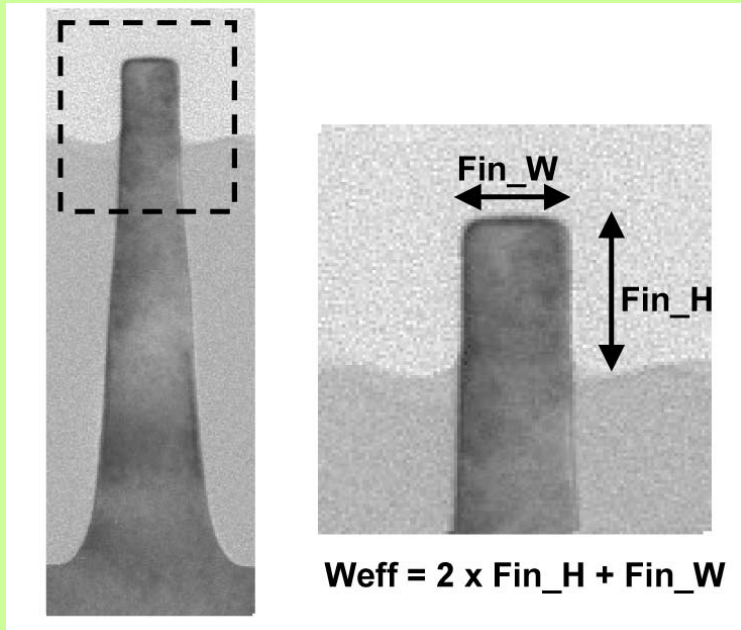
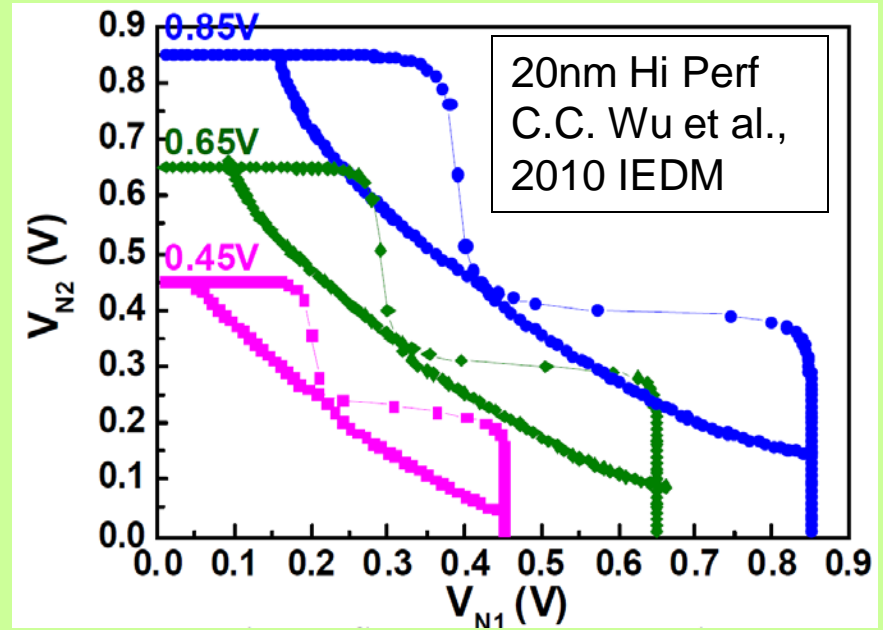
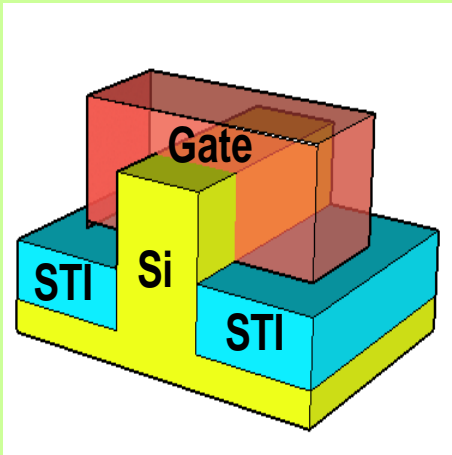
FinFET- 1999

Undoped Body. 30nm etched thin fin.
Vt set with gate work-function (SiGe).



X. Huang et al., IEDM, p. 67, 1999

State-of-the-Art FinFET on Bulk Si

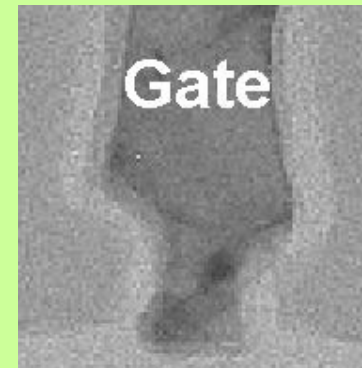
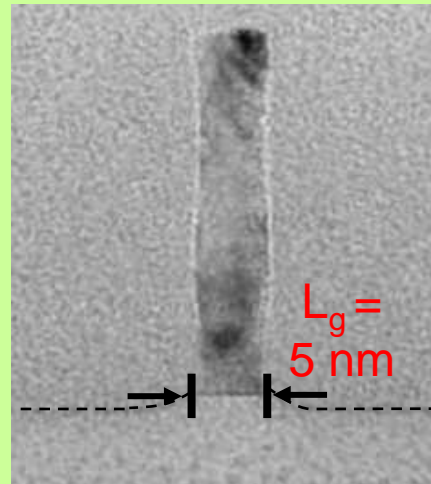
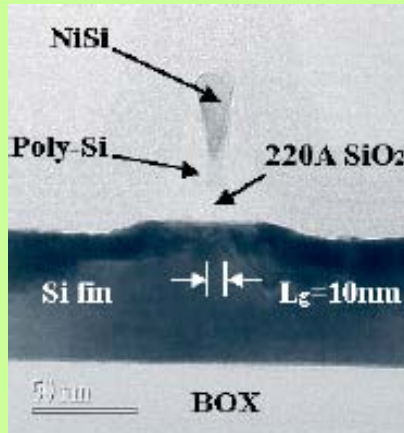


FinFET is “Easy” to Scale

10nm Lg AMD
2002 IEDM

5nm Lg TSMC
2004 VLSI Symp

3nm Lg KAIST
2006 VLSI Symp



because leakage is well suppressed if

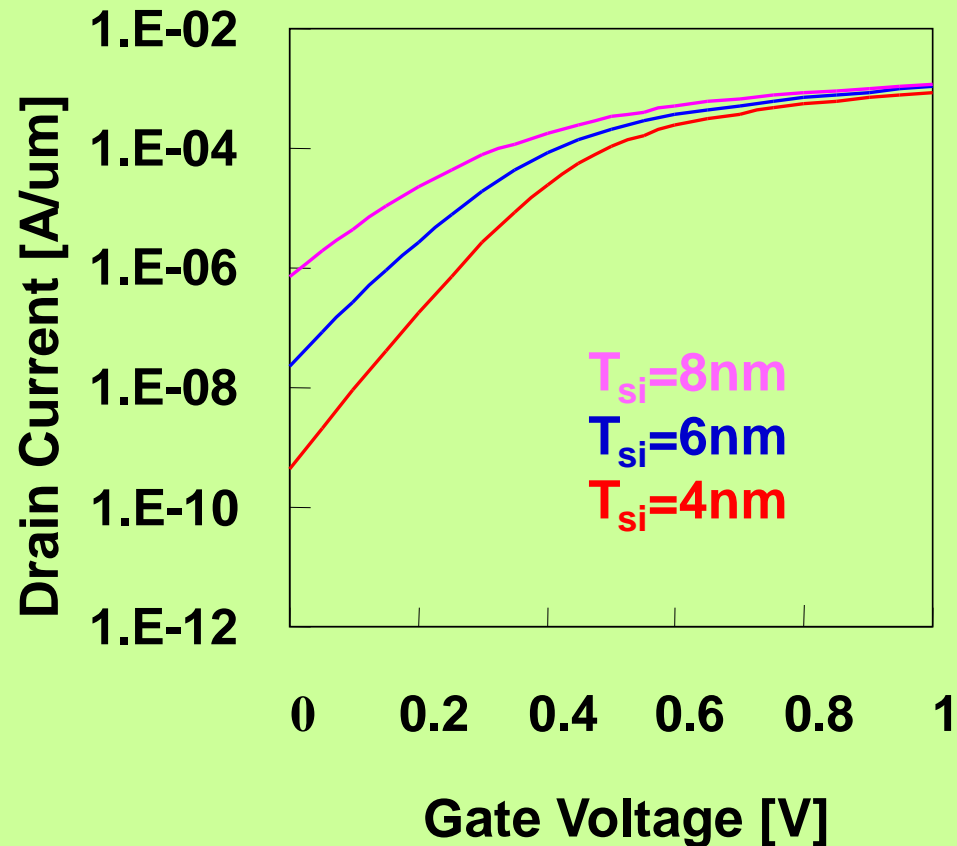
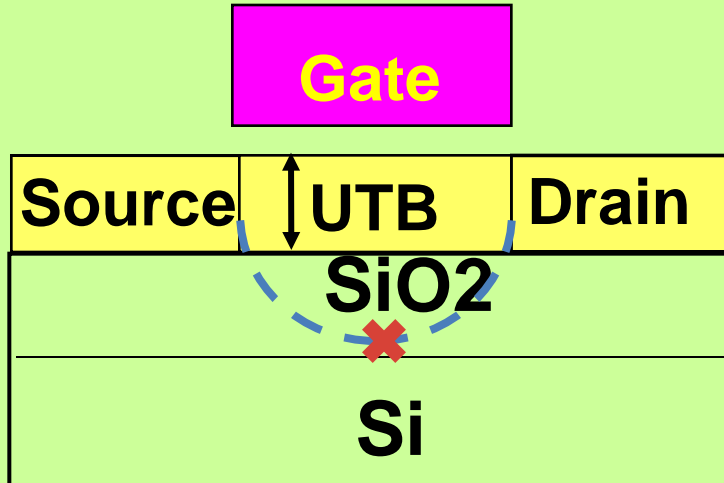
Fin thickness = or < L_g

- Thin fin can be made with the same L_g patterning/etching tools.

Second Way to Better V_t and S

Ultra-thin-body SOI (UTB-SOI) →

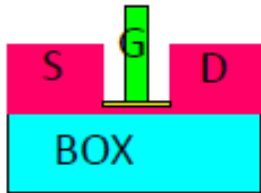
No leakage path far from the gate.



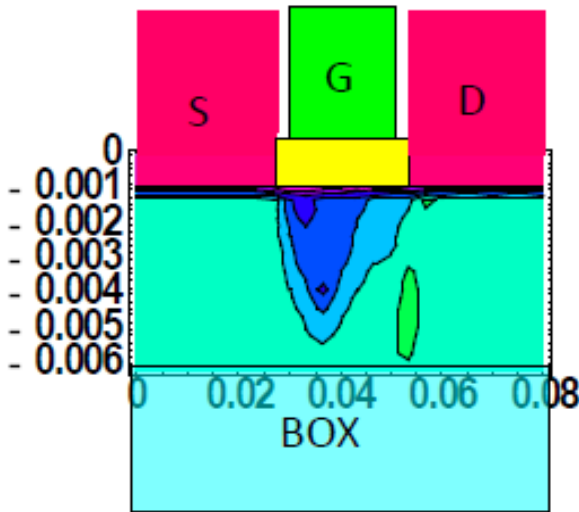
Y-K. Choi, IEEE EDL, p. 254, 2000

Most Leakage Flows >5nm Below Surface

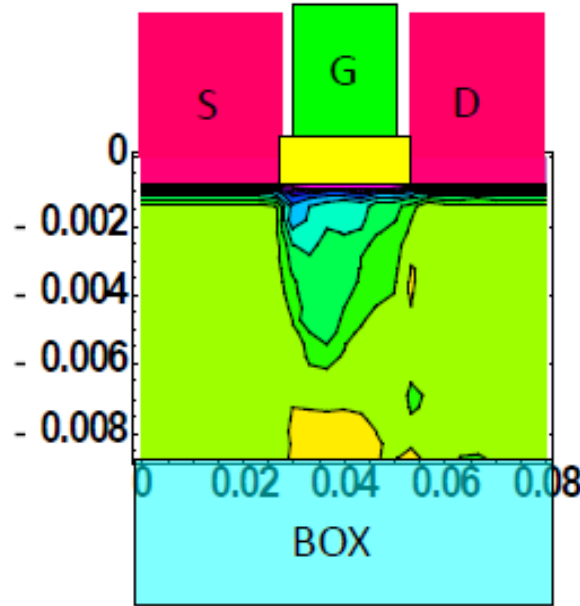
Leakage Current Density



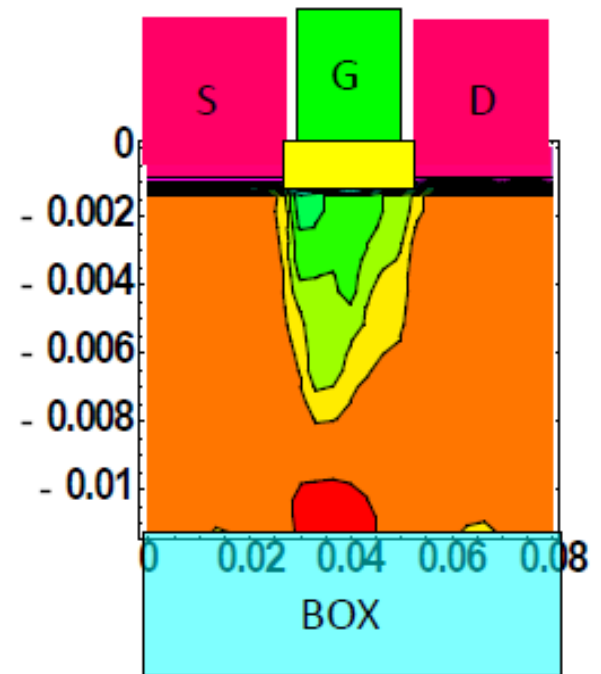
$V_{gs}=0V, V_{ds}=0.7V$
 $L_g=25nm, T_{ox}=1.5nm$



Tsi=5nm



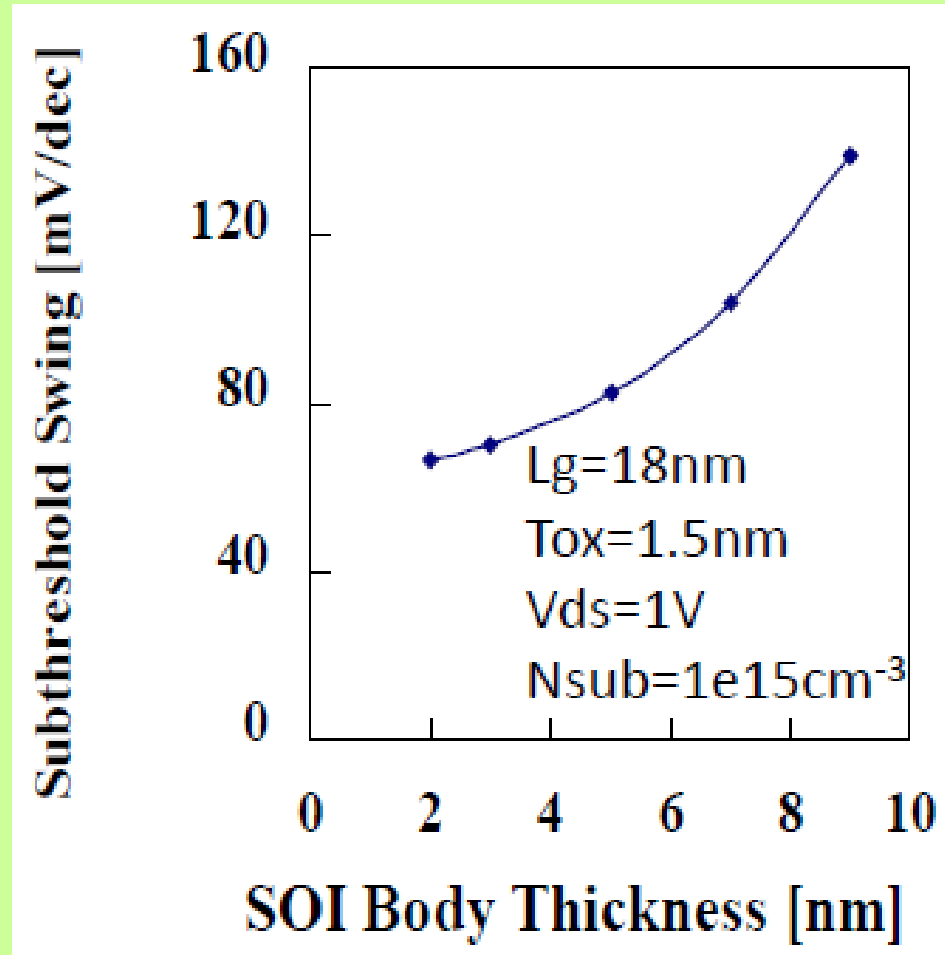
Tsi=7.5nm



Tsi=10nm

Silicon Body Needs to be $<L_g/3$

For good swing and **device variation**

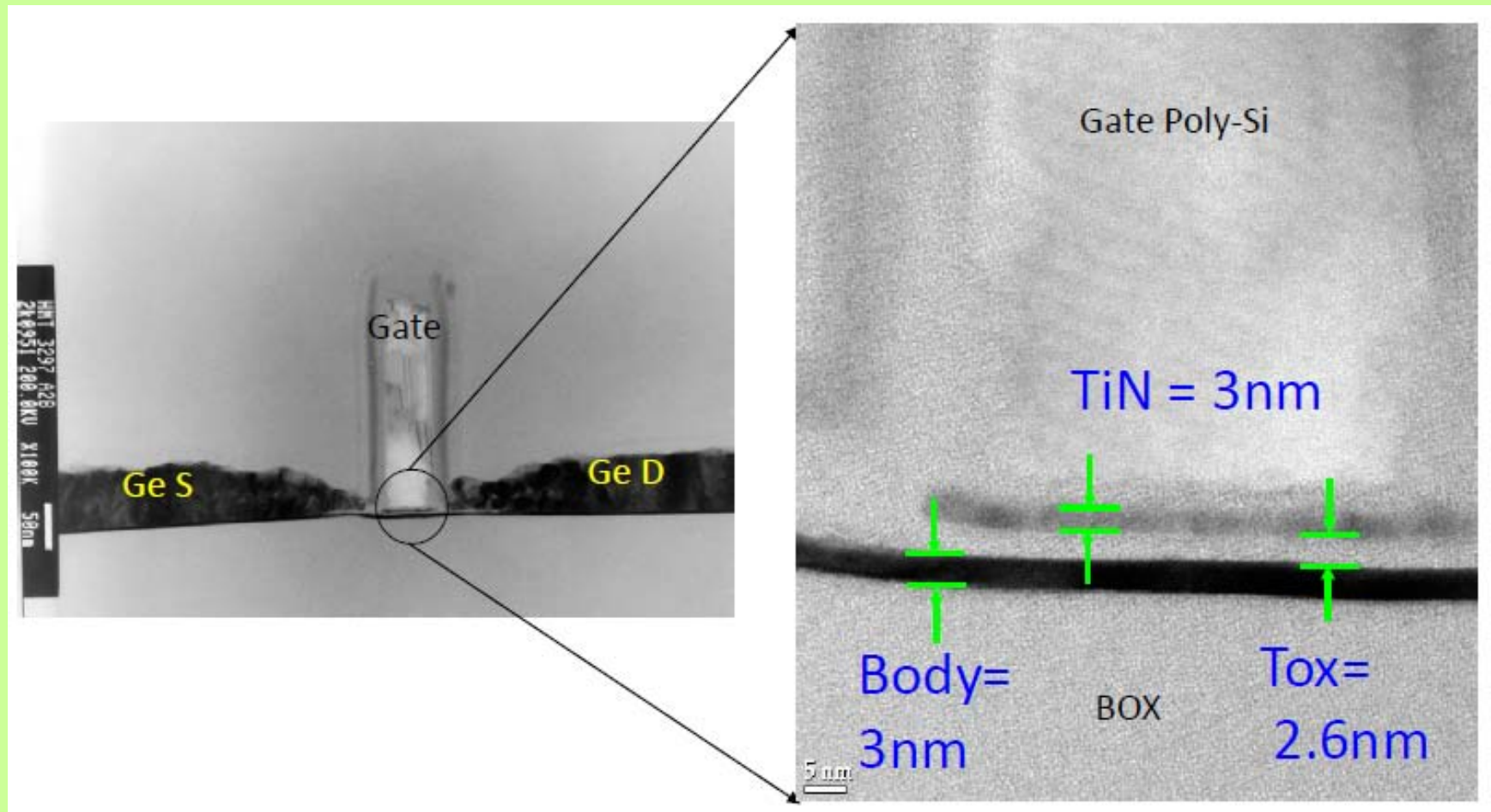


Y-K. Choi et al., IEEE Electron Device Letters, p. 254, 2000

Chenming Hu, July 2011

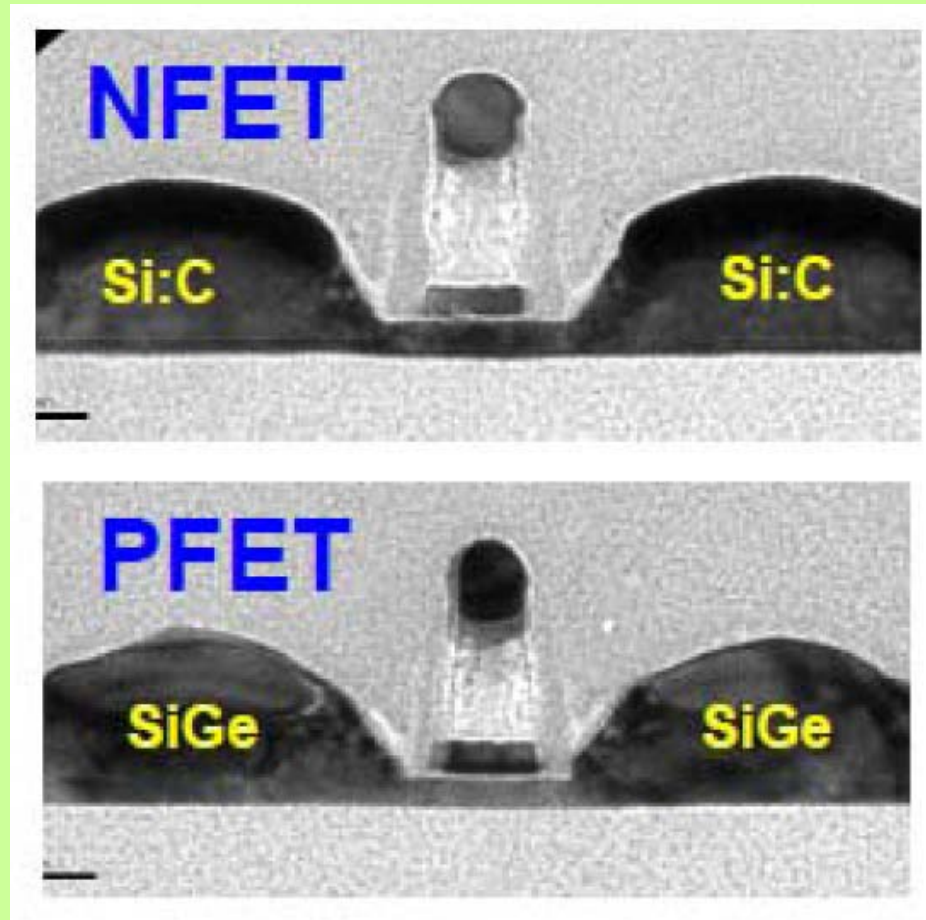
UTB-SOI

3nm Silicon Body, Raised S/D



Y-K. Choi et al, VLSI Tech. Symposium, p. 19, 2001

State-of-the-Art 5nm Thin-Body SOI



ETSOI, IBM
K. Cheng et al, IEDM, 2009

Both Thin-Body Transistors Provide

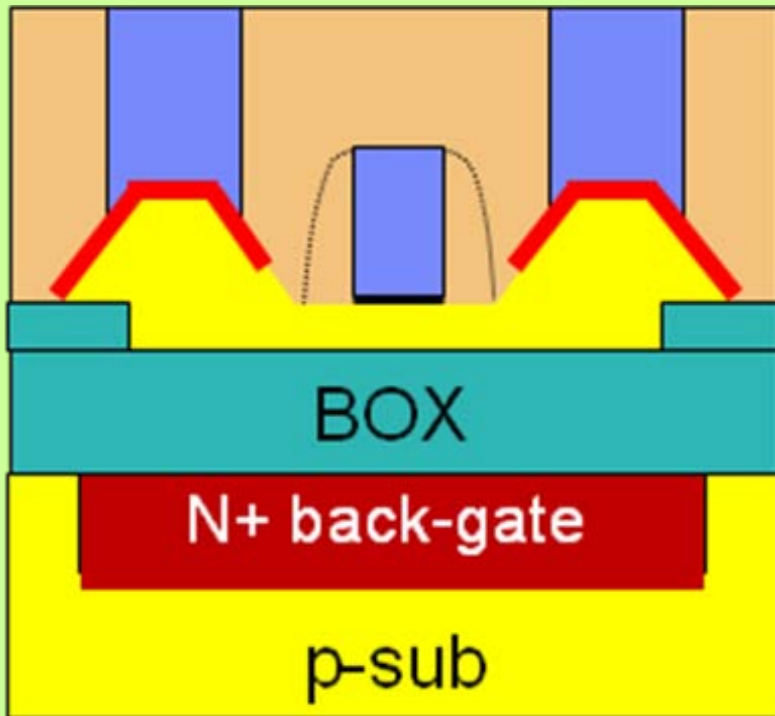
- Better swing.
- S & V_t less sensitive to L_g and V_d .
- No random dopant fluctuation.
- No impurity scattering.
- Less surface scattering (lower E_{eff}).



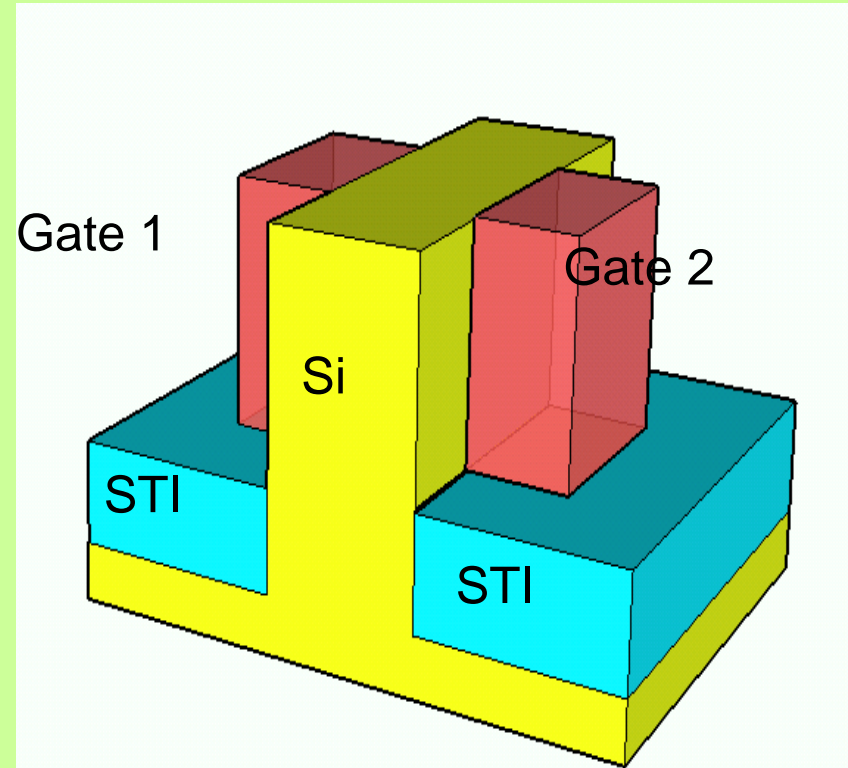
- Higher on-current and lower leakage
- Lower V_{dd} and power consumption
- Further scaling and lower cost

Back-Gate Bias Option

UTB-SOI



FinFET

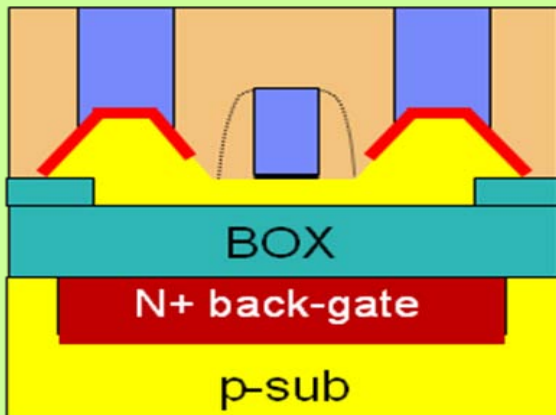


Similarities

- **1996**: UC Berkeley proposed to DARPA two “25nm Transistors”. Both of them
 - use body thickness as a new scaling parameter
 - can use undoped body for high μ and no RDF
- **1999**: demonstrated **FinFET**
- **2000**: demonstrated **UTB-SOI** (**U**ltra-**T**hin **B**ody)
- **Since 2001**: **ITRS** highlights **FinFET** and **UTBSOI**
- **Now**: Intel will use Trigate FinFET.
Soitec readies $\pm 0.5\text{nm}$ substrates for UTBSOI
- **Both FinFET & UTBSOI better than planar bulk!**

Main Differences

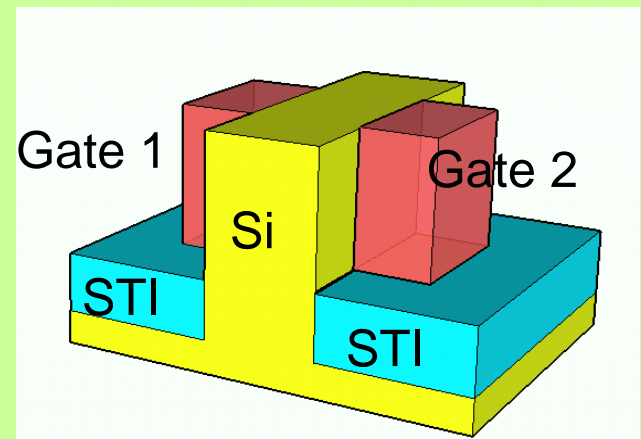
- **FinFET** body thickness $\sim L_g$. Investment by fabs
- **UTBSOI** thickness $\sim 1/3 L_g$. Investment by Soitec
- **FinFET** has clear long term scalability. **UTBSOI** may be ready sooner depending on each firm's readiness with FinFET.
- **FinFET** has larger I_{on} or can use lower V_{dd} . **UTBSOI** has a good back-gate bias option.



UTBSOI



FinFET



What May Happen

- **FinFET** will be used at 22nm by Intel and later by more firms through and beyond 10nm.
- Some firms may use **UTBSOI** to gain/protect market at 20 or 18nm if FinFET is not option.

If so, competition between **FinFET** and **UTBSOI** will bring out the best of both.

If not----- back to first bullet.

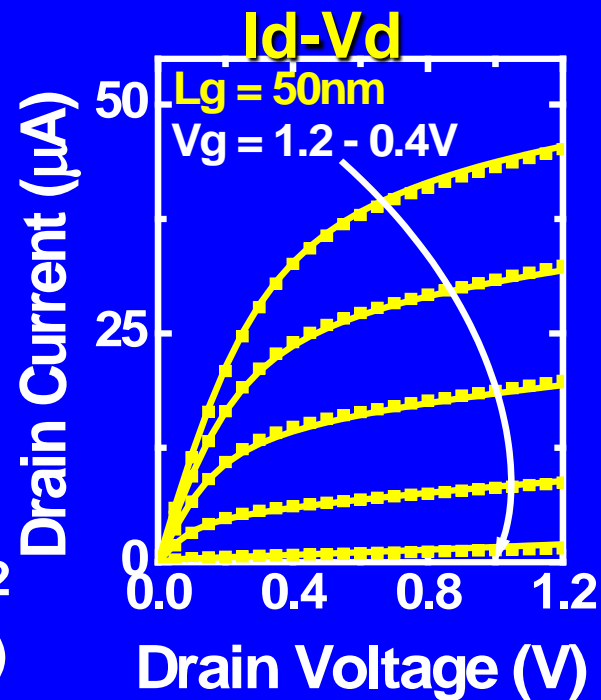
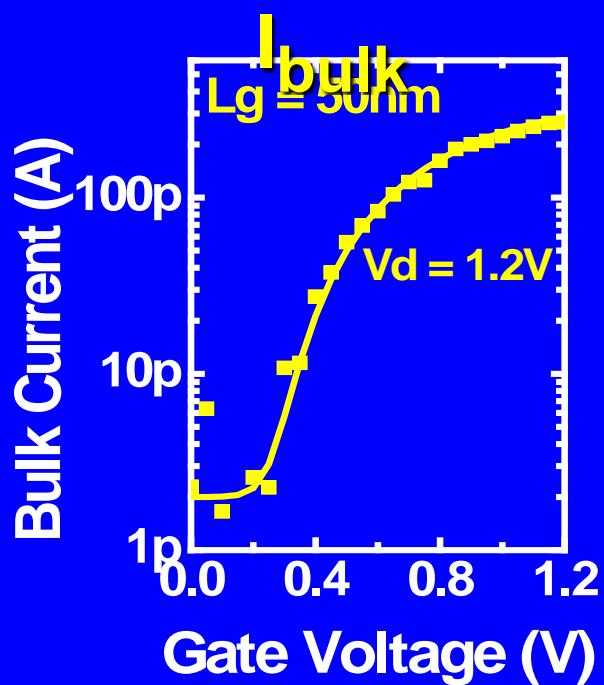
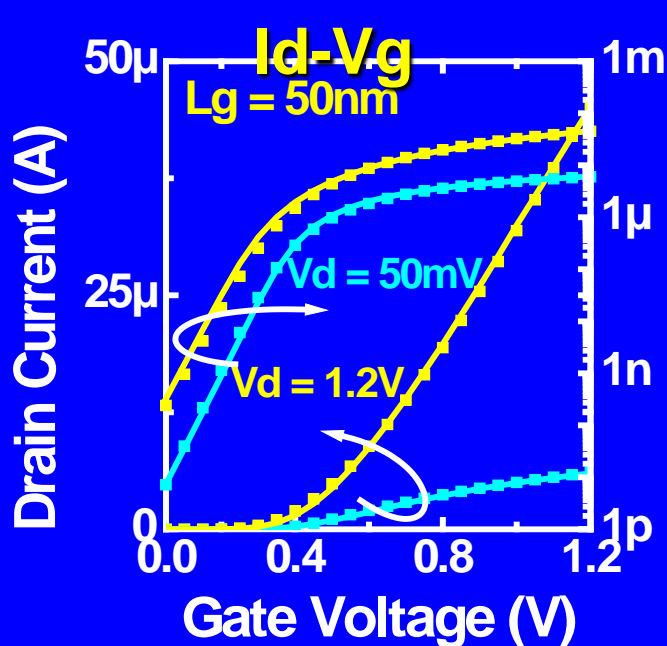
BSIM Family Compact Models

Berkeley Short-channel IGFET Models

- **BSIM4**
- **BSIMSOI**
- **BSIM-MG** for FinFETs: in CMC standardization process
- **BSIM-IMG** for UTB-SOI

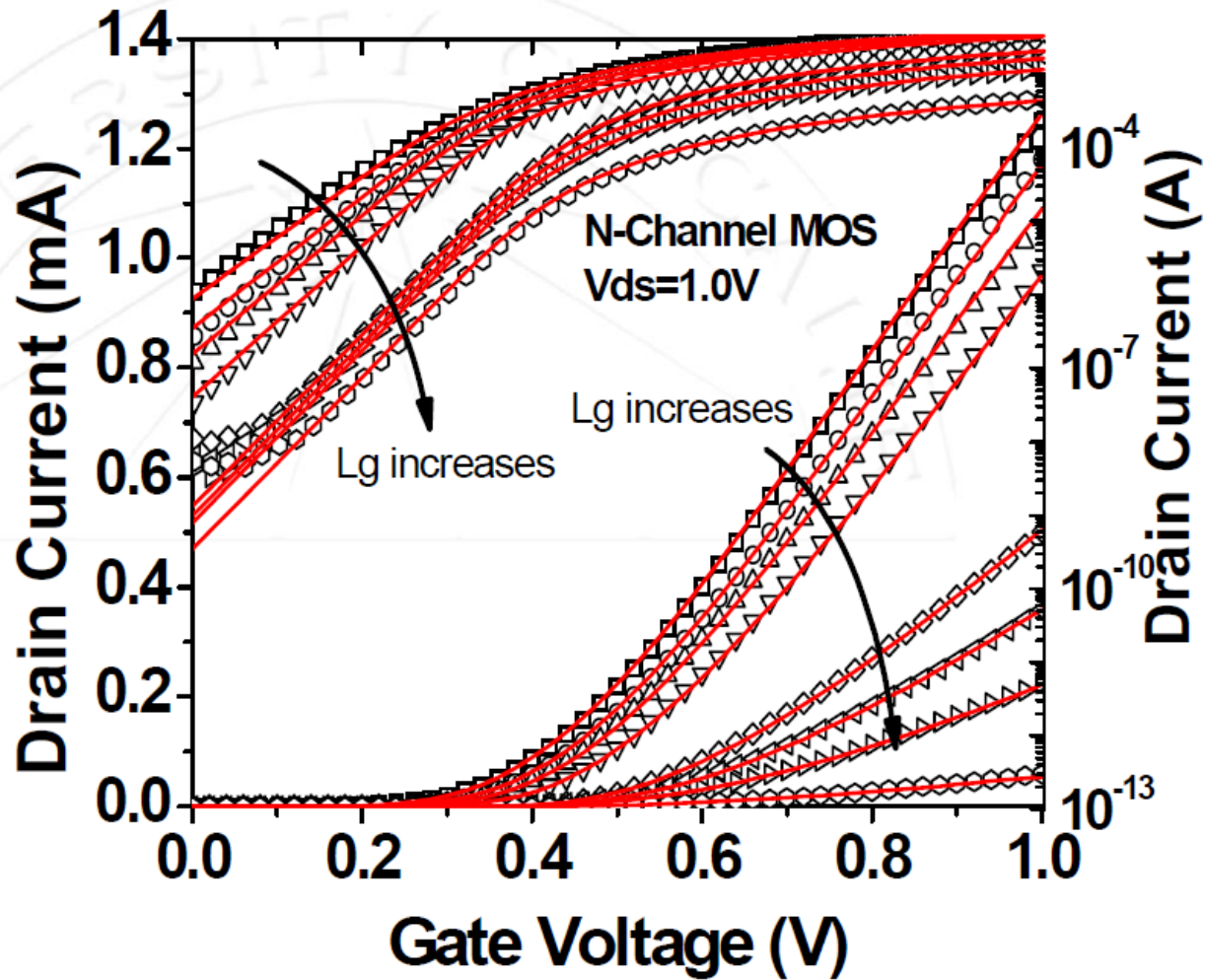
FinFET BSIM Compact Model Verified

- FinFET Fabricated at TSMC.
- $L_g = 30 \text{ nm}-10\mu\text{m}$

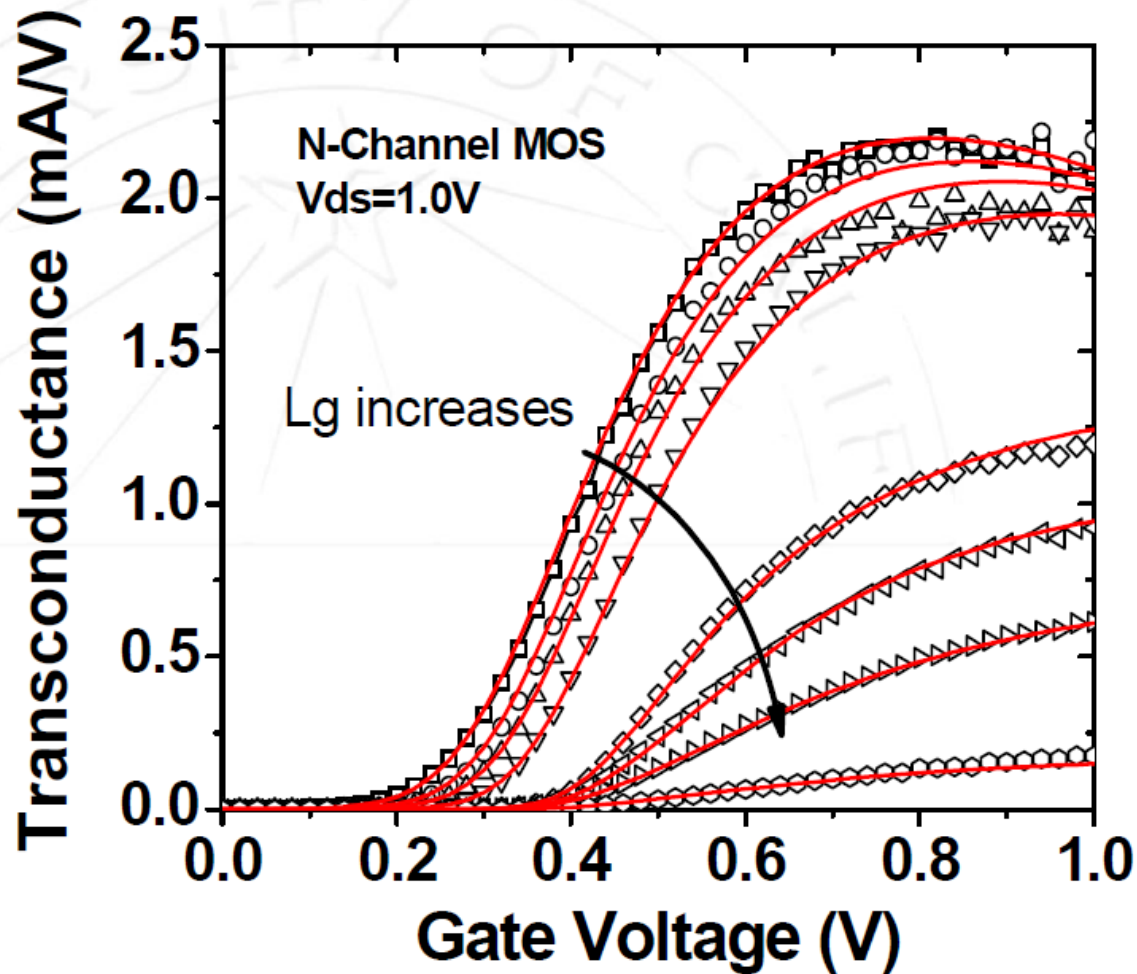


M. Dunga, 2008 VLSI Tech Sym

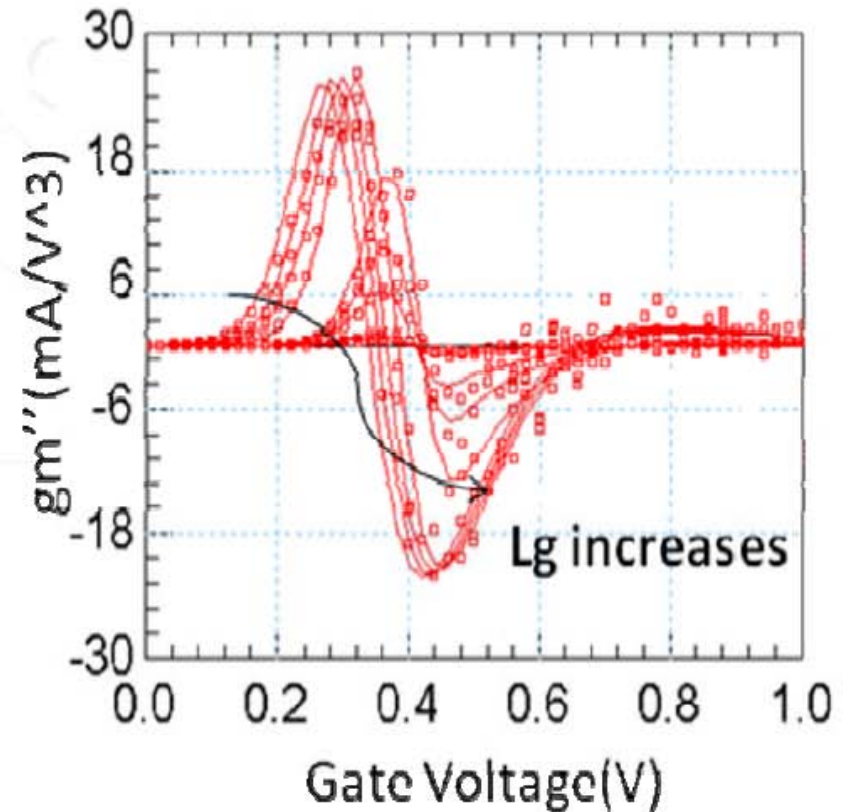
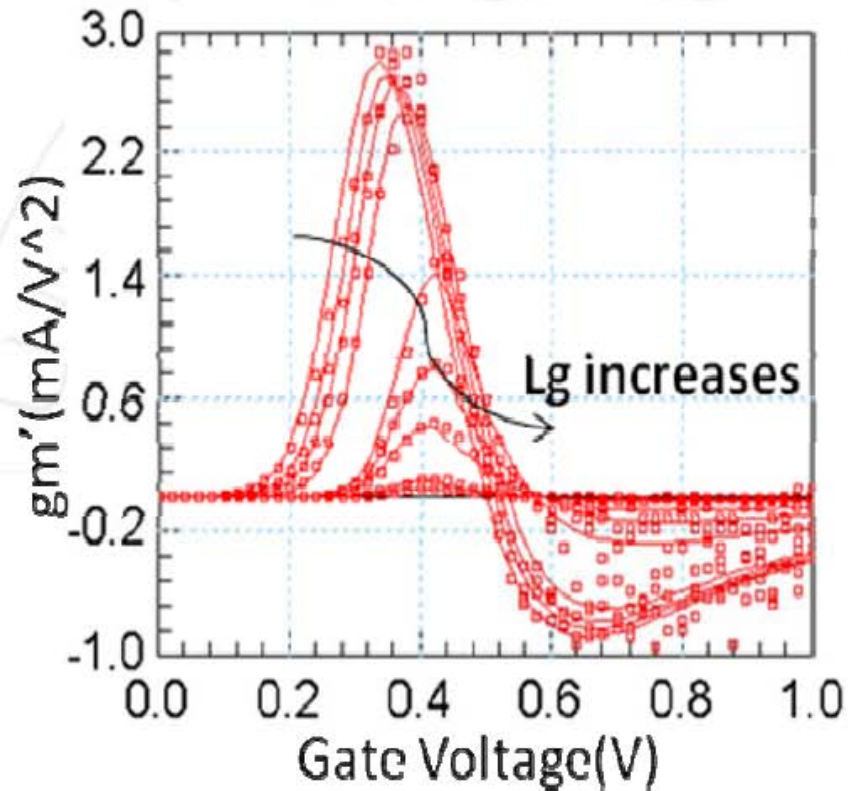
Global fitting with 30nm-10um FinFETs



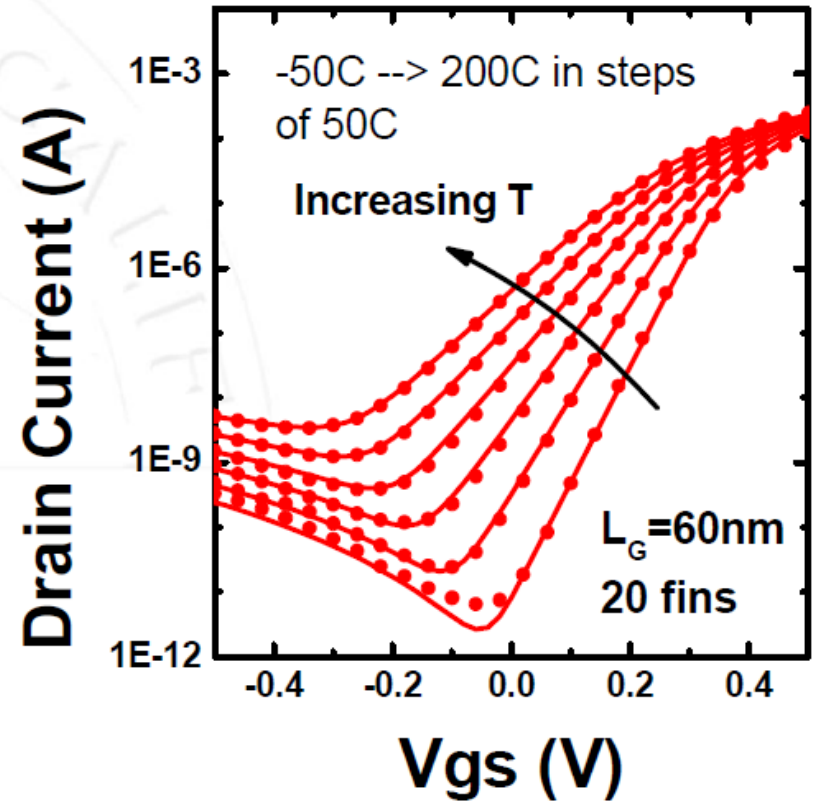
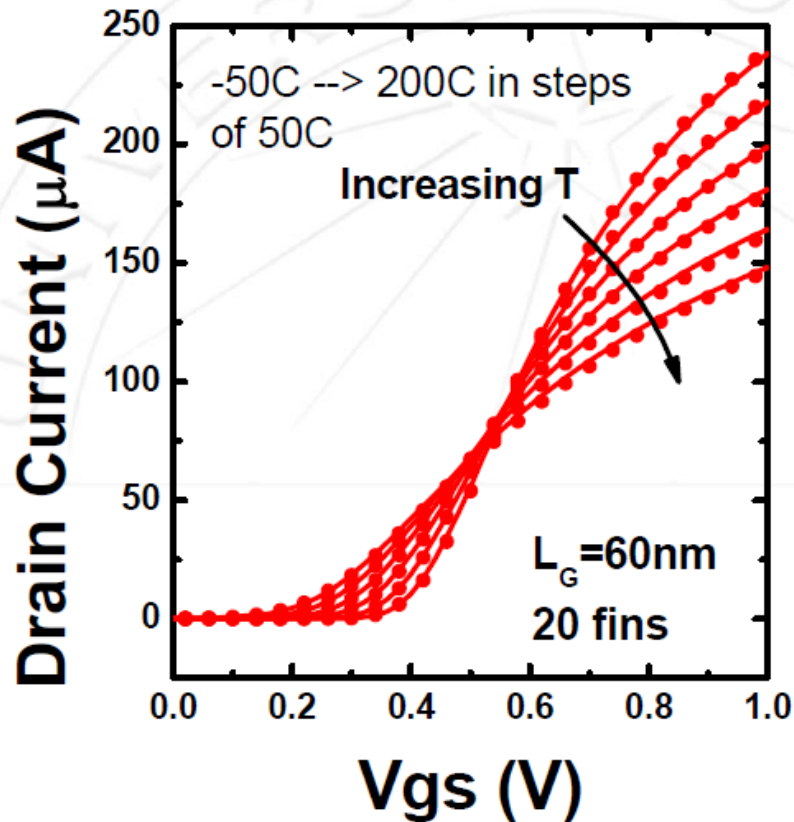
Global fitting with 30nm-10um FinFETs



Global fitting with 30nm-10um FinFETs



Temperature Model Verified for FinFET



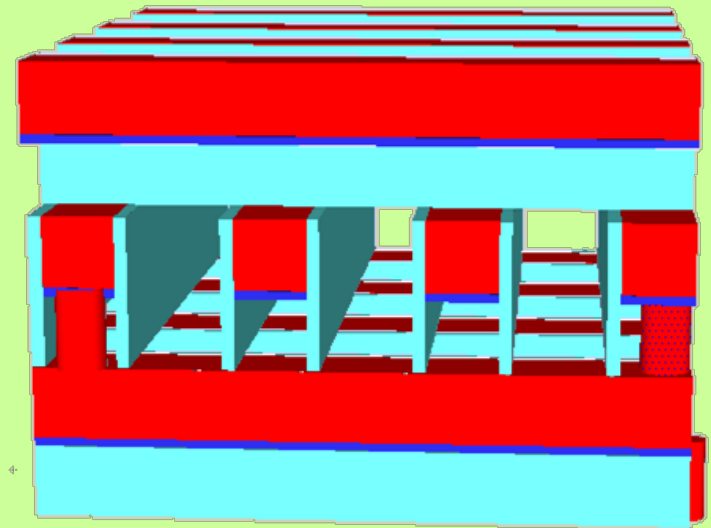
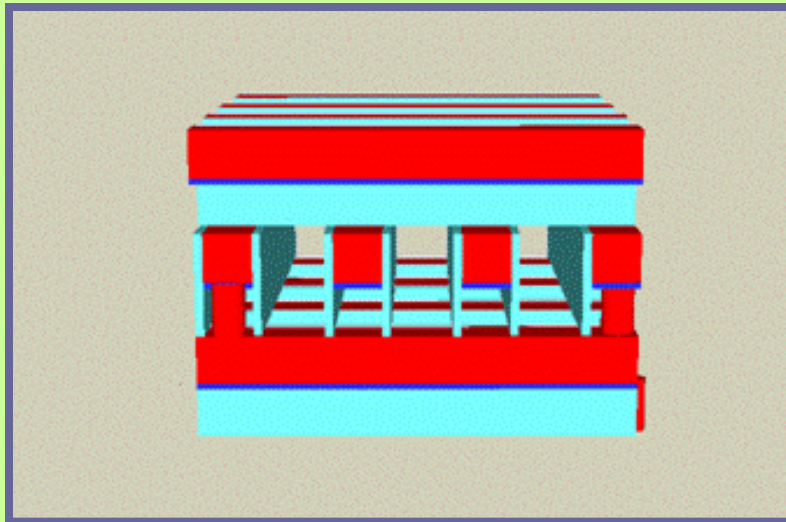
Reduce C

$$f \cdot C \cdot V_{dd}^2$$

Reduce all capacitances.

Vacuum-Sheath Interconnect

- $C_{\text{TOTAL}} \propto \text{Delay}$, $C_{\text{M}} \propto \text{Crosstalk Noise}$



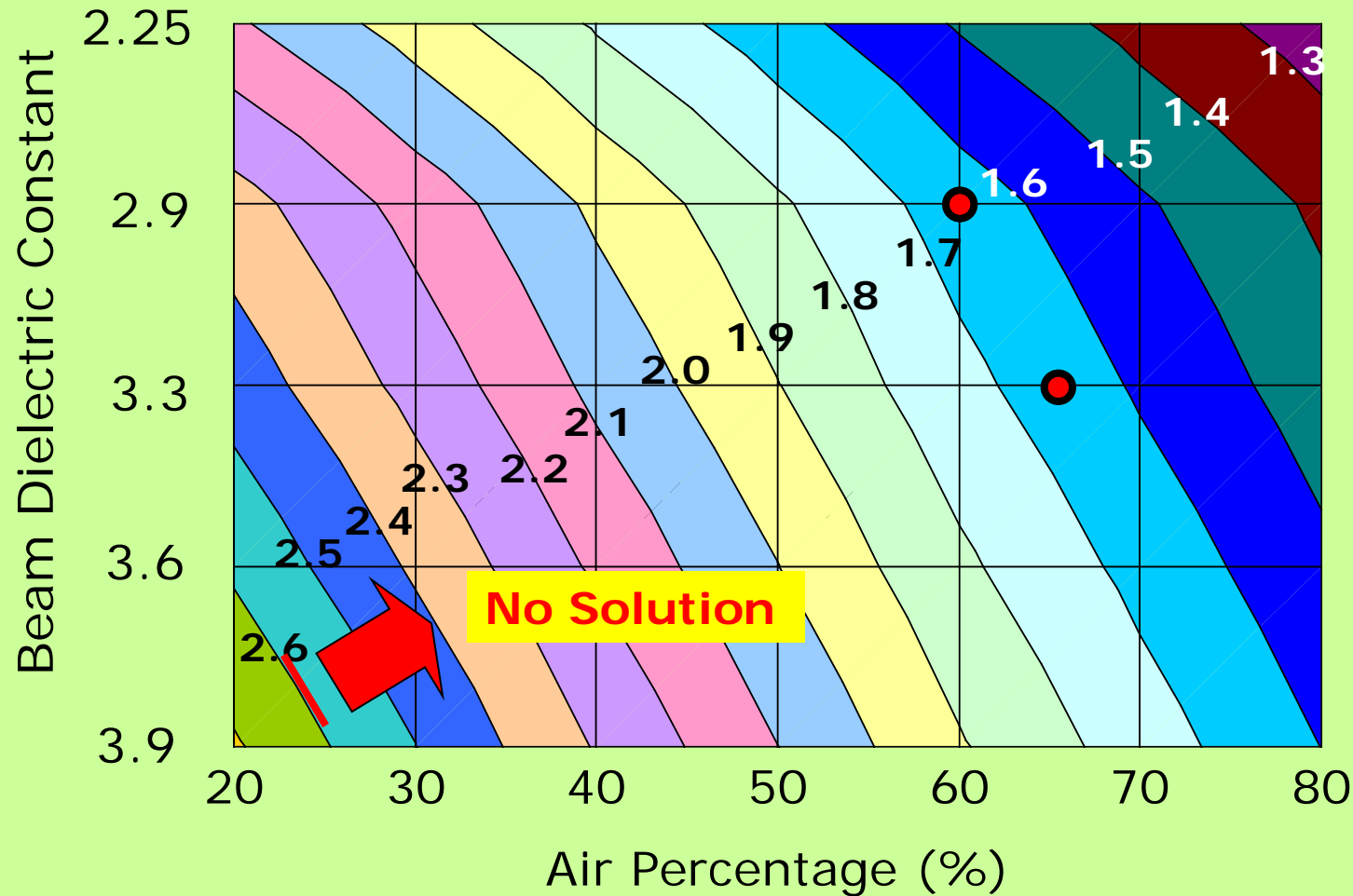
Load Capacitance : C_{O}

Mutual Capacitance : C_{M}

Total Capacitance : C_{TOTAL}

J. Park, Electronics Letters, p. 1294, 2009

Effective k of Vacuum-Sheath Interconnects

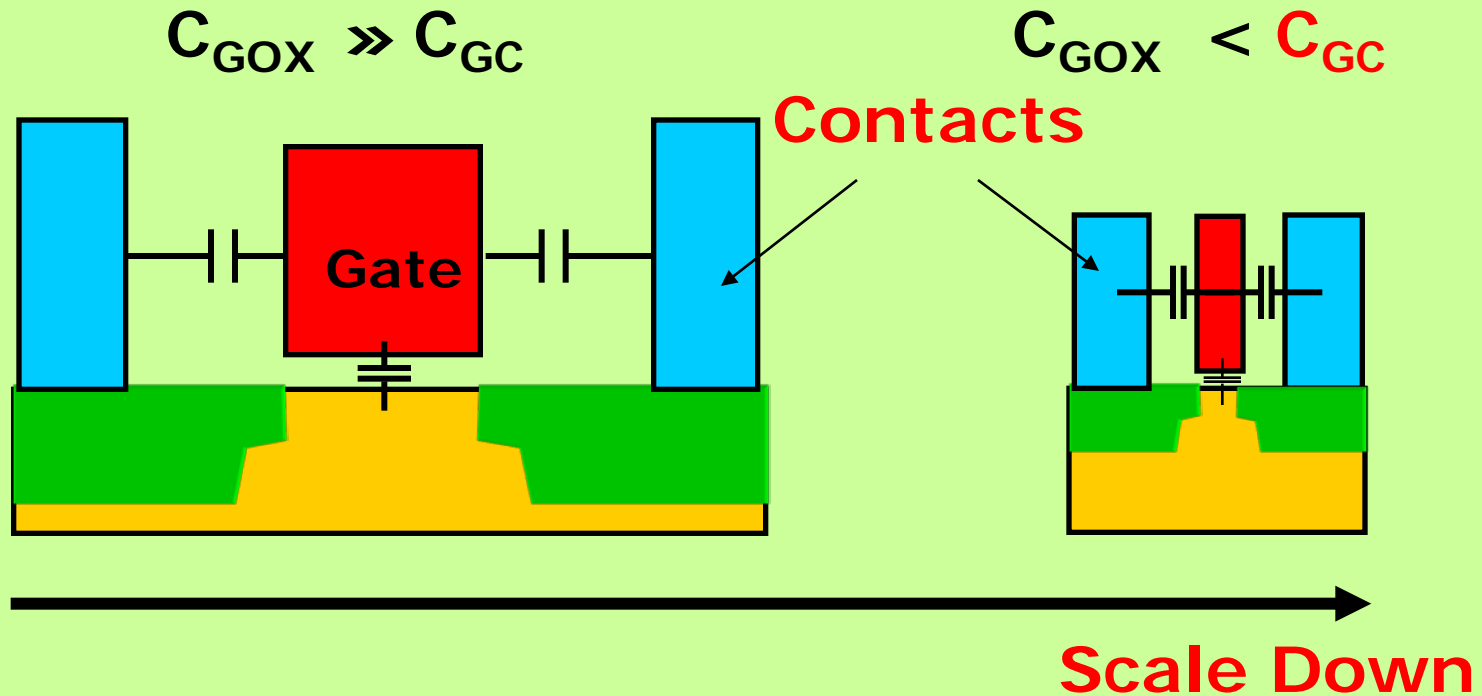


J. Park, Electronics Letters, p. 1294, 2009

Chenming Hu, July 2011

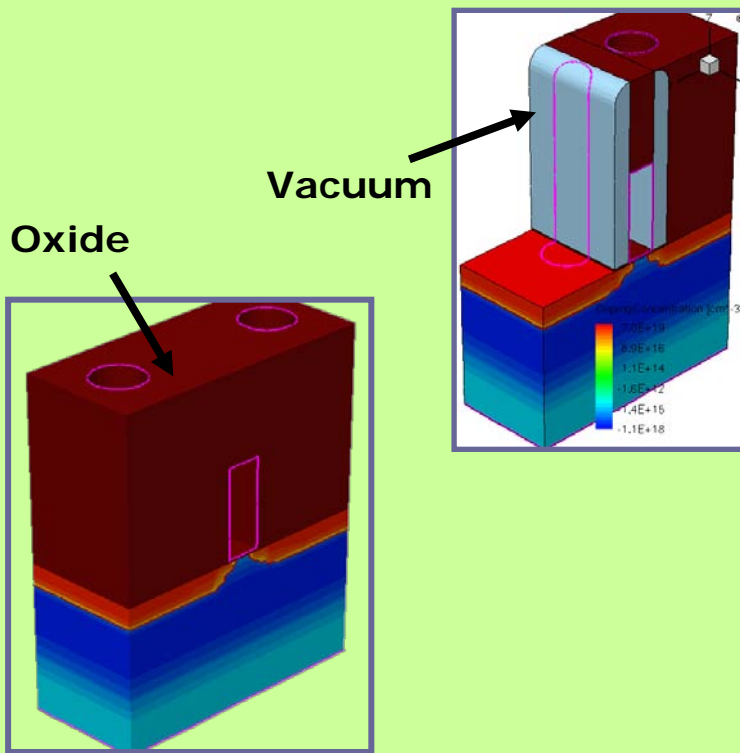
Vacuum Spacer to Reduce C_{GC}

- C_{GOX} : Gate Oxide Capacitance
- C_{GC} : Gate-to-Contact Capacitance



Vacuum Spacer Self-Aligned Contact

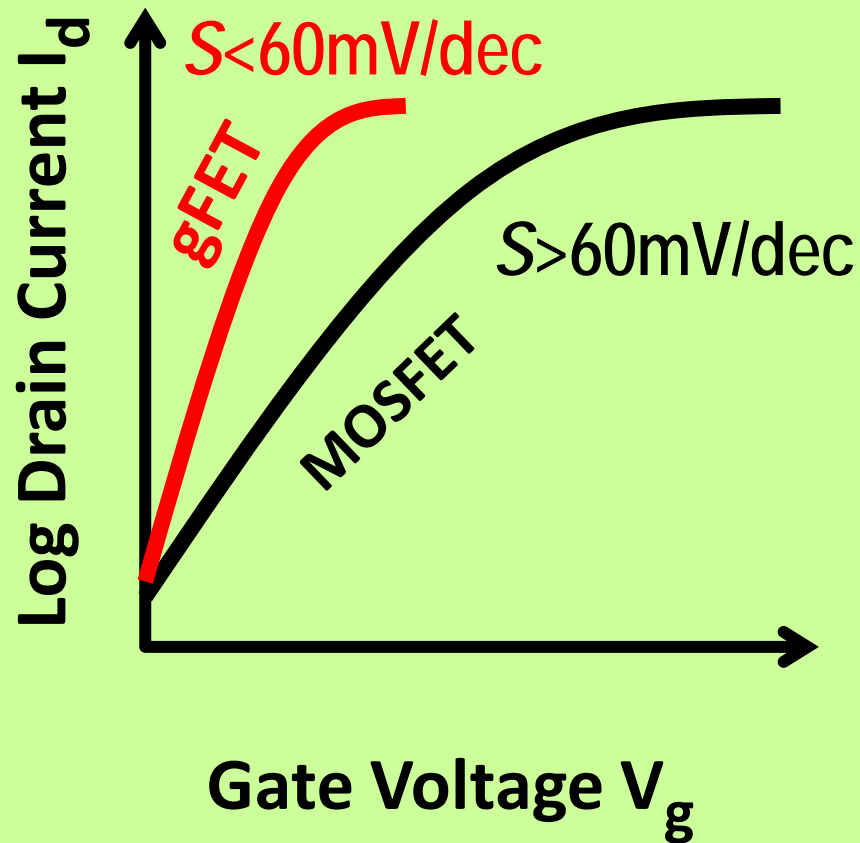
20nm MOSFET comparison



	Oxide Spacer	Vacuum Spacer Self-aligned contact (SAC)
Inverter Delay, ps	6.15 (1)	5.05 (0.82)
Inverter switching energy, fJ	24.2 (1)	18.8 (0.78)
Relative Area	1	0.7

J. Park, IEEE EDL, p.1368, 2009

Future Low Voltage Green Transistor

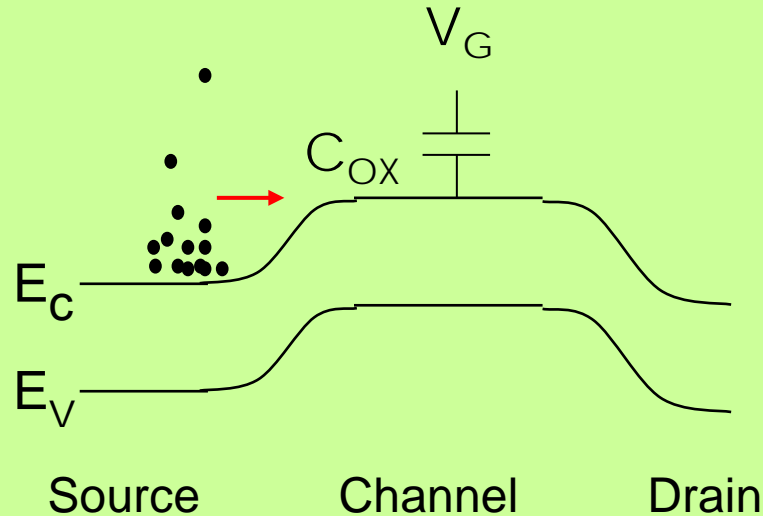


How to reduce V_{dd} to 0.15V?

1. Reduce $V_{dd} - V_t$ to $< 0.1V$ with high-mobility-channel material, or sub-threshold circuits.
2. Reduce V_t to 50mV. Need a device that is free of the 60mV/decade turn-off limit.

Origin of the 60mV/decade Limit

A potential barrier controls the electron flow.

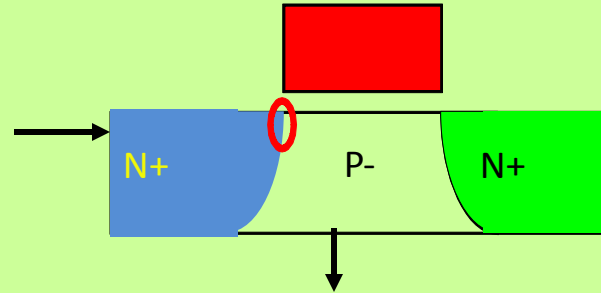
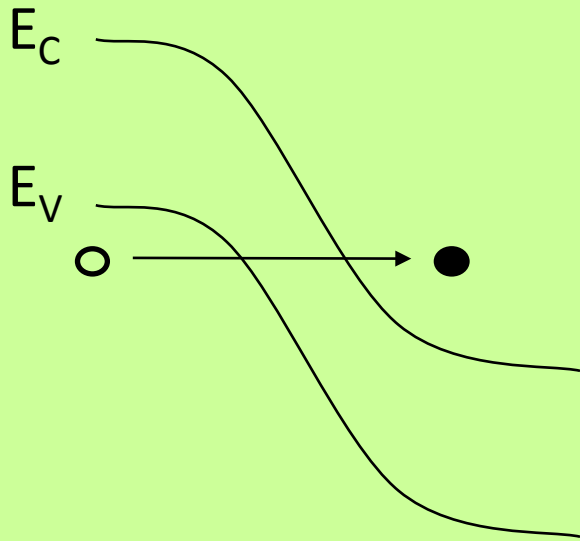


Leakage current is determined by Boltzmann distribution or 60 mV/decade, limiting MOSFET, bipolar, graphene MOSFET...

So, let electrons go **through, not over**, the energy barrier → **semiconductor tunneling** or **MEMS**

Semiconductor Band-to-Band Tunneling:

generating electron/hole pairs



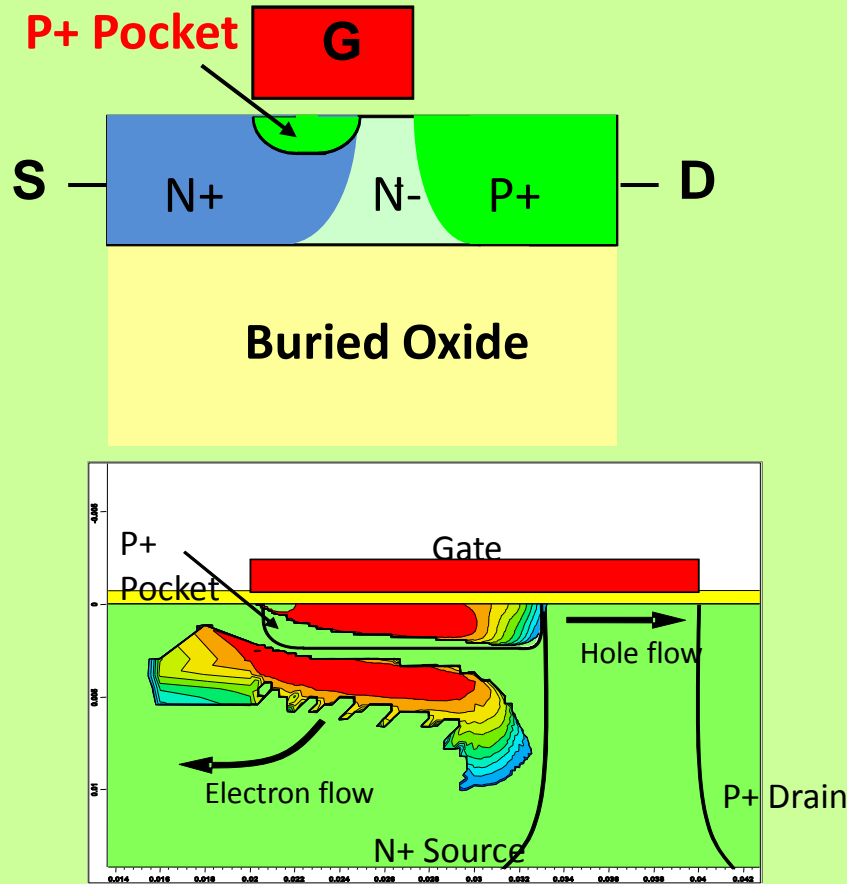
A known mechanism of leakage current since 1985.

Called Gate Induce Drain Leakage (**GIDL**).

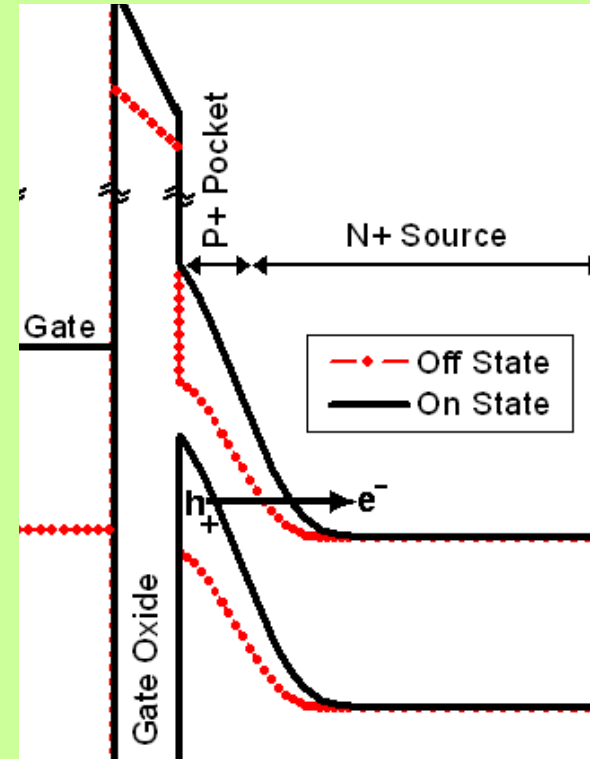
J. Chen, P. Ko, C. Hu, IEDM 1985

Green Transistor --Simulation

C. Hu, 2008 VLSI-TSA, p.14, April, 2008



Simulated carrier generation rates

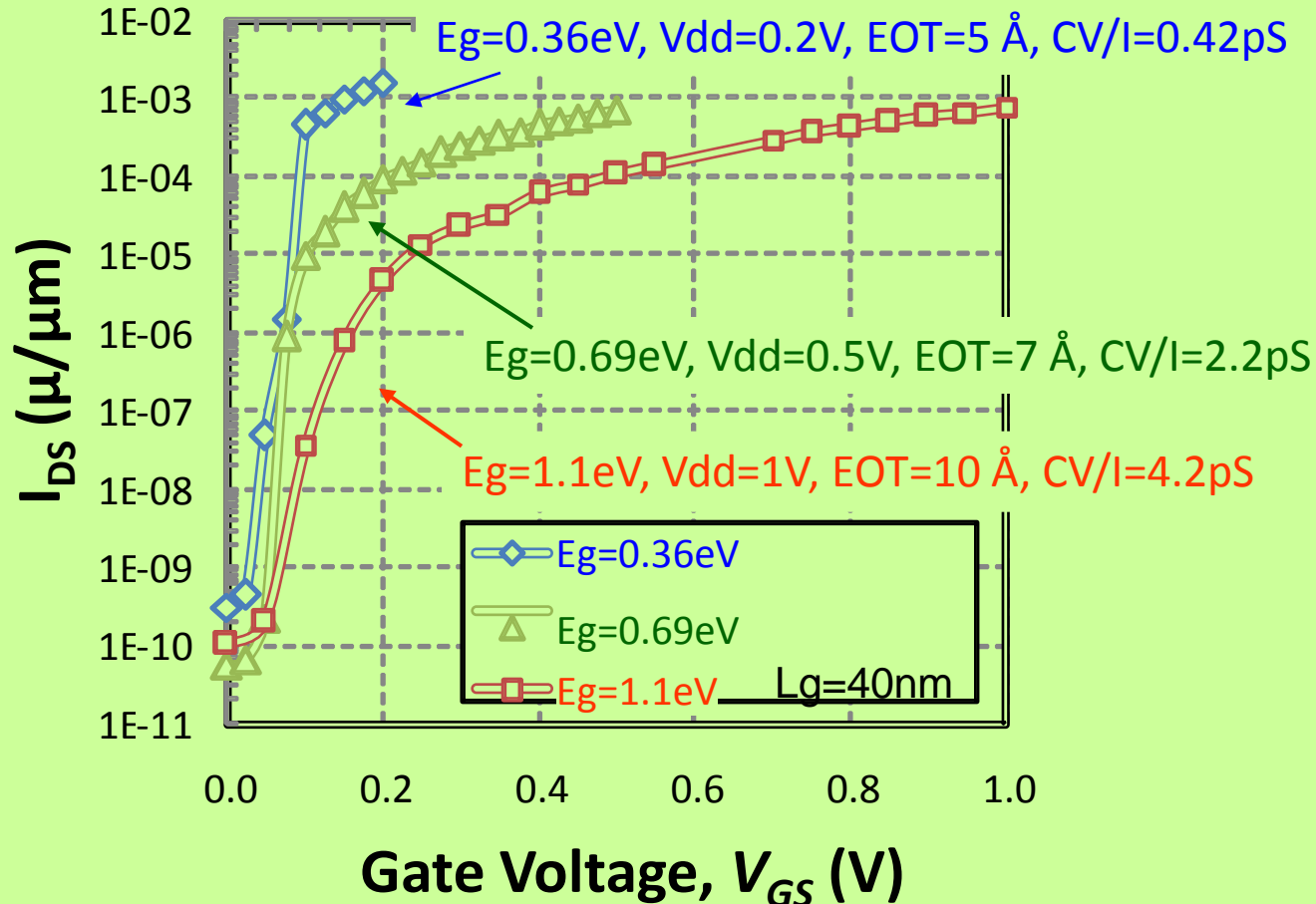


Abrupt turn-on due to over-lap of valence/conduction bands; adjustable turn-on voltage.

C. Hu, 2008 VLSI-TSA, p.14, April, 2008

Reduce Vdd by Reducing Eg

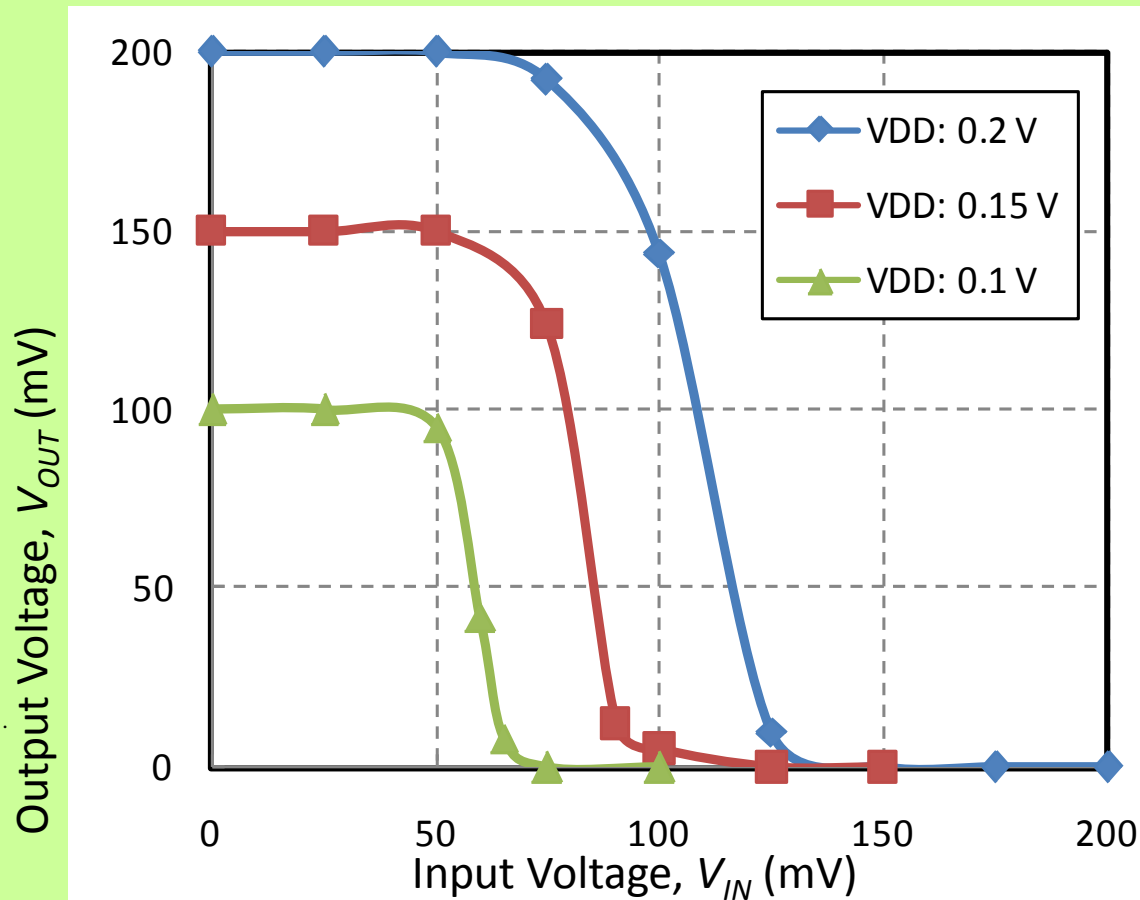
Simulated impact of Eg scaling



Vdd scales down faster than Eg.

Simulated gFET Inverter VTC

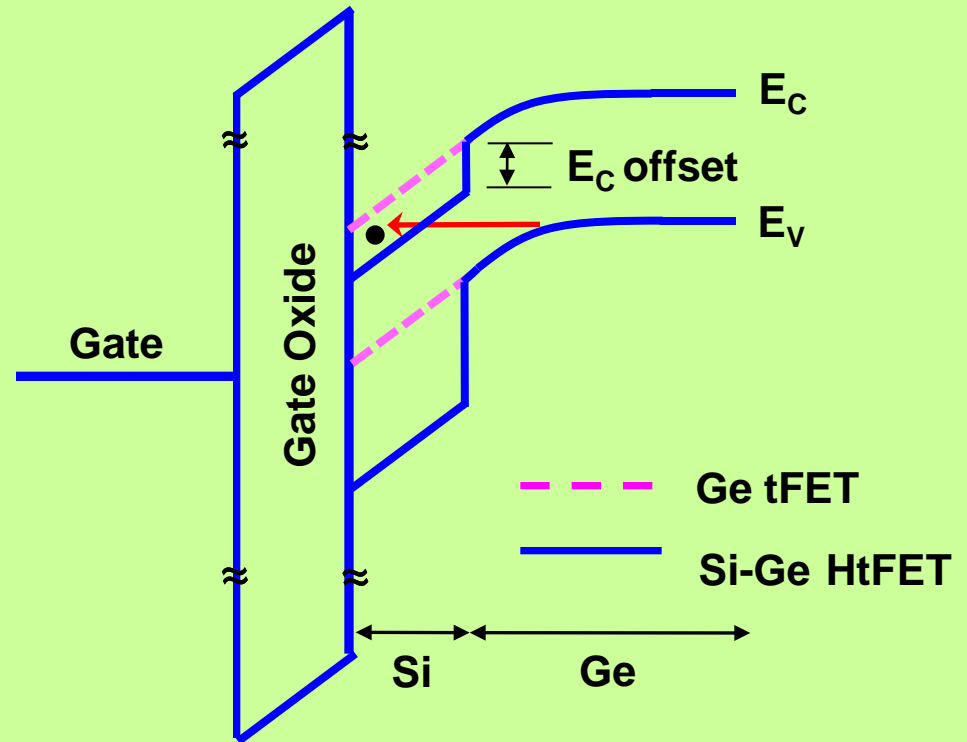
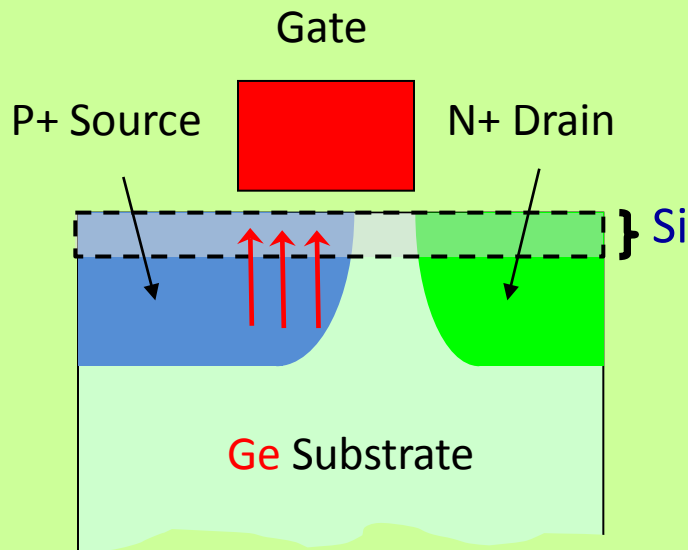
Good voltage gain at 0.1V



C. Hu, 2008 VLSI-TSA, p.14, April, 2008

Hetero-junction gFET

- Strained Si on Ge has 0.18eV “effective tunneling E_g ”.
- III-V.



A. Bowonder, Intern'l Workshop Junction Tech., 2008

Summary

- **FinFET and UTB-SOI are viable new sub-22nm transistors.**
- **Different performances, investment costs, wafer costs, scaling barriers.**
- **Their BSIM SPICE models are available – free 😊**
- **Capacitance and tunnel gFET are potential opportunities.**