FIRST 100 US PATENTS

OF CHENMING HU

1980-2005

US Pat. 4366555 - Aug 1, 1980 Electrically erasable programmable read only memory

US Pat. 4538246 - Oct 29, 1982 Nonvolatile memory cell

US Pat. 4794565 - Sep 15, 1986 Electrically programmable memory device employing source side injection

US Pat. 4908328 - Jun 6, 1989 High voltage power IC process

US Pat. 5163180 - Jan 18, 1991 Low voltage programming antifuse and transistor breakdown method for making same

US Pat. 5272101 - Aug 9, 1991 Electrically programmable antifuse and fabrication processes

US Pat. 5387812 - Sep 18, 1992 Electrically programmable antifuse having a metal to metal structure

US Pat. 5485031 - Nov 22, 1993 Antifuse structure suitable for VLSI application

US Pat. 5511020 - Nov 23, 1993 Pseudo-nonvolatile memory incorporating data refresh operation

US Pat. 5448513 - Dec 2, 1993 Capacitorless DRAM device on silicon-on-insulator substrate

US Pat. 5489792 - Apr 7, 1994 Silicon-on-insulator transistors having improved current and ESD

US Pat. 5670818 - Aug 16, 1994 Electrically programmable antifuse

US Pat. 5559368 - Aug 30, 1994 Dynamic threshold voltage mosfet for ultra low voltage operation

US Pat. 5599728 - Oct 28, 1994 Method of fabricating a self-aligned high speed MOSFET device

US Pat. 5496751 - Feb 24, 1995 Method of forming an ESD and hot carrier resistant integrated circuit structure

US Pat. 5768182 - May 9, 1995 Ferroelectric nonvolatile dynamic random access memory device

US Pat. 5982003 - Jun 5, 1995 Silicon-on-insulator transistors having improved current and ESD

US Pat. 5631485 - Jun 6, 1995 ESD and hot carrier resistant integrated circuit structure

US Pat. 5880511 - Jun 30, 1995 Low-voltage punch-through transient suppressor employing a dual-base structure

US Pat. 6111302 - Aug 30, 1995 Antifuse structure suitable for VLSI application

US Pat. 5780899 - Sep 27, 1995 Delta doped and counter doped dynamic threshold voltage MOSFET

US Pat. 6005409 - Jun 4, 1996 Detection of process-induced damage on transistors in real time

US Pat. 6027988 - Aug 20, 1997 Method of separating films from bulk by plasma immersion ion implantation

US Pat. 5790436 - Nov 3, 1997 Realistic worst-case circuit simulation system and method

US Pat. 6015999 - Mar 16, 1998 Low-voltage punch-through transient suppressor employing a dual-base structure

US Pat. 6121077 - Sep 10, 1999 Silicon-on-insulator transistors having improved current characteristics and ESD

US Pat. 6344404 - Nov 1, 1999 Method of separation films from bulk by plasma immersion ion implantation

US Pat. 6603187 - Feb 23, 2000 Antifuse structure suitable for VLSI application

US Pat. 6300649 - Aug 4, 2000 Silicon-on-insulator transistors having improved current characteristics and ESD

US Pat. 6413802 - Oct 23, 2000 Finfet transistor structures having a vertical double gate channel and methods

US Pat. 6518105 - Dec 10, 2001 High performance PD SOI tunneling-biased MOSFET

US Pat. RE38608 - Jan 17, 2002 Low-voltage punch-through transient suppressor employing a dual-base structure

US Pat. 6492216 - Feb 7, 2002 Method of forming a transistor with a strained channel

US Pat. 6878610 - Aug 27, 2002 Relaxed silicon germanium substrate with low defect density

US Pat. 6830953 - Sep 17, 2002 Suppression of MOSFET gate leakage current

US Pat. 6855990 - Nov 26, 2002 Strained-channel multiple-gate transistor

US Pat. 6864519 - Nov 26, 2002 CMOS SRAM cell configured using multiple-gate transistors

US Pat. 7022561 - Dec 2 , 2002 CMOS device

US Pat. 7214991 - Dec 6, 2002 CMOS inverters configured using multiple-gate transistors

US Pat. 6794234 - Dec 9, 2002 Dual work function CMOS gate technology based on metal interdiffusion

US Pat. 6674130 - Dec 11, 2002 High performance PD SOI tunneling-biased MOSFET

US Pat. 6720619 - Dec 13, 2002 Semiconductor-on-insulator chip incorporating PD,FD,and multi-gate devices

US Pat. 6812116 - Dec 13, 2002 Method of fabricating a wafer with strained channel layers for increased mobility

US Pat. 6627515 - Dec 13, 2002 Method of fabricating a non-floating body device with enhanced performance

US Pat. 6906398 - Jan 2, 2003 Semiconductor chip with gate dielectrics for high-performance and low leakage

US Pat. 7157774 - Jan 31, 2003 Strained silicon-on-insulator transistors with mesa isolation

US Pat. 6784071 - Jan 31, 2003 Bonded SOI wafer with <100> device layer and <110> substrate for performance

US Pat. 6855606 - Feb 20, 2003 Semiconductor nano-rod devices

US Pat. 7105894 - Feb 27, 2003 Contacts to semiconductor fin devices

US Pat. 6921913 - Mar 4, 2003 Strained-channel transistor structure with lattice-mismatched zone

US Pat. 6955952 - Mar 7, 2003 Strain balanced structure with a tensile strained and compressive strained channels

US Pat. 6949451 - Mar 10, 2003 SOI chip with recess-resistant buried insulator and method of manufacturing

US Pat. 7141459 - Mar 12, 2003 Silicon-on-insulator ULSI devices with multiple silicon film thicknesses

US Pat. 6844238 - Mar 26, 2003 Multiple-gate transistors with improved gate control

US Pat. 6872606 - Apr 3, 2003 Semiconductor device with raised segment

US Pat. 6900502 - Apr 3, 2003 Strained channel on insulator device

US Pat. 7173305 - Apr 8, 2003 Self-aligned contact for silicon-on-insulator devices

US Pat. 6882025 - Apr 25, 2003 Strained-channel transistor and methods of manufacture

US Pat. 6867433 - Apr 30, 2003 Semiconductor-on-insulator chip incorporating strained-channel

US Pat. 7074656 - Apr 29, 2003 Doping of semiconductor fin devices

US Pat. 6864149 - May 9, 2003 SOI chip with mesa isolation and recess resistant regions

US Pat. 7081395 - May 23, 2003 Silicon strain engineering accomplished via use of specific shallow trench

US Pat. 6940705 - Jul 25, 2003 Capacitor with enhanced performance and method of manufacture

US Pat. 6936881 - Jul 25, 2003 Capacitor that includes high permittivity capacitor dielectric

US Pat. 7101742 - Aug 12, 2003 Strained channel complementary field-effect transistors and methods of making same

US Pat. 6847098 - Aug 14, 2003 Non-floating body device with enhanced performance

US Pat. 6958291 - Sep 4, 2003 Interconnect with composite barrier layers and method for fabricating the same

US Pat. 7045836 - Sep 8, 2003 Semiconductor structure having a strained region and a method of fabricating same

US Pat. 7071052 - Sep 22, 2003 Resistor with reduced leakage

US Pat. 7172943 - Sep 24, 2003 Multiple-gate transistors formed on bulk substrates

US Pat. 7126225 - Sep 30, 2003 Apparatus and method for manufacturing a semiconductor wafer with reduced peeling

US Pat. 7105928 - Oct 10, 2003 Copper wiring with high temperature superconductor (HTS) layer

US Pat. 6949443 - Oct 10, 2003 High performance semiconductor devices fabricated with strain-induced processes.

US Pat. 6902965 - Oct 31, 2003 Strained silicon structure

US Pat. 7183137 - Dec 1, 2003 Method for dicing semiconductor wafers

US Pat. 7112495 - Dec 5, 2003 Structure and method of a strained channel transistor and a second semiconductor

US Pat. 7183593 - Dec 24, 2003 Heterostructure resistor and method of forming the same

US Pat. 7057237 - Mar 11, 2004 Method for forming devices with multiple spacer widths

US Pat. 7180134 - Apr 13, 2004 Methods and structures for planar and multiple-gate transistors formed on SOI

US Pat. 7176092 - Apr 16, 2004 Gate electrode for a semiconductor fin device

US Pat. 7112483 - Apr 23, 2004 Method for forming a device having multiple silicide types

US Pat. 7045847 - Apr 26, 2004 Semiconductor device with high-k gate dielectric

US Pat. 7122412 - Apr 30, 2004 Method of fabricating a necked FINFET device

US Pat. 7098119 - May 13, 2004 Thermal anneal process for strained-Si devices

US Pat. 7202122 - Jun 11, 2004 Cobalt silicidation process for substrates with a silicon—germanium layer

US Pat. 7141858 - Jun 18, 2004 Dual work function CMOS gate technology based on metal interdiffusion

US Pat. 6949769 - Oct 4, 2004 Suppression of MOSFET gate leakage current

US Pat. 7208815 - Nov 15, 2004 CMOS logic gate fabricated on hybrid crystal orientations and method

US Pat. 7268024 - Nov 29, 2004 Semiconductor-on-insulator chip incorporating PD, FD, and MG strained-channel

US Pat. 6979867 - Dec 27, 2004 SOI chip with mesa isolation and recess resistant regions

US Pat. 7052964 - Mar 16, 2005 Strained channel transistor and methods of manufacture

US Pat. 7187000 - Mar 16, 2005 High performance tunneling-biased MOSFET and a process for its manufacture

US Pat. 7029994 - Mar 18, 2005 Strained channel on insulator device

US Pat. 7167109 - Mar 31, 2005 Hybrid fractional-bit systems

US Pat. 7208754 - Apr 26, 2005 Strained silicon structure

US Pat. 7037772 - Jun 27, 2005 Method of manufacturing an integrated circuit including capacitor with high-k

US Pat. 7238989 - Aug 11, 2005 Strain balanced structure with a tensile and a compressive trained channel

US Pat. 7265447 - Sep 30, 2005 Interconnect with composite layers and method for fabricating the same

US Pat. 7262086 - Jun 30, 2006 Contacts to semiconductor fin devices

US Pat. 7265447 - Sep 30, 2005 Interconnect with composite layers and method for fabricating the same