

Hiren D. Patel

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Research Interests

- Cyber-physical and hybrid systems
- Embedded systems and real-time embedded processor architectures
- Hardware and software co-design methodologies
- System-level design and verification methodologies
- Models of computation

Education

Postdoctoral Research – University of California, Berkeley Advisor: <u>Edward A. Lee</u> Project: Lead the initiative on the Precision Timed (PRET) machines project. The objective is to reintroduce the notion of timing predictability and timing repeatability to real-time embedded processors.	2007–present
Ph.D. – Virginia Polytechnic and State University (Virginia Tech.), Computer Engineering Advisor: Sandeep K. Shukla Thesis: “ Ingredients for Successful System-Level Automation & Design Methodology ”	2004–2007
M.S. – Virginia Polytechnic and State University (Virginia Tech.), Computer Engineering Advisor: Sandeep K. Shukla Thesis: “ HEMLOCK: HEterogeneous ModeL Of Computation Kernel for SystemC ”	2002–2003
B.S. – Virginia Polytechnic and State University (Virginia Tech.), Computer Engineering	1998–2001

Research Experience

- University of California, Berkeley**, Berkeley, California. 2007–present
Postdoctoral Researcher: *Precision Timed (PRET) machines – Reintroduce time as a first-class entity of real-time embedded system design with emphasis on providing architectural support to guarantee predictable and repeatable timing.*
- Virginia Polytechnic and State University**, Blacksburg, Virginia. 2002–2007
Graduate Research Assistant: *System-level design methodologies with focus on heterogeneous models of computation.*
- IBM Research T. J. Watson**, Yorktown Heights, New York. 2005–2006
Summer Research Engineer: *A micro-architectural system-level framework for early analysis of power, performance, and thermal characteristics.*
- Bluespec Inc.**, Waltham, Massachusetts. 2005–2006
Research Engineer: *SystemC extensions for the simulation of Bluespec's rule-based semantics.*
- Calypto Design Systems**, Santa Clara, California. 2004
Summer Research Engineer: *Simulation performance comparison between SystemC and Verilog designs.*
- Microsoft Corporation**, Redmond, Washington. 2003
Summer Software Test Engineer: *Framework for combinatorial test generation based on pair-wise testing theory.*

Publications

Books

- [1] H. D. Patel and S. K. Shukla, *Ingredients for Successful System Level Design Methodology*, 208 pages, ISBN: 978-1-4020-8471-3, Springer Netherlands, June 2008.
- [2] H. D. Patel and S. K. Shukla, *SystemC Kernel Extensions for Heterogeneous System Modeling*, 172 pages, ISBN: 978-1-4020-8087-6, Springer U.S., January 2005.

Journals

- [3] H. D. Patel and S. K. Shukla, *Model-driven Validation of SystemC Designs*, in EURASIP Journal on Embedded Systems, Volume 2008, Article ID: 519474, 14 pages, April 2008.
- [4] D. A. Mathaikutty, H. D. Patel, S. K. Shukla and A. Jantsch, *SML-Sys: A Functional Framework with Multiple Models of Computation for Modeling Heterogeneous System*, in Design Automation for Embedded Systems, Volume 12, Number 1-2, pp. 1-30, Springer Netherlands, March 2008.
- [5] H. D. Patel and S. K. Shukla, *On Co-simulating Multiple Abstraction Level System Level Models*, in proceedings of **IEEE Transactions in Computer-Aided Design (TCAD)**, Volume 27, Number 2, pp. 394-398, February 2008.
- [6] D. A. Mathaikutty, H. D. Patel, S. K. Shukla and A. Jantsch, *EWD: A Metamodeling Driven Customizable Multi-MoC System Modeling Environment*, in proceedings of **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 12, Number 3, August 2007.
- [7] H. D. Patel and S. K. Shukla, *Heterogeneous Behavioral Hierarchy Extensions for SystemC*, in proceedings of **IEEE Transactions in Computer-Aided Design (TCAD)**, pp. 765-780, April 2007.
- [8] H. D. Patel, D. A. Mathaikutty, D. Berner and S. K. Shukla, *CARH: A Service Oriented Architecture for Validating System Level Designs*, in proceedings of **IEEE Transactions in Computer-Aided Design (TCAD)**, Volume 25, Number 8, pp. 1458-1474, August 2006.
- [9] H. D. Patel and S. K. Shukla, *Towards A Heterogeneous Simulation Kernel for System Level Models: A SystemC Kernel for Synchronous Data Flow Models*, in proceedings of **IEEE Transactions in Computer-Aided Design (TCAD)**, Vol. 24, No. 8, pp. 1261-1271, August 2005.

Conferences

- [10] S. Forbes, H. A. Andrade, H. D. Patel, E. A. Lee, *An Automated Mapping of Timed Functional Specification to A Precision Timed Architecture*, in proceedings of 12th IEEE International Symposium on Distributed Simulation and Real Time Applications (DSRT), October 2008.
- [11] B. Lickly, I. Liu, S. Kim, H. D. Patel, S. A. Edwards, E. A. Lee, *Predictable Programming on a Precision Timed Architecture*, in proceedings of IEEE International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), October 2008.
- [12] B. A. Jose, S. K. Shukla, H. D. Patel and J. Talpin, *On the Deterministic Multi-threaded Software Synthesis from Polychronous Specifications*, in proceedings of IEEE/ACM Formal Methods and Models for Codesign (MEM-OCODE), pp. 129-138, June 2008.

- [13] T. H. Feng, E. A. Lee, H. D. Patel, and J. Zou, *Toward an Effective Execution Policy for Distributed Real-Time Embedded Systems*, in proceedings of IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS) (work in progress), April 2008.
- [14] B. A. Jose, H. D. Patel, S. K. Shukla and J. Talpin, *Generating Multi-threaded Code from Polychronous Specifications*, in proceedings of Synchronous Languages and the Model-driven High-level Programming of Reactive and Embedded Systems (SLAP), Elsevier, March 2008.
- [15] R. Bergamaschi, G. Han, A. Buyuktosunoglu, H. D. Patel, I. Nair, G. Dittmann, G. Janssen, N. Dhanwada, Z. Hu, P. Bose, and J. Darringer, *Exploring Power Management in Multi-Core Systems*, in proceedings of IEEE Asia and South Pacific Design Automation Conference (ASPDAC), pp. 708-713, Seoul, Korea, March 2008.
- [16] R. Bergamaschi, I. Nair, G. Dittmann, H. D. Patel, G. Janssen, N. Dhanwada, A. Buyuktosunoglu, E. Acer, G. Nam, G. Han, D. Kucar, P. Bose, and J. Darringer, *Performance Modeling for Early Analysis of Multi-Core Systems*, in proceedings of IEEE/ACM International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS), pp. 209-214, 2007.
- [17] H. D. Patel and S. K. Shukla, *Model-driven validation of SystemC designs*, in proceedings of IEEE/ACM Design Automation Conference (DAC), pp. 29-34, San Diego, California, June 2007.
- [18] H. D. Patel and S. K. Shukla, *Tackling an Abstraction Gap: Co-simulating SystemC DE with Bluespec ESL*, in proceedings of IEEE Design Automation and Test in Europe (DATE), pp. 279-284, Nice, France, April 2007.
- [19] H. D. Patel and S. K. Shukla, *Deep vs. Shallow, Kernel vs. Language – What is Better for Heterogeneous Modeling in SystemC?*, in proceedings of IEEE Microprocessor Test and Verification (MTV), pp. 68-75, Austin, Texas, 2006.
- [20] H. D. Patel, S. K. Shukla, E. Mednick and R. S. Nikhil, *A Rule-based Model of Computation for SystemC: Integrating SystemC and Bluespec for Co-design*, in proceedings of IEEE/ACM Formal Methods and Models for Codesign (MEMOCODE), pp. 39-48, Napa Valley, California, July 2006.
- [21] H. D. Patel and S. K. Shukla, *Heterogeneous Behavioral Hierarchy for System Level Design*, in proceedings IEEE Design Automation and Test in Europe (DATE), pp. 565-570, Munich, Germany, March 2006.
- [22] D. Berner, H. D. Patel, D. Mathaikutty and S. K. Shukla, *Automated Extraction of Structural Information from SystemC-based IP for Validation*, in proceedings of IEEE Microprocessor Test and Verification (MTV), pp. 99-104, Austin, Texas, 2005.
- [23] D. Berner, H. D. Patel, D. A. Mathaikutty and S. K. Shukla, *SystemCXML: An Extensible SystemC Frontend Using XML*, in proceedings of Forum on Design and Specification Languages (FDL), Lausanne, Switzerland, September 2005.
- [24] D. A. Mathaikutty, H. D. Patel, S. K. Shukla and A. Jantsch, *UMoC++: Modeling Environment for Heterogeneous Systems based on Generic MoCs*, in proceedings of Forum on Design and Specification Languages (FDL), Lausanne, Switzerland, September 2005.
- [25] H. D. Patel and S. K. Shukla, *Towards Behavioral Hierarchy Extensions for SystemC*, in proceedings of Forum on Design and Specification Languages (FDL), Lausanne, Switzerland, September 2005.
- [26] D. A. Mathaikutty, H. D. Patel and S. K. Shukla, *A Functional Programming Framework of Heterogeneous Model of Computation for System Design*, in proceedings of Forum on Design and Specification Languages (FDL), Lille, France, September 2004.
- [27] H. D. Patel and S. K. Shukla, *Towards A Heterogeneous Simulation Kernel for System Level Models: A SystemC Kernel for Synchronous Data Flow Models*, in proceedings of IEEE Great Lakes Symposium on VLSI (GLSVLSI), pp. 248-253, Boston, Massachusetts, April 2004.

- [28] H. D. Patel and S. K. Shukla, *Towards A Heterogeneous Simulation Kernel for System Level Models: A SystemC Kernel for Synchronous Data Flow Models*, in proceedings of International Symposium in VLSI (ISVLSI), IEEE Computer Society Press, pp. 240-242, Lafayette, Louisiana, February 2004.
- [29] S. Sharad, D. Bhaduri, M. Chandra, H. D. Patel, and S. Syed, *Systematic Abstraction of Microprocessor RTL models to enhance Simulation Efficiency*, in proceedings of IEEE Microprocessor Test and Verification (MTV), pp. 103-108, Austin, Texas, September 2003.
- [30] P. Kachroo, S. Shukla, T. Erbes, and H. D. Patel, *Stochastic Learning Feedback Hybrid Automata for Power Management in Embedded Systems*, the proceedings of the IEEE Workshop on Soft Computing in Industrial Applications, pp. 121-125, Binghamton, New York, June 2003.

Book Chapters

- [31] D. A. Mathaikutty, H. D. Patel, S. K. Shukla and A. Jantsch, *UMoC++: Modeling Environment for Heterogeneous Systems based on Generic MoCs*, in Advances in Design and Specification Languages for SoCs - Selected Contributions from FDL'05, Chapter 7. Springer Verlag, 2006.
- [32] H. D. Patel, S. K. Shukla. Edited by R. Gupta, P. Le Guernic, S. Shukla, and J. P. Talpin, *Truly Heterogeneous Modeling with SystemC*, ch. Formal Models and Methods for System Design, pp. 88-101, Kluwer Academic Publishers, The Netherlands, 2004.
- [33] H. D. Patel, S. Gupta, S. K. Shukla, and R. Gupta, *Design Issues in 'Embedded Systems'*, CRC Press, 2004.
- [34] H. D. Patel, S. Gupta, S. K. Shukla, and R. Gupta, *A survey of networked embedded systems: An introduction*, in the Handbook of Information Technology, CRC Press, 2004.

Technical Reports

- [35] H. D. Patel, B. Lickly, B. Burgers and E. A. Lee, *A Timing Requirements-Aware Scratchpad Memory Allocation Scheme for a Precision Timed Architecture*, EECS Department, University of California, Berkeley, Technical Report No. UCB/EECS-2008-115, September 12, 2008.
- [36] S. Bandyopadhyay, T. H. Feng, H. D. Patel and E. A. Lee, *A Scratchpad Memory Allocation Scheme for Dataflow Models*, EECS Department, University of California, Berkeley, Technical Report No. UCB/EECS-2008-104, August 25, 2008.
- [37] P. Derler, T. H. Feng, E. A. Lee, S. Matic, H. D. Patel, Y. Zhao, and J. Zou, *PTIDES: A Programming Model for Distributed Real-Time Embedded Systems*, EECS Department, University of California, Berkeley, Technical Report No. UCB/EECS-2008-72, May 2008.

Ph.D Forum

- [38] H. D. Patel and S. K. Shukla, *Ingredients for Successful System-Level Design Methodology*, IEEE Design Automation and Test in Europe (DATE), Nice, France, April, 2007.

University Booth

- [39] H. D. Patel and S. K. Shukla, *Ingredient for Successful System Level Automation & Design Methodology: Heterogeneous Behavioral Hierarchy*, University booth tool demonstration at Design Automation Conference, San Francisco, California, July, 2006.
- [40] H. D. Patel and S. K. Shukla, *SystemC-H: SystemC Kernel Extensions for Heterogeneous System Modeling*, University booth tool demonstration at Design Automation Conference, San Diego, California, June, 2004.

Mentoring Experience

- Real-time Processor Design for Precision Timed (PRET) Machine** 2007–present
Ph.D. Students: Ben Lickly and Isaac Liu (University of California, Berkeley)
Objective: *Propose a real-time embedded processor architecture for the Precision Timed (PRET) machine. Implement a cycle-accurate model for the PRET machine that is programmable using the GCC toolchain.*
- Programming Models for the Precision Timed (PRET) Machine** 2007–present
Ph.D. Student: Shanna-Shaye Forbes (University of California, Berkeley)
Objective: *Explore a set of programming models for the specification and simulation of real-time embedded systems. In particular, we provided a mapping from National Instrument's LabVIEW Embedded to the Precision Timed machine.*
- C Extensions for Real-time Constructs** 2008
M.S. Student: Bas Burgers (University of Twente) – Google Summer of Code
Objective: *Define and extend C with timing constructs. Use an open-source C/C++ front-end (Clang) to identify these timing constructs and synthesize specific timing instructions for the Precision Timed (PRET) machine*
- EDG-based Static Program Analysis of SystemC** 2006–2007
Undergraduate Student: Derek O'Neill (Virginia Tech.)
Objective: *Static analysis of SystemC source code using commercial C/C++ front-end parser from the Edison Front-end Group (EDG). Parse all SystemC structural and behavioral constructs and represent in an intermediary structure for further processing.*
- Eclipse plugin for SystemC IDE** 2006–2007
Undergraduate Student: Nick Sandanato (Virginia Tech.)
Objective: *An Eclipse-based SystemC modeling, development and simulation environment. Some of the supported features are managed make projects, syntax highlighting, code folding, content assist and outline manipulation.*
- Static Dataflow Specification with Abstract State Machines** 2006
Undergraduate Student: Aaron Mhyr (Virginia Tech.)
Objective: *Formal specification of Static Dataflow scheduling algorithms with Abstract State Machines for model-checking and test generation.*
- Graduate Grader: Network Programming** 2002
Students: Graduate and Senior Undergraduates (Virginia Tech.)
Responsibility: *Network programming using C++ and Winsock API. Evaluating and assisting students with technical projects and implementation.*
- Graduate Teaching Assistant: Advanced Digital Design** 2002
Students: Graduate and Senior Undergraduates (Virginia Tech.)
Responsibility: *Preparing and grading laboratory projects for digital systems using VHDL and Xilinx FPGA boards.*

Teaching Experience

- Virginia Polytechnic and State University**, Blacksburg, Virginia. 2002
Graduate Teaching Assistant: *Grade and aid students in projects and homework for a course on advanced digital design of systems using VHDL and Xilinx FPGA platforms.*
- Virginia Polytechnic and State University**, Blacksburg, Virginia. 2002
Graduate Grading Assistant: *Grade projects and assignments for a course on network programming using C++ and Winsock API.*
- Virginia Polytechnic and State University**, Blacksburg, Virginia. 2001-2002
Mathematics Teaching Assistant: *Tutor small groups of students in Freshman and Sophomore-level Mathematics courses.*
- Virginia Polytechnic and State University**, Blacksburg, Virginia. 1999-2001
Mathematics Teaching Assistant: *Assist students in Freshman-level Mathematics courses.*

Professional Activities

Professional Society Membership

- Member, IEEE 2001–

Journal Activities

- IEEE Transactions on Computer Aided Design of Integrated Circuits (TCAD)
Reviewer 2006–
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
Reviewer 2007–
- IEEE Transactions on Computers (TCSI)
Reviewer 2006–
- ACM Transactions on Embedded Computing Systems (TECS)
Reviewer 2004–
- IEEE Design and Test of Computers
Reviewer 2006–
- EURASIP Journal on Embedded Systems
Reviewer 2007–
- Journal of Zhejiang University-SCIENCE A (ZUSA)
Reviewer 2008

Conference/Workshop Activities

- Design Automation and Test in Europe (DATE)
TPC Member 2008
Reviewer 2004–2007
- Real-Time and Embedded Technology and Applications Symposium (RTAS)
TPC Member 2008
Reviewer 2009
- Design Automation Conference (DAC)
Reviewer 2006–2007
- International Conference on Computer Aided Design (ICCAD)
Reviewer 2005–2006
- International Conference on Embedded Software (EMSOFT)
Reviewer 2008
- International Conference series on Formal Methods and Models for Codesign (MEMOCODE)
Reviewer 2005–2006
- International High Level Design Validation and Test Workshop (HLDVT)
Reviewer 2006–2007
- Forum on Design Languages (FDL)
Reviewer 2004–2006
- International Conference on Embedded Software and Systems (ICCESS)
Reviewer 2005

Tutorials

- S. A. Edwards, H. D. Patel, A. Schyn, S. K. Shukla and J-P. Talpin, *Correct-by-Construction Embedded Software Synthesis: Formal Frameworks, Methodologies, and Tools*, IEEE Design Automation and Test in Europe (DATE), 2009.
- H. D. Patel and S. K. Shukla, *Heterogeneous Modeling of SoCs with System C using Multi-MOC Kernel of SystemC*, IEEE International System-on-Chip Conference, Santa Clara, California, September, 2004.

Session Chair

- Hiren D. Patel, *Emerging Computation Models and Systems*, IEEE Design Automation and Test in Europe (DATE), 2009.

Invited Talks

- Virginia Tech.**, Blacksburg, Virginia. 2008
Title: Predictable Programming on a Precision Timed Architecture
- National Instruments Inc.**, Austin, Texas. 2008
Title: Ingredients for Successful System Level Automation & Design Methodology and a Little More
- University of California, Berkeley**, Berkeley, California. 2007
Title: Ingredients for Successful System Level Automation & Design Methodology
- Nokia Research**, Cambridge, Massachusetts. 2007
Title: Ingredients for Successful System Level Automation & Design Methodology

Honors and Awards

- Design Automation Conference – Young Student Support Program (YSSP) Award 2003
- Dean’s List, Virginia Tech.
- B. K. Tanna Award, International School of Tanganyika 1998
Summary: Outstanding effort for academic success, high academic achievement, significant contribution to community and social development, enthusiasm and attitude towards athletic activities, exemplary behavior and character.
- Honor Roll, International School of Tanganyika

Selected Programming Projects

- Precision Timed Machine cycle-accurate simulator based on the SPARC v8 ISA.
 - <http://chess.eecs.berkeley.edu/pret/>
- Model-driven validation of SystemC using Abstract State Machines.
 - <http://fermat.ece.vt.edu/tools/systemcasm/>
- Heterogeneous hierarchy for System-level Design Languages (SystemC).
 - <http://fermat.ece.vt.edu/tools/hierarchy/index.html>
- CARH: A Service-oriented Architecture for Validating System-level Designs
 - <http://fermat.ece.vt.edu/tools/carh/index.html>
- SystemCXML: FERMAT’s SystemC Parser using Doxygen and XML.
 - <http://systemcxml.sourceforge.net/>