Integrated Regulation for Energy-Efficient Digital Circuits

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Abstract – Linear regulation can reduce the effective supply impedance of digital circuits without increasing their total power dissipation. This can be achieved with a push-pull regulator topology that uses a second, higher-than-nominal supply, comparator-based feedback, and a switched-source follower output stage. Measured results from a 65nm SOI test-chip verify that by using these techniques, regulation reduces supply noise by ~30% while also enabling a slight decrease (~1.4%) in total power.

I. Introduction

With the roughly 1mΩ impedance required by today's 1V, 100A microprocessors, concerns about the effects of supply noise on the robustness, performance, and power dissipation of modern chips have been steadily increasing. Supply noise has always been a major concern for sensitive analog or mixed-signal circuits, but it can have significant impacts on digital circuits as well. For example, noise on the supply voltage directly modulates the delay of digital gates. Thus, supply variations force increased buffering to avoid hold-time violations on fast paths, and decreased nominal delay on slow paths in order to meet performance. Furthermore, overshoots in the supply voltage can accelerate long-term degradation in the transistor characteristics.

To alleviate these concerns, recent works such as [1] and [2] have explored active noise reduction for digital chips. However, these approaches for digital supply regulation increase total power dissipation. Thus, despite the potential robustness benefits of such regulation, its associated power overhead has been a significant barrier to widespread adoption in today's severely power-limited chips.

Since a linear regulator[1] must spend power to reduce noise on the supply voltage, at first glance it may seem impossible to build an integrated regulator that does not increase total power. However, variations in the supply voltage (caused by load current variations) are themselves a direct cause of extra power dissipation. In synchronous digital systems, the operating frequency is set by the minimum average supply voltage over a clock cycle. Hence, to maintain the same performance, noise-induced drops in the minimum supply voltage necessitate an increase in the nominal voltage. Thus, if a regulator consumes less power countering noise than the power saved by reducing the nominal voltage, it will not negatively impact the chip's total power – and in fact may even reduce it.

In this paper, we demonstrate an integrated supply regulator in a 65nm SOI technology that meets the goal of reducing noise without increasing the total chip power. To achieve this objective, the static power dissipation of the regulator (both in the output stage and in the feedback circuitry) must be minimized. As we describe in the next section, minimizing regulator static power leads to a push-pull topology using a second, higher-than-nominal power supply [5,6], comparator-based feedback, and a switched source-follower output stage.

[1] While works such as [3] and [4] have explored integrated switching DC-DC converters, at the nearly 1W/mm^2 power density required in modern processors, these converters have not achieved the efficiencies required not to increase total chip power. Thus, in this paper we focus on integrated linear regulators that efficiently reduce the supply impedance.

II. Regulator Design for Minimal Static Power

Achieving the efficiency required to enable regulation for digital circuits requires optimization of both the regulator's topology and its circuit implementation. Topologically, the most immediate concern is the static power that linear regulators are typically forced to burn in their output stages. Specifically, in order to keep its output impedance decoupled from the impedance of the input supply, a series regulator must maintain a minimum drop-out voltage across its output device. Similarly, a typical shunt regulator must statically burn output current in order to counter bidirectional load current variations.

In order to eliminate the need to statically burn output current, a second, higher-than-nominal supply voltage can be added to create a push-pull shunt regulator [5,6] (Fig. 1). With this second supply, the regulator's nominal output current can be set to zero, but with the appropriate push or pull side turned on when needed to counter noise.

By spending output power only when necessary, this topology has the potential to achieve efficiency high enough to be applied to power-limited digital chips. Since the regulator makes use of a second power supply, we next briefly examine some of the important considerations in the design of the shunt supply network. We then describe circuit techniques for ensuring that the regulator burns minimal static power.

A. Shunt Supply Design

To integrate a push-pull regulator, the pad, pin, and metal resources dedicated to supply distribution must be allocated between the main power supply (V_{dd}) and the shunt supply (V_{shunt}). As long as the regulator delivers current just to counter transient noise, only a small portion (< 5%) of these resources need be used for V_{shunt}. Hence, the impact of this reallocation on the losses of the main supply will be minor.

In addition to properly allocating metal resources between the supplies, steps must be taken to ensure that I_{push} returns only through the on-chip path (Fig. 2). To keep the return current flowing almost entirely through the on-chip path, $||Z_{Vshunt\_dist}(j\omega)||$ should be significantly larger than $1/(\omega C_{Vshunt})$ at the frequencies of interest. Thus, part of V_{dd}'s decoupling

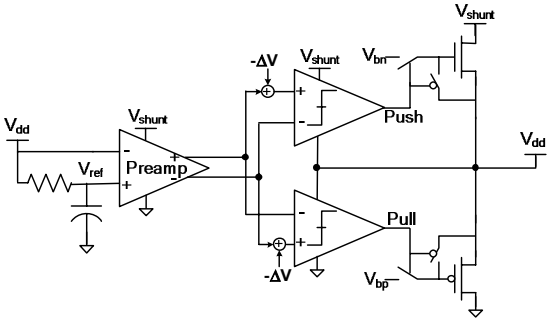


Fig. 1 Push-pull shunt regulator using a second supply voltage V_{shunt}.

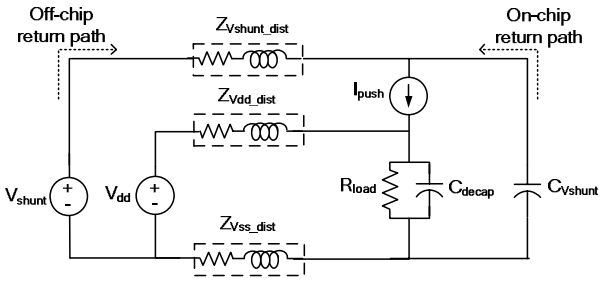


Fig. 2 Simplified model of the supply impedances showing the on- and off-chip return paths for I_{push}.

capacitance must be used for V_{shunt}. To keep the capacitance reallocated to V_{shunt} low (~10% of the total), $||Z_{Vshunt\_dist}(j\omega)||$ must typically be increased as well. To avoid impacting the shunt supply's resistive losses, this is best achieved by increasing V_{shunt}'s series inductance.

Even though the average current through V_{shunt} will be relatively small, the transient currents are set by the full load current variations – making V_{shunt} very noisy. Therefore, to guarantee that the regulator's push-side output device does not fall out of saturation, appropriate margin (typically 200-300mV) must be added to V_{shunt}'s nominal value.

B. Minimizing Static Output Power

Given the low resistance of the main supply distribution network, attempting to counter slowly varying IR drops by statically pushing or pulling current with the regulator would clearly be a waste of power. Thus, to force the regulator to operate only on voltage transients, the regulator's reference is generated by locally RC filtering V_{dd} [5,6], as shown in Fig. 1. Since IR drop varies spatially within the die, a local filter for each regulator location[2] (vs. one global filter) is necessary.

Although this RC reference stops the regulator from spending output current on static IR drops, the output devices could still burn significant current due to their nominal biasing. To robustly ensure that the output devices are completely shut off when the supply is relatively quiet, we can employ comparator-based feedback (shown conceptually in Fig. 1). In order to avoid potential limit cycles, the thresholds of the comparators should be offset to create a symmetric dead-band (as well as to compensate for mismatch).[3]

While the use of comparators increases the feedback gain required over a linear feedback scheme, it allows the use of CMOS inverters as gain stages in the comparator and as buffers to drive the output stages (Fig. 3). As discussed in [8], the efficiency of CMOS buffers in modern processes allows the power consumption of this approach to be the same or less than a comparable design with class-A feedback amplifiers.

C. Minimizing Feedback Circuitry Power

Achieving a voltage-positioned response [9,10] from the regulator (i.e., the regulator's output impedance remains

[2] The impact of high-frequency current noise on the supply network is localized, and therefore a full chip implementation would require many distributed regulator sites. This paper focuses on a single isolated regulator site, but this can be used to project the impact of many sites on an entire chip.

[3] Analysis of appropriate settings for the dead-band width can be found in [7].

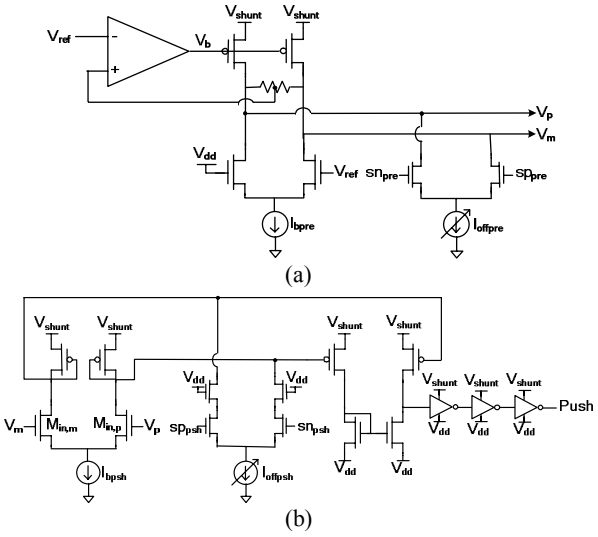


Fig. 3 Implementations of the (a) preamp and (b) push side comparator (the pull side is complementary) from the test-chip described in Section III. The programmable current sources I_{offpre} and I_{offpsh} implement offset cancellation and a tunable dead-band.

constant until the frequency at which the decoupling capacitance reaches the required impedance) can require a high gain-bandwidth (GBW) feedback loop. For example, achieving a worst-case impedance of 10% of the load resistance R_{load} requires an effective feedback g_m of ~$12/R_{load}$ with a bandwidth of ~825MHz (for typical supply network parameters) [7]. To achieve the efficiency required for digital supply regulation, the power cost of achieving this gain-bandwidth from the feedback circuitry must be minimized.

One very effective method to reduce the power required from the feedback circuitry is to employ a source follower-based output stage. To understand the reasons for this, it is instructive to examine the small-signal noise models for shunt regulators (with linear feedback amplifiers) based on common-source and source-follower output stages (Fig. 4).

Typically, most of the loop gain in such a regulator will be contributed by the g_m of the output stage. In fact, the voltage gain of the amplifier itself is often one or less. Thus, in a common-source regulator, the amplifier essentially acts only as a power-consuming wire routing the error signal to M_{pwr}'s

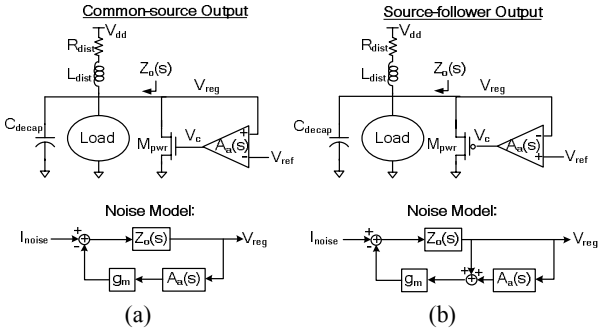


Fig. 4 Shunt regulators with (a) common-source and (b) source-follower output stages and their associated small-signal noise models.

gate. In contrast, with a source-follower output stage, the feedback signal is directly applied to M_{pwr} through a high-bandwidth wire that has no power dissipation.

For a given required output impedance, this intrinsic feedback from the source-follower significantly reduces the requirements on the amplifier's GBW – hence reducing the amplifier's power. At low GBW, one can eliminate the amplifier entirely [11], while even at higher gains it can decrease the required amplifier GBW by over 40%.

Although a regulator for digital circuits will most likely be based on comparators (for the previously described reasons), such a regulator similarly benefits from a source-follower-based output stage. For this application, the two principal requirements on the design of a source-follower-based output stage are achieving low turn-on delay (since feedback delay is analogous to bandwidth in the linear loop), and maintaining predictable output current with a noisy V_{shunt}.

To achieve these goals, as shown in Fig. 5(a), we can employ a replica-biasing scheme where a bias voltage is driven onto the gate of the power device. For efficiency, the power consumption of the amplifier in the replica-bias loop should be minimal, making its output impedance high. This means that directly switching V_{bias} onto the gate of the power device would create disturbances on V_{bias}. While adding capacitance to V_{bias} can reduce the disturbance, this would exacerbate the dependence of I_{push} on the history of the comparator outputs. Hence, it is advantageous to include a buffer to isolate V_{gn} from the high-impedance V_{bias}.

This additional buffer can be implemented as another source follower, as shown in Fig. 5(b). To eliminate its static power, the buffer is turned on only when current is being pushed. However, waiting for I_{sf} to charge V_{gn} up to its final value can cause significant delay, so during the turn-on transition M_{p_up} can be left on to provide a large transient current. For implementation simplicity, the width and magnitude of the pre-emphasis current pulse may be not well-controlled – leading to some transient imprecision in the output current. Fortunately, as long as the transient is short, its effects will be minor, while the improvement in the feedback delay directly impacts the regulator's performance.

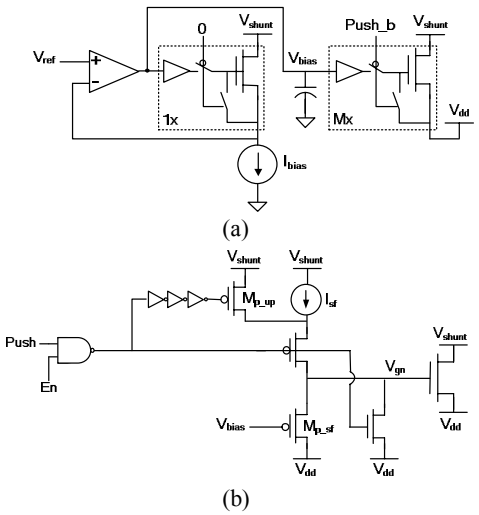


Fig. 5 (a) Replica-bias generation for a source-follower output driver. (b) Push side output driver implementation, highlighting the switched source-follower buffer isolating V_{bias} from V_{gn}.

III. Experimental Verification

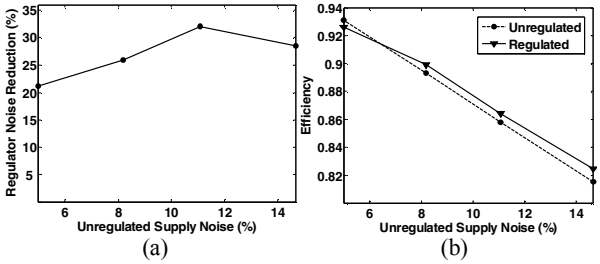
In order to experimentally verify the benefits of integrated regulation for digital logic, in collaboration with AMD, a push-pull shunt regulator was included in a 65nm SOI test-chip used for technology bring-up. The die area of the regulator test-site was ~400µm by 400µm. The supply distribution network was designed with a methodology similar to the rest of the processor test-chip, but with a reallocation of resources for V_{shunt}. To characterize the impacts of regulation, the test-chip included noise generators and a performance monitor circuit.

The programmable on-chip noise generator was used to inject different levels of broadband current noise onto the supply. The noise generator had 5 banks, each consisting of a binary-weighted, 4-bit array of NMOS devices tied between V_{dd} and V_{ss}. Each individual bank can have its magnitude set by a static control signal (such that the bank draws only DC current), or by the lower 4 bits of a 2^{15}-1 PRBS generator. The current noise generated by the PRBS is white up to roughly half of the PRBS generator's clock frequency.

To measure the supply variations as they would impact the performance of the digital circuits themselves, the test-chip also included a performance monitor. The monitor operates by generating a signal that transitions every clock cycle, and then checking on every cycle that this signal was correctly captured by a flip-flop after N stages (typically, 16-24) of fanout-of-four inverters. In this manner, the monitor indicates whether the input clock frequency can be maintained at the worst-case V_{dd}.

The measurement procedure began with picking a supply voltage $V_{dd,set}$, and with the regulator disabled, setting the noise generator to statically draw roughly half of its maximum current (i.e., no noise). The performance monitor was then used to determine the maximum frequency of operation (f_{op}). Leaving this frequency constant, measurements were then taken at 4 magnitudes of current noise.

At each level of current noise, three different measurements were taken. First, with the regulator still disabled and the supply voltage at $V_{dd,set}$, the average power consumption of the chip (at the current noise setting) was recorded. Since the devices within the noise generator banks may not match perfectly, this measurement provides the baseline power (P_{min}) against which to evaluate the chip's efficiency (for that level of noise). Next, with the regulator still off, the supply voltage was raised to the minimum level needed to operate at f_{op}. This voltage ($V_{dd,unreg}$) and the chip's power consumption (P_{unreg}) were once again recorded. Finally, the regulator was turned on, and its parameters were tuned along with the supply voltage (calling the final voltage $V_{dd,reg}$) to achieve minimum power consumption (P_{reg}) at the same f_{op}. The peak-to-peak voltage noise for each current noise setting was calculated as $V_{n,\{unreg,reg\}} = 2(V_{dd,\{unreg,reg\}} - V_{dd,set})$, and the efficiency as $\eta_{\{unreg,reg\}} = P_{min}/P_{\{unreg,reg\}}$.



(a) (b)

Fig. 6 (a) Measured noise reduction provided by the integrated regulator. (b) Measured chip efficiency with and without regulation.

Figure 6 shows the results measured from the chip using this procedure with $V_{dd,set}$=1.188V and V_{shunt}=2.14V. At this $V_{dd,set}$, f_{op} was 1.67GHz and P_{min} (at zero noise) was ~105mW. The static power of the regulator's biasing and feedback circuitry was less than 1.5mW. Based on the measured supply current and calculated peak-to-peak voltage noise, the effective (broadband) unregulated supply impedance was ~869mΩ. For a 12mm by 12mm chip with the same power density (94.5W total power), this corresponds to an impedance of ~966μΩ.

In the range of expected supply noise (~8% peak-to-peak and above), the regulator reduces the noise by ~30%, while successfully maintaining no net increase (in fact, a drop of up to ~1.4%) in total chip power. Although these results already confirm the applicability of regulation to digital circuits, the f_t of the transistors in this developmental process was significantly lower than that of a production process.

With a higher f_t, the benefits of the regulator would be even larger. Fig. 7(a) shows a simulation of the regulated supply impedance with the target f_t for the production process – the noise is reduced by ~50%. Fig. 7(b) shows the same simulation, but with the transistor speed scaled according to the measured performance monitor frequency. Since the measured noise reduction of 30% closely matches the simulation of Fig. 7(b), in a production process we anticipate the regulator to achieve the simulated 50% reduction in noise. With this higher level of noise reduction, a simple model of the regulated chip's efficiency [7] shows the expected reduction in total power increases to ~4%.

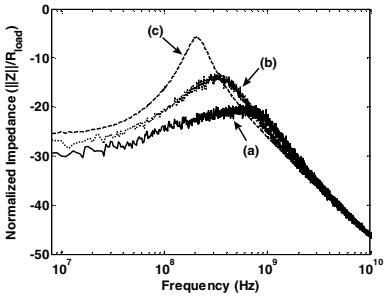


Fig. 7 Simulated effective impedance of (a) regulated supply with production transistors, (b) regulated supply with test-chip transistors, and (c) unregulated supply. The simulations use a block-level model similar to Fig. 4(b), but with comparator-based feedback. The effective impedance of the regulator (which is a non-linear system) was calculated with ~14% peak-to-peak unregulated noise.

IV. Conclusion

In order for on-chip regulation of digital power supplies to be applied in modern, power-limited chips, this regulation must not adversely impact the chip's power dissipation. Fortunately, since variations in the supply voltage force the nominal supply to be increased, the net power overhead of a regulator can in fact be negative. To achieve this goal, a push-pull shunt regulator uses a second power supply and comparator-based feedback, enabling it to spend output power only when necessary to counter noise. Incorporating a switched source-follower output stage minimizes the power consumption of the feedback circuitry.

Measurement results from a fabricated design confirm that regulation can significantly (~30%) reduce the noise on a digital chip's power supply while actually resulting in a slight improvement (~1.4%) in the total power dissipation. While issues related to distributing many regulator sites on a die and adapting the parameters of each of these regulators for maximum efficiency remain, these results show that integrated regulation is a promising approach to improving the robustness of energy-efficient digital circuits.

Acknowledgments

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