

# Elad Alon

Department of Electrical Engineering and Computer Sciences  
University of California, Berkeley  
565 Cory Hall, Berkeley, CA 94720-1770  
<http://www.eecs.berkeley.edu/~elad>  
[elad@eecs.berkeley.edu](mailto:elad@eecs.berkeley.edu)

## ACADEMIC POSITIONS

1/07 – present *Assistant Professor* – University of California, Berkeley, CA  
Department of Electrical Engineering and Computer Sciences  
Co-Director of the Berkeley Wireless Research Center  
*Interests:* Energy-efficient integrated systems; nano/micromechanical relay-based circuit design; on-chip power conversion and management; gigabit-per-second mobile 60GHz wireless transceivers; clocking architectures and circuits.

## EDUCATION

6/02 – 12/06 **Ph.D.** in Electrical Engineering, Stanford University  
*Advisor:* Prof. Mark Horowitz  
*Dissertation topic:* “Measurement and Regulation of On-Chip Power Supply Noise”  
2004-2005 AMD FMA Fellow

9/00 – 6/02 **M.S.** in Electrical Engineering, Stanford University

9/97 – 6/01 **B.S.** with Distinction in Electrical Engineering, Stanford University  
Tau Beta Pi Honor Society, 2000 HP/Agilent EE Undergraduate Design Award

## PAST EXPERIENCE AND EMPLOYMENT

### Research

9/02 – 9/06 *Research Assistant* – Department of Electrical Engineering, Stanford University  
*Interests:* Efficient power supply regulation. Circuits and techniques for on-chip measurement and characterization. Power efficient high-speed link architectures, circuits, and communication techniques. Optimization of multi-mode fiber optical communication systems with adaptive spatial filtering. Applications of optimization and non-linear control to VLSI and high-speed mixed-signal design. Methodologies and tools for modern chip and system design.

### Teaching

1/06 – 3/06 *Teaching Affiliate* – Department of Electrical Engineering, Stanford University  
EE313 – Digital MOS Integrated Circuit Design

1/03 – 3/03 *Teaching Affiliate* – Department of Electrical Engineering, Stanford University  
EE272 – Design Projects in VLSI Systems

9/01 – 6/03 *Teaching Assistant* – Department of Electrical Engineering, Stanford University  
EE371 – Advanced VLSI Circuits (Spr 01-02, Spr 02-03), EE313 – Digital MOS Integrated Circuit Design (Win 01-02), EE271 – Introduction to VLSI Systems (Fall 01-02)

### Industry

8/05 – 11/05 *Advanced Design Intern* – Intel Corp., Hillsboro, OR  
Developed and designed a compact, reference-free on-chip jitter measurement circuit and integrated it along with a supply noise measurement system into a 45nm test-chip. Explored, architected, and designed circuit components for a power-efficient, high-PSRR, self-calibrating digital PLL. Guided optimization and debug of on-die VRMs for PLL power supply generation.

3/05 – 8/05 *Analog Design Co-Op Engineer* – Advanced Micro Devices, Sunnyvale, CA  
Designed an integrated push-pull regulator for simultaneous reduction of digital logic supply noise and improved energy efficiency. Built characterization structures and connected the regulator (along with on-chip supply noise monitors) to the global supply of a K8 test vehicle in 65nm SOI. Designed low voltage, supply-independent distributed thermal sensing circuits for adaptive power and thermal control, and guided feasibility studies for a multi-standard 1-5+ Gb/s receiver.

- 4/03 – 3/05 **Visiting Researcher** – Rambus Inc., Los Altos, CA  
Investigated architectures, communications techniques, signaling schemes, and circuits for power-efficient, parallel high-speed links. Designed clock generation circuits (duty cycle-corrector, phase interpolator, PLL regulator) for a 6.4 Gb/s/link, 12-byte parallel interface on a first generation CELL processor in 90nm SOI. Implemented on-chip power supply noise measurement systems on several test chips. Involved in multi-tone link architecture and circuit explorations, adaptive equalization, backchannel circuits and signaling schemes, and on-die calibration circuits.
- 8/03, 8/04 **Visiting Researcher** – Hewlett Packard, Fort Collins, CO  
Integrated a power supply noise measurement circuit into a 90nm Itanium processor, and utilized the circuit to characterize noise on the digital and analog supplies.
- 6/02 – 9/02 **Exploratory VLSI Design Intern** – IBM Research, Austin, TX  
Designed a test-chip to demonstrate closed-loop control of supply and threshold voltages for minimum power consumption at a fixed operating frequency. Created a logic circuit style to allow direct, dynamic control of transistor threshold.
- 6/01 – 9/01 **Circuit Design Intern** – Rambus Inc., Los Altos, CA  
Architected and designed a fully digital and synthesizable DLL with infinite phase generation and a quadrature output generator.

## PUBLICATIONS

- E. Alon and M. Horowitz, “Integrated Regulation for Energy-Efficient Digital Circuits,” *IEEE Journal of Solid-State Circuits*, Aug. 2008.
- M. Horowitz, D. Stark, and E. Alon, “Digital Circuit Design Trends,” *IEEE Journal of Solid-State Circuits*, Apr. 2008.
- E. Alon and M. Horowitz, “Integrated Regulation for Energy-Efficient Digital Circuits,” *IEEE Custom Integrated Circuits Conference*, Sept. 2007.
- E. Alon, J. Kim, S. Pamarti, K. Chang, and M. Horowitz, “Replica Compensated Linear Regulators for Supply-Regulated Phase-Locked Loops,” *IEEE Journal of Solid-State Circuits*, Feb. 2006.
- S. Naffziger, B. Stackhouse, T. Grutkowski, D. Josephson, J. Desai, E. Alon, and M. Horowitz, “The Implementation of a 2-core, Multi-Threaded Itanium Family Processor,” *IEEE Journal of Solid-State Circuits*, Jan. 2006.
- M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, “Scaling, Power, and the Future of CMOS,” *IEEE International Electron Devices Meeting*, Dec. 2005.
- C. Werner, C. Høyer, A. Ho, M. Jeeradit, F. Chen, B. Garlepp, W. Stonecypher, S. Li, A. Bansal, A. Agarwal, E. Alon, V. Stojanović, and J. Zerbe, “Modeling, Simulation, and Design of a Multi-Mode 2-10 Gb/sec Fully Adaptive Serial Link System,” *IEEE Custom Integrated Circuits Conference*, Sept. 2005.
- V. Abramzon, E. Alon, B. Nezamfar, and M. Horowitz, “Scalable Circuits for Supply Noise Measurement,” *IEEE European Solid-State Circuits Conference*, Sept. 2005.
- E. Alon, V. Stojanović, and M. A. Horowitz, “Circuits and Techniques for High-Resolution Measurement of On-Chip Power Supply Noise,” *IEEE Journal of Solid-State Circuits*, April 2005.
- V. Stojanović, A. Ho, B. Garlepp, F. Chen, J. Wei, G. Tsang, E. Alon, R. Kollipara, C. Werner, J. Zerbe, and M. A. Horowitz, “Autonomous Dual-Mode (PAM2/4) Serial Link Transceiver with Adaptive Equalization and Data Recovery,” *IEEE Journal of Solid-State Circuits*, April 2005.
- K. Chang, S. Pamarti, K. Kaviani, E. Alon, X. Shi, T. Shin, J. Shen, G. Yip, C. Madden, R. Schmitt, C. Yuan, F. Assaderaghi, and M. Horowitz, “Clocking and Circuit Design for a Parallel I/O on a First Generation CELL Processor,” *IEEE International Solid-State Circuits Conference*, Feb. 2005.
- K. Mai, R. Ho, E. Alon, D. Liu, Y. Kim, D. Patil, and M. Horowitz, “Architecture and Circuit Techniques for a 1.1GHz 16Kb Reconfigurable Memory in 0.18 $\mu$ m CMOS,” *IEEE Journal of Solid-State Circuits*, Jan. 2005.
- E. Alon, V. Stojanović, J. M. Kahn, S. Boyd, and M. Horowitz, “Equalization of Modal Dispersion in Multimode Fiber Using Spatial Light Modulators,” *IEEE Global Telecommunications Conference*, Nov. 2004.

E. Alon, V. Stojanović, and M. Horowitz, "Circuits and Techniques for High-Resolution Measurement of On-chip Power Supply Noise," *IEEE Symposium on VLSI Circuits*, June 2004.

V. Stojanović, A. Ho, B. Garlepp, F. Chen, J. Wei, E. Alon, C. Werner, J. Zerbe, and M. A. Horowitz, "Adaptive Equalization and Data Recovery in a Dual-Mode (PAM2/4) Serial Link Transceiver," *IEEE Symposium on VLSI Circuits*, June 2004.

A. Ho, V. Stojanović, F. Chen, C. Werner, G. Tsang, E. Alon, R. Kollipara, J. Zerbe, and M. A. Horowitz, "Common-mode Backchannel Signaling System for Differential High-speed Links," *IEEE Symposium on VLSI Circuits*, June 2004.

K. Mai, R. Ho, E. Alon, D. Liu, Y. Kim, D. Patil, and M. Horowitz, "Architecture and Circuit Techniques for a Reconfigurable Memory Block," *IEEE International Solid-State Circuits Conference*, Feb. 2004.

## **PATENTS**

S. Pamarti and E. Alon, "Transmitter with Skew Reduction," application published Jun. 2007.

S. Pamarti and E. Alon, "Four-Wire Signaling System," application published Jun. 2007.

E. Alon, V. Stojanović, A. Amirkhany, "Digital Transmitter with Data Stream Transformation Circuitry," application published Dec. 2006.

M. A. Horowitz, E. Alon, V. Stojanović, J. M. Kahn, "Adaptive Control for Mitigating Interference in a Multimode Transmission Medium," issued Mar. 2007.

A. Amirkhany, V. Stojanović, E. Alon, J. L. Zerbe, M. A. Horowitz, "Linear Transformation Circuits," issued Nov. 2006.

E. Alon, S. Pamarti, F. Assaderaghi, K. Chang, "Simultaneous Bi-Directional Link," application published Jun. 2006.

E. Alon, B. Garlepp, V. Stojanović, A. Ho, F. Chen, "Circuit Calibration System and Method," issued Oct. 2006.

A. Ho, V. Stojanović, F. Chen, E. Alon, M. Horowitz, "Noise-tolerant signaling schemes supporting simplified timing and data recovery," issued Nov. 2007.

V. Stojanović, A. Ho, A. Bessios, F. Chen, E. Alon, M. A. Horowitz, "High speed signaling system with adaptive transmit pre-emphasis and reflection cancellation," issued Apr. 2006.

E. Alon, J. L. Burns, K. J. Nowka, R. M. Rao, "Technique for mitigating gate leakage during a sleep state," issued Sept. 2004.

E. Alon and S. Best, "Apparatus and method for a digital delay locked loop," issued Nov. 2003.