Synthesis of Higher Dimensional Chua Circuits

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Abstract— **In this paper, we present a universal method to design n-dimensional piecewise linear circuits. These circuits are described by a system of differential equation associated with a piecewise linear continuous vector-field in the n-dimensional state-space, which consists of two different linear regions. The circuits contain only two-terminal elements, one piecewise linear resistor and a number of linear resistors capacitors and inductors. The developed method leads to a variety of structures. It is possible to design n-dimensional canonical circuits containing a minimum number of inductors as well as inductor-free circuits. A surprising result is the transformation of the 3-D Chua circuit [2] into an inductor-free circuit that exhibits the double scroll as well. We compare our results with the recently published method of Kocarev [1]. Using our approach, a theorem that specifies the restriction of eigenvalue patterns associated with a piecewise linear vector-field having at least two equilibrium points can be proved.**

I. Introduction

THE INVESTIGATION of nonlinear autonomous dynamic systems which can exhibit a large variety of behaviour was strongly forced in the past. One direction of efforts is the design of physical systems generating chaotic motion in the state space. For this purpose especially electrical circuits are easy to handle. Under certain conditions we can realize a piecewise linear continuous vector-field with such circuits and study any possible behaviour experimentally. From this point of view one goal is to design a circuit capable of realizing every member of the higher dimensional Chua circuit family [2]. One 3-D canonical Chua circuit is given in [3]. Furthermore, one extension to higher dimensional canonical circuits is published by Kocarev [1]. Both represent an analysis of a given structure in the time domain and made sure that the structure is canonical. Here we choose a synthesis approach in the frequency domain which is capable of generating a whole class of structures containing both ones mentioned above. With this method, we design as examples a canonical as well as a noncanonical n-dimensional piecewise linear circuit. Canonical in our sense means

1) canonical with respect to the behavior i.e., capable of realizing all possible behaviour of the associated vector-field. We will call it canonical in behavior
2) canonical with respect to the number of circuit elements i.e., containing the minimum number of elements necessary. We will call it canonical in structure.

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II. Network-Design-Algorithm for the n-Dimensional Piecewise Linear Circuit

A. General Approach

We choose an electrical network consisting of a nonlinear static two-terminal element connected to a linear two-terminal dynamic network. Consider the class $L(n, 2)$ of n-dimensional two-region continuous piecewise linear vector-fields and the class $C(n, 3)$ of n-dimensional symmetric with respect to the origin three-region continuous piecewise linear vector-fields defined in [1]. One realization of this class of vector-fields is shown in principle in Fig. 1. This system consists of either a two-segment static resistor as a member of $L(n, 2)$ or a three-segment symmetric (with respect to the origin) static resistor as a member of $C(n, 3)$ and a n-dimensional two-terminal linear network. The common feature of both classes is the existence of two different linear regions. Now we increase the number of segments to k retaining the feature of then two different linear regions. Let us call this more common class $L(n, k/m)$. N represents the dimension, k the region and m the number of the different regions. Consider now a $L(n, k/2)$ and a subset $C(n, k/2)$ that represents a vector-field symmetric (with respect to the origin). Subsequently the vector-field of $L(n, k/2)$ or $C(n, k/2)$ shall be represented by the eigenvalues of the linear systems of differential equations in the two different regions. Assuming that the eigenvalues in each region are given, a circuit that realizes all possible patterns of $2n$ eigenvalues has to be designed. This circuit will be canonical in behaviour. First, we have to decide on the minimum number of element parameters needed for a circuit that is canonical in structure. It is pointed out in [1] and [3] that at least $2 \cdot n + 1$ parameters are needed to generate any set of $2 \cdot n$ eigenvalues because of the impedance scaling property of linear systems [3]. This impedance scaling deals with normalized parameters: Z_n/α for impedances and $Y_n \cdot \alpha$ for admittances with the scaling factor α.

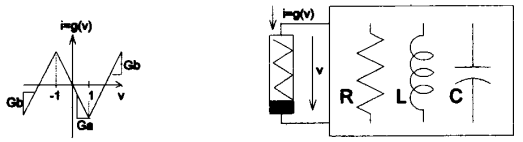
B. Coefficients of the Characteristic Polynomials

The state equations of an autonomous piecewise linear network are given by

$$\frac{d\vec{z}}{dt} = \begin{cases} A_0 \cdot \vec{z}, & \vec{z} \in D_0 \\ A_1 \cdot \vec{z}, & \vec{z} \in D_1 \end{cases}, \tag{1}$$

where D_0 an D_1 denote the two different regions.

The eigenvalues of these systems of homogeneous differential equations are determined by $\det(A_i - sI) = 0$, $i = 0, 1$, where I is the unity matrix.



(a) (b)

Fig. 1. One v-i-characteristic of the nonlinear transistor; (b) general structure of the unknown circuit.

This leads to the characteristic polynomial

$$P(s) = s^n + \sum_{i=0}^{n-1} d_i \cdot s^i = 0. \tag{2}$$

According to [3] we denote the coefficients for regions D_0 and D_1 by

$$d_i = \begin{Bmatrix} p_i, & \vec{z} \in D_0 \\ q_i, & \vec{z} \in_1 \end{Bmatrix} \tag{3}$$

Usually the eigenvalues of a given system are calculated from (2). Here we have the inverse problem to calculate the coefficients (3) from the given eigenvalues in each region. This can be done using Vieta's formulas [5]:

$$\begin{array}{ll} p_{n-1} = \sum_{i=1}^{n} \mu_i & q_{n-1} = \sum_{i=1}^{n} \nu_i \\ -p_{n-2} = \sum_{i,j=1}^{n} \mu_i\mu_j & -q_{n-2} = \sum_{i,j=1}^{n} \nu_i\nu_j \\ p_{n-3} = \sum_{\substack{i,j,k=1 \\ (i<j<k)}}^{n} \mu_i\mu_j\mu_k & q_{n-3} = \sum_{\substack{i,j,k=1 \\ (i<j<k)}}^{n} \nu_i\nu_j\nu_k \\ \cdots & \cdots \\ (-1)^n p_1 = \prod_{i=1}^{n} \mu_i & (-1)^n q_1 = \prod_{i=1}^{n} \nu_i \end{array} \tag{4}$$

where μ_i and $\nu_i (i = 1, \ldots, n)$ are the eigenvalues in D_0 and D_1 respectively.

C. Network Function

Our goal is to determine the structure of the two-terminal linear network and to calculate all parameters of the circuit shown in Fig. 1(b). By simply applying Kirchhoff's voltage law to the circuit in the complex domain we obtain

$$Y(s) + G_a = 0 \text{ in region } D_0 \text{ and} \tag{5}$$

$$Y(s) + G_b = 0 \text{ in region } D_1. \tag{6}$$

where G_a and G_b denote the small-signal conductance corresponding to the slope of the v-i-characteristics of the piecewise linear two-terminal element and s is the complex frequency $s = \sigma + j\omega$. Assuming the complex admittance function of the linear network to be

$$Y(s) = K * \frac{s^n + b_{n-1} * s^{n-1} + b_{n-2} * s^{n-2} + \cdots + b_1 * s + b_0}{s^m + a_{m-1} * s^{m-1} + a_{m-2} * s^{m-2} + \cdots + a_1 * s + a_0} \tag{7}$$

we obtain by substituting (7) into (6) and (5)

$$G_a + K * \frac{s^n + b_{n-1} * s^{n-1} + b_{n-2} * s^{n-2} + \cdots + b_1 * s + b_0}{s^m + a_{m-1} * s^{m-1} + a_{m-2} * s^{m-2} + \cdots + a_1 * s + a_0} = 0 \quad \text{for} \vec{z} \in D_0 \tag{8}$$

and

$$G_b + K * \frac{s^n + b_{n-1} * s^{n-1} + b_{n-2} * s^{n-2} + \cdots + b_1 * s + b_0}{s^m + a_{m-1} * s^{m-1} + a_{m-2} * s^{m-2} + \cdots + a_1 * s + a_0} = 0 \quad \text{for } \vec{z} \in D_1. \tag{9}$$

If the circuit in Fig. 1(b) has to realize the state equation (1), (8) and (9) have to correspond to the characteristic polynomials ((2), with respect to (3)). This will be achieved by comparising the coefficients of both groups of equations.

D. Design Algorithm

The algorithm to design a network which realizes the given sets of eigenvalues will consist of the following two steps:

Step one: Determine the coefficients $(b_{0\cdots n-1}, a_{0\cdots m-1})$ of the polynomial of the two-terminal function, and also the parameters G_a and G_b by comparing it with the characteristic polynomial resulting from the given set of eigenvalues.

Step two: Design the network which realizes the two-terminal function.

Note that we use admittance functions in developing our algorithm. Using impedance functions is also possible and leads to the dual network, as will be shown at the end of this chapter.

To carry out the first step we have to convert (8) and (9) into the form of the characteristic equation (2) for comparison. Multiplying (8) and (9) with the denominator polynomial we obtain:

$$G_a \cdot \left(s^m + \sum_{i=0}^{m-1} a_i s^i \right) + K \cdot \left(s^n + \sum_{i=0}^{n-1} b_i s^i \right) = 0 \tag{10}$$

$$G_b \cdot \left(s^m + \sum_{i=0}^{m-1} a_i s^i \right) + K \cdot \left(s^n + \sum_{i=0}^{n-1} b_i s^i \right) = 0 \tag{11}$$

First decide how the order of the denominator and numerator polynomials has to be chosen. Since the order of the denominator and numerator of a two-terminal network-function can only differ by 1 at maximum, we have three possible cases:

Case 1) $n = m$ (12)

Case 2) $n = m - 1$ (13)

Case 3) $n = m + 1$ (14)

In the following we choose the Case 3, for this is the only one, which does not include restrictions to the choice of the component values (especially G_a, G_b and K) of the circuit and hence can lead to a canonical structure. Then, (10) and (11) can be written in the form

$$s^n + \left(b_{n-1} + \frac{G_a}{K} \right) s^{n-1} + \sum_{i=0}^{n-2} \left(b_i + \frac{G_a}{K} \cdot a_i \right) s^i = 0 \tag{15}$$

TABLE I

Approach: $P(s) = G_{a/b} \cdot (s^m + a_{m-1} \cdot s^{m-1} + \cdots + a_1 \cdot s + a_0) + K \cdot (s^n + b_{n-1} \cdot s^{n-1} + \cdots + b_1 \cdot s + b_0)$
$= s^n + d_{n-1} \cdot s^{n-1} + \cdots d_1 \cdot s + d_0 = 0 \quad d_i = p_i(\text{resp.}q_i),\ \vec{z} \in D_0(\text{resp.}D_1)$

System of equations:

$$\left(b_{n-1} + \frac{G_a}{K}\right) = p_{n-1} \tag{17}$$

$$\left(b_{n-1} + \frac{G_b}{K}\right) = q_{n-1} \tag{18}$$

$$\left(b_i + \frac{G_a}{K} \cdot a_i\right) = p_i \qquad \text{for } i = 0, 1, \cdots, n-2 \tag{19}$$

$$\left(b_i + \frac{G_b}{K} \cdot a_i\right) = q_i \qquad \text{for } i = 0, 1, \cdots, n-2 \tag{20}$$

First additional equation:

First step of polynomial division: Separate a capacitor and select its value: $Y(s) = Ks + Y_{r1}(s)$ (21)

$$K = C_1 = 1 \tag{22}$$

Second additional equation: Two alternative possibilities:

First possibility:

Separate a parallel conductance and set it to zero:

$$Y(s) = s + (b_{n-1} - a_{n-2}) + Y_{r2}(s)$$

The obtained second equation is:

$$(b_{n-1} - a_{n-2}) = 0 \tag{23}$$

(for examples, see Section III)

Second possiblity:

Avoid separating a conductance parallel to the capacitor

C_1 (for examples see Sections IV and V)

Look for an equation obliterating an arbitrary circuit element thus obtaining a circuit canonical in structure

Choose a condition for one of the coefficients of the numerator polynomial b_i or one of the parameters G_a or G_b arbitrarily

Calculate the coefficients of the denominator polynomial:

$$a_i = \frac{(p_i - q_i)}{(p_{n-1} - q_{n-1})} \text{ for } i = 0, 1, \cdots, n-2 \tag{26}$$

One obtains the restriction: $p_{n-1} \neq q_{n-1}$

Calculate the remaining coefficients and parameters of the nonlinear resistor using the equations derived above and (17)–(20) and (22).

Carry out the second step completely, realizing $y_{r1}(s)$ or $Y_{r2}(s)$ by one of the well-known methods of network theory considering the above condition.

$$s^n + \left(b_{n-1} + \frac{G_b}{K}\right)s^{n-1} + \sum_{i=0}^{n-2}\left(b_i + \frac{G_b}{K} \cdot a_i\right) = 0 \tag{16}$$

Comparing the coefficients of (15) and (16) with those of the characteristic polynomial (2) Table I, we obtain the system of (17)–(20) shown in Table I.

These are $2 \cdot n$ equations for the $2 \cdot n + 2$ unknown values $a_i (i = 0, \cdots, n-2)$, $b_i (i = 0, \cdots, n-1)$, G_a, G_b and K. Hence to clearly determine all unknown values, two additional equations are required. The definition of them allows to introduce additional conditions concerning the desired form of the network. To get the first additional equation we carry out the first step of polynomial division in (7) thus separating a parallel capacitor to be the first network element seen from the input (see (21) in Table I). C_1 is the normalized value of the parallel capacitor. Since one circuit element parameter can be chosen arbitrarily because of the impedance scaling property, we set it for convenience and simplicity as in (22) in Table I. There are different ways to determine the second additional equation (for instance (23) in Table I). Two of these possibilities are shown in the table below. If all necessary $2n + 2$ equations are determined, the unknown values can be calculated as follows: Subtracting (18) from (17) and (20) from (19) gives

$$(p_{n-1} - q_{n-1}) = \frac{(G_a - G_b)}{K} \tag{24}$$

$$(p_i - q_i) = \frac{(G_a - G_b)}{K} \cdot a_i \qquad \text{for } i = 0, 1, \cdots, n-2 \tag{25}$$

Substituting (24) into (25) we obtain all $a_i (i = 0, 1, \cdots, n-2)$ in (26) in Table I.

The kind of the structure we will obtain depends on the chosen way shown in Table I.

Note that there is the restriction

$$p_{n-1} \neq q_{n-1} \tag{27}$$

which also arises in [1] and [3]. However $p_{n-1} \neq q_{n-1}$ is a singular situation and can be eliminated by perturbing one of

the eigenvalues without substantially changing the behaviour of the system [3].

We give examples of both proposed ways in Sections III and IV.

Closing this chapter we mention that there exists a dual network to every circuit realization outlined above. Then, instead of (8) and (9), we have

$$R_{a/b} + Z(s) = R_{a/b} + K * \frac{s^n + b_{n-1} * s^{n-1} + b_{n-2} * s^{n-2} + \cdots + b_1 * s + b_0}{s^m + a_{m-1} * s^{m-1} + a_{m-2} * s^{m-2} + \cdots + n_1 * a_0} = 0 \tag{28}$$

where $R_{a/b}$ denotes the slope of the i-v-characteristic of the piecewise linear one-port.

III. Synthesis of Canonical Chua Circuits

In this chapter we take the first possibility in Table I. First we determine the coefficients and the parameters of the non-linearity. Substituting (26) for $i = n - 2$ into (23):

$$b_{n-1} = a_{n-2} = \frac{(p_{n-2} - q_{n-2})}{(p_{n-1} - q_{n-1})} \tag{29}$$

Now we can calculate the parameters of the non-linearity and all remaining coefficients b_i:

$$G_a = p_{n-1} \frac{(p_{n-2} - q_{n-2})}{(p_{n-1} - q_{n-1})} \tag{30}$$

$$G_b = q_{n-1} \frac{(p_{n-2} - q_{n-2})}{(p_{n-1} - q_{n-1})} \tag{31}$$

$$b_i = p_i - G_a \cdot a_i$$

$$b_i = p_i - \left(p_{n-1} \frac{(p_{n-2} - q_{n-2})}{(p_{n-1} - q_{n-1})} \right) \cdot \left(\frac{(p_i - q_i)}{(p_{n-1} - q_{n-1})} \right) \quad i = 0 \cdots n-2. \tag{32}$$

Now all needed coefficients of $Y(s)$ are calculated. Next, we carry out the second point i.e., we determine the structure of $Y_{r1}(s)$. Different ways are possible. Our current goal is to design a canonical n-dimensional Chua circuit. The easiest way to achieve this is using the method of continued polynomial division. One example structure and its dual network is shown in Fig. 2. The associated equation is:

$$G_{a/b} + C1 \cdot s + \cfrac{1}{L2 \cdot s + R2 + \cfrac{1}{C_3 \cdot s + G3 + \cfrac{1}{L4 \cdot s + R4 + \cfrac{1}{\cdots + \cfrac{1}{Kn \cdot s + Hn}}}}} = 0 \tag{33}$$

where for even n: $Hn = Rn$ and $Kn = Ln$ and for odd n: $Hn = Gn$ and $Kn = Cn$. It is the same structure as chosen by Kocarev in [1]. Another structure containing only one single inductor can be synthesized in the following way: Instead

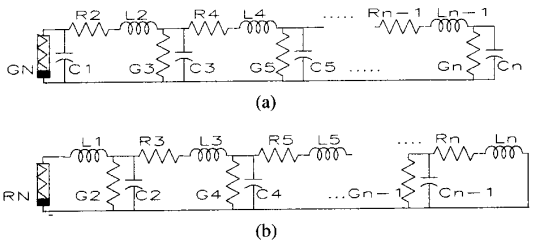


Fig. 2. (a) Structure of the n-dimensional canonical circuit for odd n; (b) corresponding dual network.

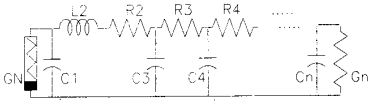


Fig. 3. Structure of the n-dimensional "inductor poor" canonical circuit.

of calculating the conductance G3 in (33) we calculate a resistance of the reciprocal term having separated the capacitor C3 before, etc. The corresponding equation is

$$G_{a/b} + C1 \cdot s + \cfrac{1}{L2 \cdot s + R2 + \cfrac{1}{C3 \cdot s + \cfrac{1}{R3 + \cfrac{1}{\cdots + \cfrac{1}{Cn \cdot s + Gn}}}}} = 0 \tag{34}$$

The structure is shown in Fig. 3.

Obviously, there exist further canonical realizations of Chua circuit containing w inductors, where w is a number with:

$$1 \le w \le \frac{n}{2} \quad \text{for even } n \tag{35}$$

$$1 \le w \le \frac{n-1}{2} \quad \text{for odd } n. \tag{36}$$

IV. Synthesis of an Inductor Free Canonical Chua Circuit

Now we follow the second possibility in Table I. We use our method to design an inductor-free circuit. Inductors can be avoided by a modification of the polynomial division. Instead of calculating a conductance after separating a capacitor we calculate a resistance from the reciprocal term. Assuming that we can completely determine the two-terminal function $Y(s)$ by adding any second equation additional to (17)–(20) and (22) we obtain the continued fraction:

$$Y(s) = C1 \cdot s + \cfrac{1}{R1 + \cfrac{1}{C2 \cdot s \cfrac{1}{R2 + \cfrac{1}{\cdots + \cfrac{1}{Cn \cdot s + Gn}}}}}. \tag{37}$$

Fig. 4 shows the corresponding structure of a RC ladder network. Next we propose an idea to find the necessary second equation. The n-dimensional polynomial representing the linear two-terminal network contains $2 \cdot n$ coefficients ($b_{0 \cdots n-1}$, $a_{0 \cdots n-2}$ and K). This leads to $2 \cdot n$ circuit elements. Therefore our circuit has $2 \cdot n + 2$ parameters ($C_{1 \cdots n}$, $R_{1 \cdots n}$, G_a, G_b). In order to find the second additional equation, we use

Theorem 1: Let G_n denote the last conductor at the end of the n-dimensional RC-ladder network. Then the following equivalence is valid: $G_n = 0$ if and only if $b_0 = 0$.

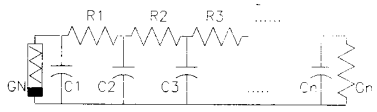


Fig. 4. Structure of the n-dimensional inductor free circuit.

Fig. 5. (a) Chua's 3-D circuit; (b) associated RC-ladder obtained by transforming Chua's circuit.

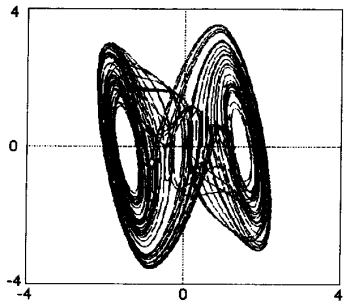


Fig. 6. Double scroll produced by the RC-ladder network. (Projection onto the (V_{C1}, V_{C2}) – plane).

Proof: See Appendix I.

This allows us to eliminate the last conductor G_n in the structure of Fig. 4. We choose:

$$b_0 = 0. \tag{38}$$

Therefore, we make the inductor-free circuit canonical in structure because it contains exactly the minimum number of circuit parameters. Using the equations (17)–(20), (22) and (38), we obtain the remaining coefficients:

$$G_a = \frac{p_0}{a_0} = p_0 \cdot \frac{(p_{n-1} - q_{n-1})}{(p_0 - q_0)} \tag{39}$$

$$G_b = \frac{q_0}{a_0} = q_0 \cdot \frac{(p_{n-1} - q_{n1})}{(p_0 - q_0)} \tag{40}$$

$$b_i = p_i - G_a \cdot a_i$$

$$b_i = p_i - \left(p_0 \cdot \frac{(p_0 - q_0)}{(p_{n-1} - q_{n-1})}\right) \cdot \left(\frac{(p_i - q_i)}{p_{n-1} - q_{n-1}}\right) \qquad i = 1 \cdots n-2 \tag{41}$$

$$b_{n-1} = p_{n-1} - G_a = p_{n-1} - p_0 \cdot \frac{(p_{n-1} - q_{n-1})}{(p_0 - q_0)}. \tag{42}$$

Next we determine $C2 \cdots n$, $2 \cdots n$ by polynomial division described above. With this approach we are able to design an inductor free network capable of realizing any desired member of $L(n, k/2)$ and $C(n, k/2)$.

V. Inductor Free Three-Dimensional Chua Circuit

Vector-fields of $C(3, 3/2)$ are either linear conjugate or linear equivalent if they have identical or identical normalized eigenvalue patterns [2]. Circuits which realize those vector-fields will only differ in state or in time and state scale thus having the same behaviour in quality. Since our method is suitable to realize given eigenvalue patterns it can also be used to transform circuits conserving their qualitative behaviour. As an example we choose the well known 3-D Chua circuit first published in [7] shown in Fig. 5(a). We transform the linear network into a RC-ladder network shown in Fig. 5(b). The following algorithm applies:

1) From the Chua circuit (see [7]) we determine the coefficients of the characteristic equations in both regions:

$$p_0 = -18.367 \quad p_1 = 4 \quad p_2 = -2/7 \qquad \text{for } D_0$$
$$q_0 = 36.735 \quad q_1 = 7.857 \quad q_2 = 25/7 \qquad \text{for } D_1$$

2) From this set of coefficients we design a RC-ladder network, following the second possibility in Table I.

   a. Calculating the coefficients of the denominator polynomial yields:

$$a_0 = 14.286$$

   b. Set

$$K = C_1 = 1 \quad b_2 = 0$$

   c. Calculating the remaining coefficients and parameters of the nonlinear resistor using the equation derived above and (17)–(20) and (22) yields:

$$b_0 = -14.285 \quad b_1 = 4.286 \quad G_a = p_2 = -2/7 \quad G_b = q_2 = 25/7$$

   d. Carry out the second point by continued polynomial division avoiding inductors. In order to confirm our results we have simulated the obtained RC-ladder network. The Double Scroll attractor is shown in Fig. 6.

Finally, we emphasize the following theorem:

Theorem 2: It is impossible to transform the 3-D Chua circuit into a RC-ladder network which is canonical in structure.

Proof: See Appendix II.

VI. Necessary Condition for at Last Two Equilibrium Points

For some applications it is important to make sure that a vector-field has two or more equilibrium points i.e. fixed points. The theorem for the 3-D canonical circuit associated with $C(3, 3/2)$ having three equilibrium points is given in [3] and for a special n-dimensional canonical circuit in [1]. Here we prove a theorem that determines the conditions for the existence of equilibrium points in the outer regions (denoted D_{+1} and D_{-1}) for a vector-field of $C(n, 3/2)$. This vector-field can be realized by any n-dimensional circuit following the method in Section II and has always an equilibrium point in the inner region D_0 at the origin.

Theorem 3: A vector field of $C(n, 3/2)$ realized by any n-dimensional circuit only has equilibrium points in the outer regions D_{+1} and D_{-1} if:

(i) The canonical circuit has three dc operating points,

or

(ii) $p_0 \cdot q_0 < 0$ (43)

Proof: (direct):

1) The nonlinear v-i-function of the nonlinear resistor is described in the outer region $D+1$ by the equation (see Fig. 1(a)):

$$i_N = G_b \cdot v + (G_a - G_b) \tag{44}$$

2) Therefore, the DC-Network ($s = 0$) of the whole n-dimensional circuit is described by the equation

$$\frac{i_N}{v_0} = G_b + \frac{(G_a - G_b)}{v_0} + \frac{b_0}{a_0} = 0 \tag{45}$$

where v_0 is the normalized voltage of the assumed equilibrium point. b_0/a_0 represents the dc-conductance of the two-terminal element with capacitors open-circuited and inductors short-circuited.

Solving this equation, v_0 is obtained to be

$$v_0 = \frac{(G_b - G_a)}{G_b + \frac{b_0}{a_0}} \qquad \left(\text{assumed } G_b + \frac{b_0}{a_0} \neq 0\right). \tag{46}$$

The region D_{+1} has exactly one equilibrium point if

$$v_0 > 1 \tag{47}$$

because the break-point is located at $v = 1$.

3) Inserting (46) into (47) we have

$$v_0 = \frac{a_0 \cdot (G_b - G_a)}{a_0 \cdot G_b + b_0} > 1. \tag{48}$$

from which we obtain

$$0 > (a_0 \cdot G_a + b_0) \cdot (a_0 \cdot G_b + b_0) \tag{49}$$

Using (19) and (20) yields

$$0 > p_0 \cdot q_0 \tag{50}$$

Because of symmetry there is an equilibrium point in the region D_{-1}, too, i.e., the theorem is proved. Assuming that the vector-field has an equilibrium point in the original in D_0. Theorem 1 is also valid for the class $L(n, 2/2)$.

VII. Conclusion

In this paper we have discussed a method to synthesize piecewise linear networks with given eigenvalues in each linear region in the state space. We derived a simple algorithm consisting of the following two steps:

1) Calculation of the coefficients of the characteristic polynomial in linear region
2) determination of the admittance or impedance network function corresponding to the characteristic polynomial and the realization of the network by continued fraction expansion.

Because of some degree of freedom additional conditions concerning the desired form of the network can be introduced into the synthesis procedure thus providing the possibility of synthesizing inductor free or networks canonical in structure. The proposed method will be important for practical design of nonlinear system which are to generate chaotic signals as electronic integrated circuits. We have demonstrated several variants of Chua circuits by synthesizing including an inductor free version of the original three dimensional Chua circuit. This result which is surprising to some extent was confirmed by direct simulation of the resulting network showing the typical Double Scroll behaviour. Now for example the Chua circuit can be easily realized by an electronic circuit containing no inductive elements. The proposed method allows also to prove a theorem about the existence of equilibrium points in a piecewise linear vector-field. This theorem is a generalized of the three dimensional case in [3] and of the particular n-dimensional case in [1].

Appendix I
Inductive Proof of Theorem 1

1) The theorem applies for $n = 1$:

$$Y(s) = K \cdot (s + b_0) = C_1 \cdot s + G_1 \tag{A1.1}$$

$$G_1 = K \cdot b_0 \tag{A1.2}$$

$$b_0 = 0 \Leftrightarrow G_1 = 0 \tag{A1.3}$$

2) Assuming that the theorem is valid for n, i.e., for the admittance function

$$Y(s) = K \cdot \frac{s^n + \sum_{i=1}^{n-1} b_i \cdot s^i + b_0}{s^{n-1} + \sum_{i=0}^{n-2} a_i \cdot s^i} \tag{A1.4}$$

$$b_0 \Leftrightarrow G_n = 0 \tag{A1.5}$$

is valid.

3) We prove the validity for $n + 1$: Performing a two-step polynomial division, we get

$$\begin{aligned} Y(s) &= K \cdot \frac{s^{n+1} + \sum_{i=1}^{n} b_i \cdot s^i + b_0}{s^n + \sum_{i=0}^{n-1} a_i \cdot s^i} \\ &= K \cdot s + \frac{K}{\frac{s^n + \sum_{i=0}^{n-1} a_i \cdot s^i}{\sum_{i=4}^{n} (b_i - a_{i-1}) \cdot s^i + b_0}} = K \cdot s \\ &\quad + \frac{K}{\frac{1}{(b_n - a_{n-1})} + \frac{1}{\frac{\sum_{i=1}^{n} (b_i - a_{i-1}) \cdot s^i + b_0}{\sum_{i=1}^{n-1} \left(a_i \frac{(b_i - a_{i-1})}{(b_n - a_{n-1})}\right) \cdot s^i + \left(a_0 - \frac{b_0}{(b_n - a_{n-1})}\right)}}} \end{aligned} \tag{A1.6}$$

$$b_0 = 0 \Leftrightarrow G_{n+1} = 0 \tag{A1.7}$$

The denominator of the last fraction in (A1.6) has the form of (A1.4). Thus, if the equivalence (A1.5) is valid for n then it is also valid for $n + 1$. This proves the theorem.

APPENDIX II
INDIRECT PROOF OF THEOREM 2

We show that the method of Section IV leads to a singular network.

Consider the characteristic equation belonging to the normalized differential equations of Chua circuit [2] and the special coefficients p_i and q_i in it:

$$s^3 + (1 + \alpha \cdot c) \cdot s^2 + (\alpha(c-1) + \beta) \cdot s + \alpha \cdot \beta \cdot c = 0$$

$$c = \begin{Bmatrix} c_0 & \vec{z} \in D_0 \\ c_{\pm 1} & \vec{z} \in D_{\pm 1} \end{Bmatrix} \tag{A2.1}$$

Assumption: The transformation is possible.

Using (22), (26) and (38)–(42), we obtain the coefficients

$$a_1 = \frac{p_1 - q_1}{p_2 - q_2} = \frac{\alpha \cdot (c_0 - c_{\pm 1})}{\alpha \cdot (c_0 - c_{\pm 1})} = 1 \tag{A2.2}$$

$$b_0 = 0 \tag{A2.3}$$

$$G_a = \frac{p_0}{a_0} = p_0 \cdot \frac{p_2 - q_2}{p_1 - q_1} \tag{A2.4}$$

$$b_2 = p_2 - G_a \cdot p_0 = \frac{p_0 \cdot q_2 - p_2 \cdot q_0}{p_0 - q_0}$$
$$= \frac{\alpha \cdot \beta \cdot c_0 \cdot (1 + \alpha \cdot c_1) - \alpha_n \cdot \beta \cdot c_1 \cdot (1 + \alpha \cdot c_0)}{\alpha \cdot \beta \cdot (c_0 - c_1)} = 1. \tag{A2.5}$$

Now, having all coefficients, we determine the network parameters performing polynomial division:

$$\frac{s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0}{s^2 + a_1 \cdot s + a_0} = s + \frac{1}{\frac{1}{(b_2 - a_1)} + Z_r(s)}. \tag{A2.6}$$

From (A2.2) and (A2.5) we get:

$$(b_2 - a_1) = 0. \tag{A2.7}$$

Comparing (A2.6) with (37) yields:

$$R_1 \to \infty. \tag{A2.8}$$

Thus the effective part of the network will consist only of C_1. An infinite series resistor R_1 isolates it from the remaining part. Thus, the assumption is false, and the theorem holds.

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