

# An IC Chip of Chua's Circuit

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**Abstract**—This paper reports a working microelectronic chip implementation of Chua's circuit. This chip has been designed and fabricated by using a  $2\ \mu\text{m}$  CMOS technology, with the circuit itself occupying a silicon area of  $2.5\text{mm} \times 2.8\text{mm}$ . The chip needs to be powered with a single 9V battery, is autonomous, and generates chaotic signals from the three state variables of Chua's circuit. The proper operation of this chip has been confirmed by experimental reproduction of bifurcation and chaotic phenomena. This microelectronic design of Chua's circuit can be employed as a basic component in the VLSI synthesis of complex circuits making use of chaotic signals, including a class of cellular neural networks and secure communication systems.

## I. INTRODUCTION

**E**LECTRONIC circuits exhibiting well-understood bifurcation and chaotic behavior can be exploited as basic components of emerging classes of complex dynamic electronic networks and systems, including cellular neural networks exhibiting spatially chaotic dynamics and secure communication systems based on chaos synchronization.

Chua's circuit [1]–[9] is the simplest autonomous circuit that can exhibit bifurcation and chaos. It has been studied extensively and is one of the very few circuits in which a formal proof of the existence of chaos has been accomplished [5]. Moreover, the theoretical and simulated behavior of this circuit can be accurately reproduced experimentally. These factors have made Chua's circuit a tool for studying and generating chaos, and is being used as a building block for developing other, more complex circuits exploiting chaotic and bifurcation phenomena [10], [11].

Several physical implementations of the circuit have been proposed since 1985 [6]–[8]. They use discrete components to implement the linear elements and a combination of op amps, resistors, diodes, or discrete bipolar transistors to implement the nonlinear element (Chua's diode). Recently, monolithic CMOS implementations of the Chua's diode [2] and the Chua's circuit [1] have been fabricated.

In this paper, we report the experimental results and the implementation details of a microelectronic chip of Chua's circuit. The linear resistor  $R$  is the only element implemented externally, by a potentiometer, to allow the setting of a bifurcation parameter. This chip has been designed and fabricated by using a  $2\ \mu\text{m}$  double-metal double-poly CMOS technology [15]. The three linear storage elements are implemented with double-poly capacitors, with one of them used to emulate the

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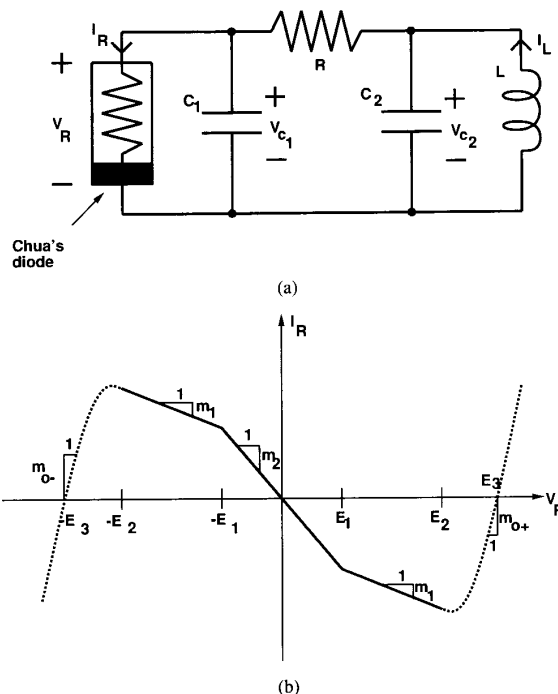


Fig. 1. (a) Chua's Circuit. (b) Driving-point characteristic of Chua's Diode.

TABLE I  
PARAMETERS OF THE CHIP

Parameter	Value	Unit
$C_1$	150	$\text{pF}$
$C_2$	2000	$\text{pF}$
$L$	0.33	$\text{mH}$
$R$	1750	$\Omega$
$m_1$	-0.41	$\text{mA/V}$
$m_2$	-0.78	$\text{mA/V}$
$E_1$	0.7	$\text{V}$

inductor [13]. The resonant frequency of the active LC circuit is approximately 160 KHz. This 8-pin, autonomous chip is powered by a single 9V bias battery, and generates three output signals representing the state variables of Chua's circuit.

The outline of this paper is as follows. Section II gives the chip's electrical specifications and its experimental performance. It shows the three projections of the experimental double-scroll Chua's attractor and the experimental bifurcation sequences obtained by modifying two independent parameters. Section III gives the internal structure of the chip and detail the design procedure for a CMOS technology. Section IV presents

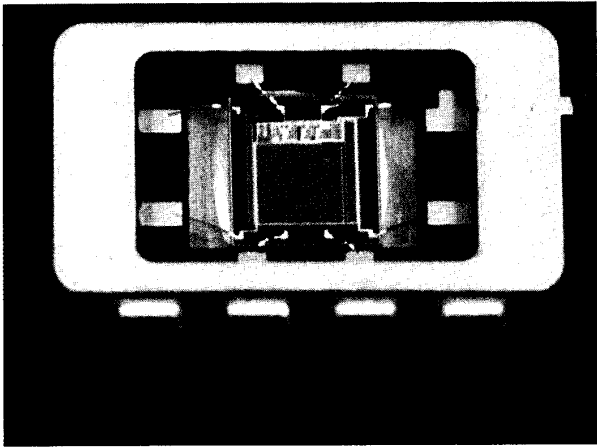


Fig. 2. Photograph of the IC chip.

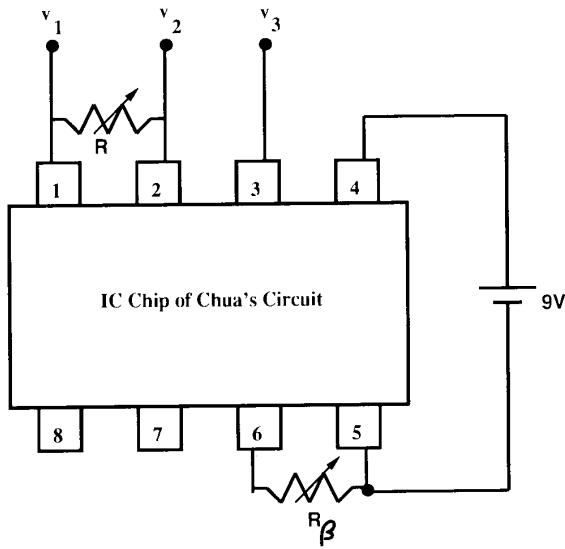


Fig. 3. A typical operating configuration of the chip, with the bias battery, and two external potentiometers to set two bifurcation parameters.

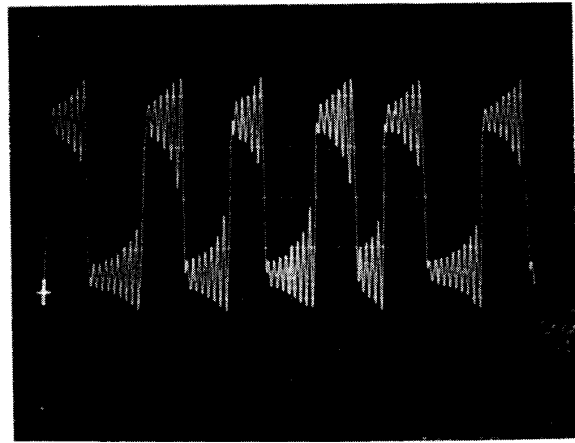
a numerical simulation of the chip. Finally, Section V gives some concluding remarks and applications of the new chip.

II. CHIP SPECIFICATIONS AND EXPERIMENTAL PERFORMANCE

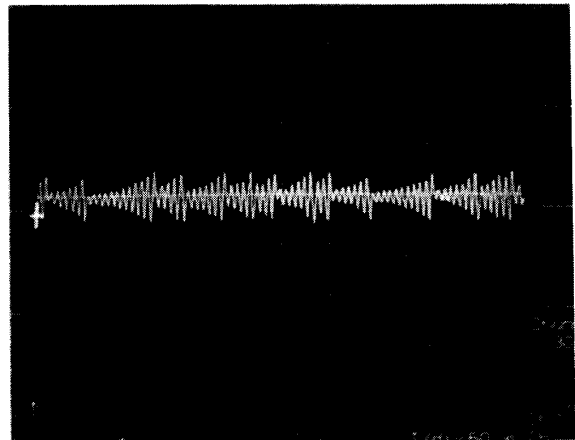
2.1. Parameters of Chua's Circuit Chip

Chua's circuit, shown in Fig. 1, is a third-order circuit. The three variables are the voltages across capacitors  $C_1$  and  $C_2$  and the current through the inductor  $L$ . They are denoted as  $v_{C_1}$ ,  $v_{C_2}$  and  $i_L$ , respectively; and their dynamics are given by:

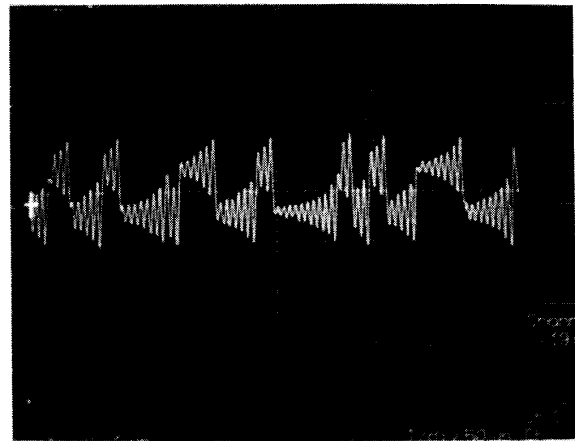
$$\begin{aligned} C_1 \frac{dv_{C_1}}{dt} &= \frac{1}{R}(v_{C_2} - v_{C_1}) - g(v_{C_1}) \\ C_2 \frac{dv_{C_2}}{dt} &= \frac{1}{R}(v_{C_1} - v_{C_2}) + i_L \\ L \frac{di_L}{dt} &= -v_{C_2} \end{aligned} \tag{1}$$



(a)



(b)



(c)

Fig. 4. Experimental time-domain waveforms of the state variables. Vertical scales are 1V/div; horizontal scale is 50μs/div. (a)  $v_1$  versus time. (b)  $v_2$  versus time. (c)  $v_3$  versus time.

where  $g(v_{C_1})$  is the function given in Fig. 1(b). Inside the range  $(-E_2, E_2)$  of  $v_{C_1}$ , in which the circuit normally oper-

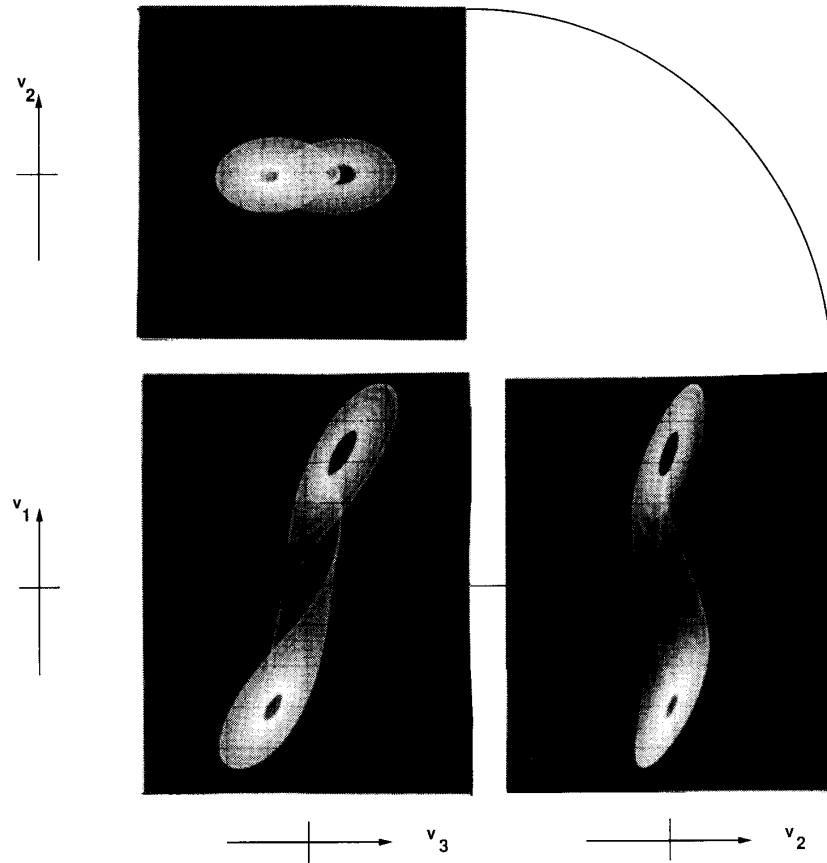


Fig. 5. Experimental Lissajous figures of the double-scroll Chua's attractor. All scales are 500mV/div.

ates, this function is given by:

$$g(v_{C_1}) = m_1 v_{C_1} + \frac{1}{2}(m_2 - m_1)(|v_{C_1} + E_1| - |v_{C_1} - E_1|) \quad (2)$$

A particular Chua's circuit is characterized by seven parameters denoted as  $(C_1, C_2, L, R, E_1, m_1, m_2)$ . They represent, respectively, the parameter values of the two linear capacitors  $C_1$  and  $C_2$ , the linear inductor  $L$ , the linear resistance  $R$ , and finally the first breakpoint  $E_1$ , and the inner slopes  $m_1$  and  $m_2$  of the Chua's diode driving-point characteristic.

The IC chip reported in this paper implements a Chua's circuit with the seven parameter values given in Table I. Five of these parameters have fixed values ( $C_1, C_2, E_1, m_1$ , and  $m_2$ ), and the two others ( $L$  and  $R$ ) are variable. This allows us to implement with our chip a 2-D parameter space of possible Chua's circuits.

It is shown in [5] how, by proper normalization of the three state variables,  $V_{C_1}$ ,  $V_{C_2}$ , and  $I_L$ , and of the time scale, the set of Chua's circuits with *different dynamics* can be specified with only four parameters ( $\alpha, \beta, a, b$ ), instead of seven. However, the control of  $R$  and  $L$  values still give us access to a 2-D parameter space of Chua's circuits. In particular, varying  $R$  leads to the variation of a combination of  $\beta, a$  and  $b$ , while varying  $L$  leads to the independent variation of  $\beta$ .

TABLE II  
OUTPUT PINS OF THE CHIP

Pin No.	Name	Description
1	$v_1$	output signal $v_{C_1}$
2	$v_2$	output signal $v_{C_2}$
3	$v_3$	output signal $r_d I_L$
4	$v_+$	positive terminal for bias
5	$v_-$	negative terminal for bias
6	$control_1$	terminal for $L$ tuning (optional use)
7	$control_2$	terminal for $L$ tuning (optional use)
8	$v_{GND}$	output ground reference

## 2.2. External Description of the Chip

Fig. 2 shows a photograph of the IC chip of Chua's circuit. The package is an eight-pin DIP that is 0.3 in wide and 0.1 in interlead. It can be plugged into standard breadboards or op amp sockets. The output pins of the chip are defined in Table II.

The chip is autonomous and therefore does not require any input signal. The bias is provided by a single 9V battery connected between terminals  $v_+$  and  $v_-$ . To set the two

independent bifurcation parameters, we use potentiometers  $R$  and  $R_\beta$  connected as shown in Fig. 3.<sup>1</sup>

The chip generates three output signals representing the three state variables of Chua's circuit. For convenience, the three signals are provided as three voltages  $v_1$ ,  $v_2$  and  $v_3$ , referenced to a common ground,  $v_{GND}$ . The outputs  $v_1$  and  $v_2$  are the voltage across capacitors  $C_1$  and  $C_2$  in Volts. The output  $v_3$  is a voltage proportional to the current through the inductor,<sup>2</sup> according to

$$v_3 = r_d I_L \quad (3)$$

The nominal value of the proportionality constant  $r_d$  is  $-500 \text{ V/A}$ .

### 2.3. Experimental Results

Using the above IC chip of Chua's circuit, powered by a 9V battery, we have generated chaos and bifurcation phenomena.

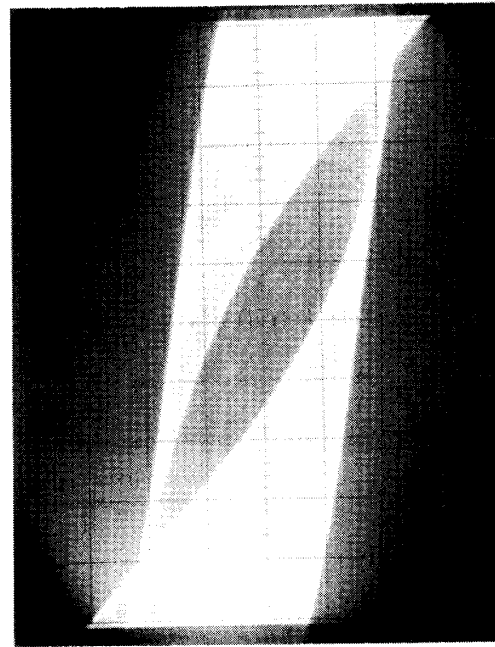
**Chaos Generator:** Using the nominal values of  $R = 1750\Omega$  and  $R_\beta = 20K\Omega$ , the chip works as a generator of chaotic signals. The chip operates in the double-scroll region. Fig. 4 shows the experimental time waveforms of the three output state variables  $v_1$ ,  $v_2$ , and  $v_3$ . Fig. 5 shows the three experimental Lissajous figures. They represent the projection of the chaotic strange attractor onto the  $(v_1, v_3)$ ,  $(v_2, v_1)$ , and  $(v_2, v_3)$  planes.

Fig. 6(a) shows a photograph with a magnified detail of the central part of the  $(v_1, v_3)$  projection of the double-scroll Chua's attractor. It corresponds to the same conditions of the lower left photograph of the previous figure. Fig. 6(b) shows a further magnification of the region. It is possible to distinguish some of the individual trajectories that thickly fill the outer surface of the attractor during the  $1/8s$  of the time-exposure photograph. In the center of this photograph, a perspective of the trajectories going along the inner part of the spiral cylinder can also be observed.

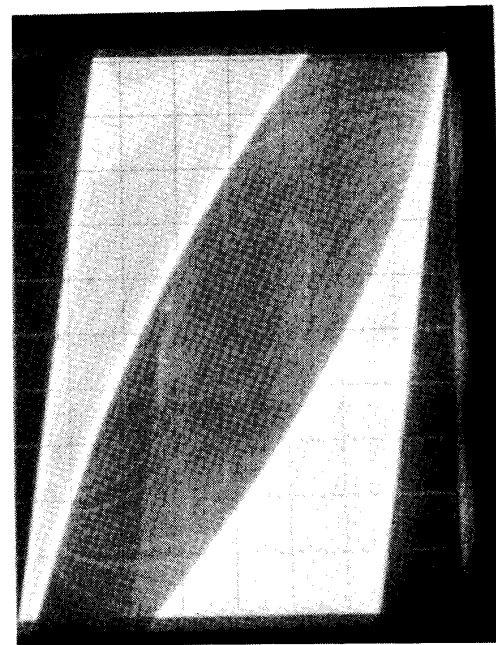
Note that for the same parameters, there is another possible solution: a large limit cycle associated with the outer slopes of the nonlinear element. However, this solution can be observed only if the initial conditions for the state variables is forced to be far away from the origin, outside the basin of attraction of the double-scroll Chua's attractor. Normally, when the chip is powered, the state variables are inside the basin of attraction of the chaotic attractor, because, due to current leakage, the storage capacitors are initially discharged. Fig. 7 shows a photograph superimposing the two solutions.

<sup>1</sup>The potentiometer  $R_\beta$  is used only as a convenient means of changing the bifurcation parameter  $\beta$  [5] in the experimental results presented in this paper. However, this potentiometer  $R_\beta$  is *not* necessary for the operation of the chip. An alternative way to change  $\beta$ , if desired, is by applying directly a voltage bias reference to pin *control*<sub>1</sub>, which controls the value of the internal voltage-controlled inductor. This latter approach of using electronic control of the internal  $L$ , may be more convenient for those using this chip as part of a larger electronic system.

<sup>2</sup>In previous experimental implementations of Chua's circuit this third signal, representing the current through the inductor, has been generated by measuring the voltage drop in a small resistor connected in series with the inductor, an approach which may distort the dynamic behavior of the circuit. In our implementation, as we will demonstrate in Section III, the signal  $v_3$  is generated without introducing any artifact affecting the dynamics of Chua's circuit.



(a)



(b)

Fig. 6. Detail around the origin of the projection of the double-scroll Chua's attractor onto the  $(v_1, v_3)$  plane. (a) Vertical and horizontal scale is  $200mV/div$ . (b) Vertical and horizontal scale is  $100mV/div$ .

**$R$  Bifurcation Sequence:** The well-known bifurcation sequence obtained by decreasing the resistor value  $R$  has been experimentally reproduced. As an example, Fig. 8, shows the experimental Lissajous figures in the  $(v_1, v_3)$  plane.  $R_\beta$  is kept constant at the nominal value of  $20K\Omega$ . As  $R$  is

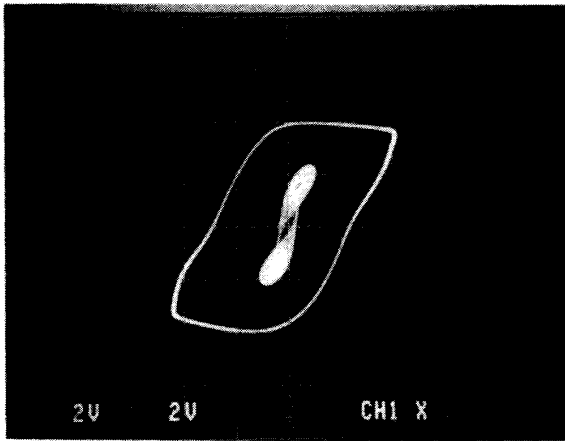
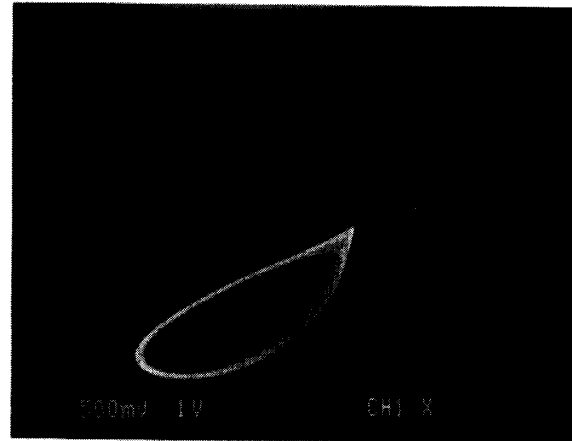
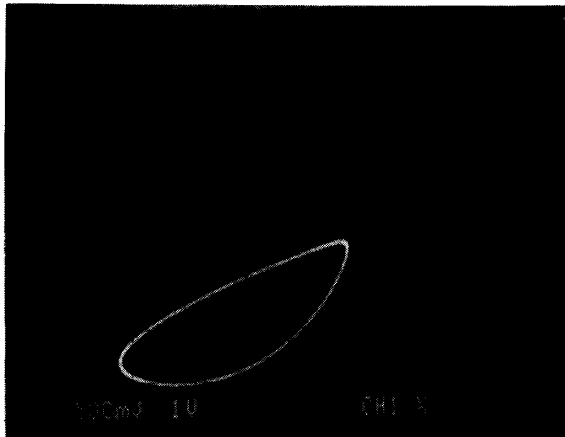


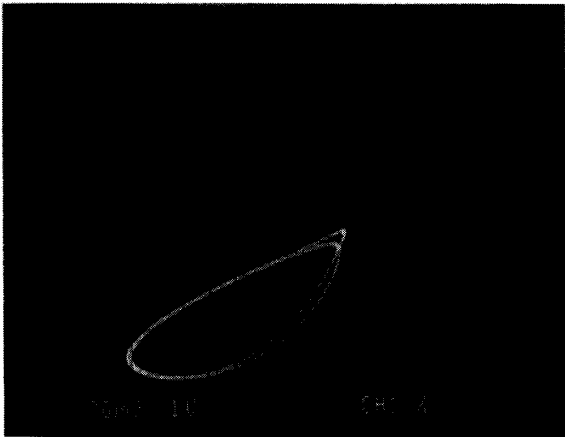
Fig. 7. Experimental limit cycle outside the double-scroll Chua's attractor. Projection into the  $(v_1, v_3)$  plane. Vertical scale is  $2V/\text{div}$ ; horizontal scale is  $2V/\text{div}$ .



(c)

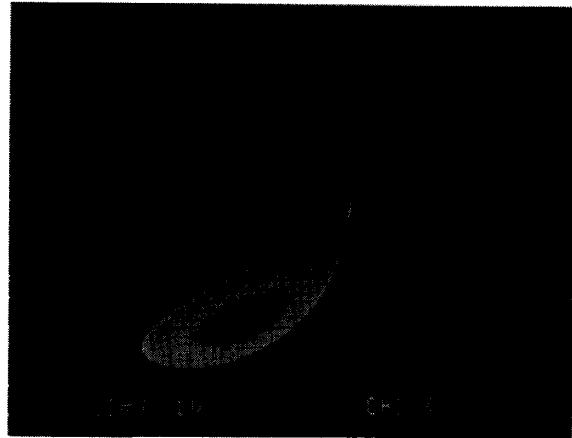


(a)



(b)

Fig. 8.  $R$ -bifurcation sequence. Experimental  $v_1$  versus  $v_3$  Lissajous figures. Vertical scale is  $1V/\text{div}$ ; horizontal scale is  $500mV/\text{div}$ . (a)  $R = 2050\Omega$ , period 1. (b)  $R = 2015\Omega$ , period 2.

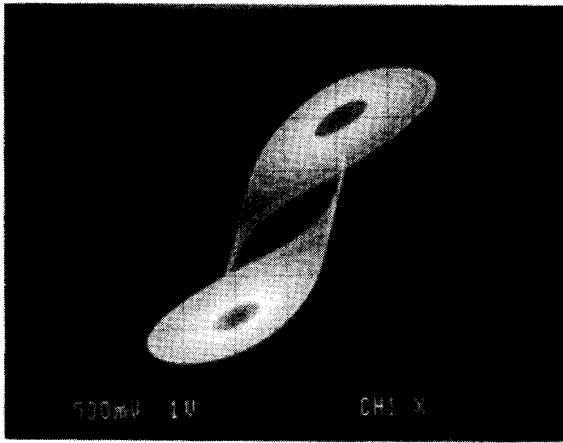


(d)

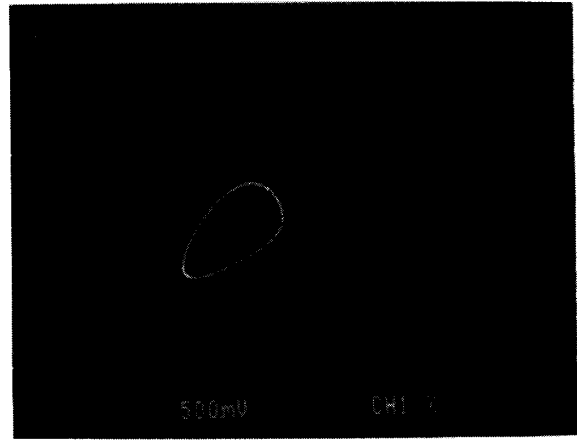
Fig. 8. (c)  $R = 2009\Omega$ , period  $n$ . (d)  $R = 1974\Omega$ , spiral Chua's attractor.

decreased from  $2050\Omega$  to  $1568\Omega$ , we observe periodic behavior emerging from a stable equilibrium point, then a period-doubling sequence, a spiral Chua's attractor, and, finally, a double-scroll Chua's attractor. As  $R$  is decreased further, the double-scroll Chua's attractor shrinks in size, and its central region becomes thinner. As  $R$  decreases below  $1568\Omega$ , the double-scroll Chua's attractor and the saddle-type periodic orbit collide with each other. At that point, the only solution is the large limit cycle determined by the outer segments of the Chua's diode characteristic.

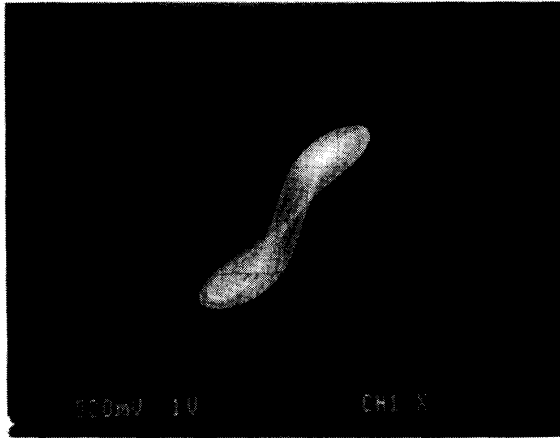
**$\beta$  Bifurcation Sequence:** This chip also allows independent change of the bifurcation parameter  $\beta$  [5]. Using the configuration of Fig. 3, the parameter  $\beta$  can be increased by decreasing the value of the potentiometer  $R_\beta$ . As an example, Fig. 9 shows the experimental Lissajous figures in the  $(v_2, v_1)$  plane.  $R$  is kept constant at the nominal value of  $1750\Omega$ . As  $R_\beta$  is decreased from  $26K\Omega$  to  $18K\Omega$ , we observe, as before, periodic behavior emerging from a stable equilibrium point, then a period-doubling sequence, a spiral Chua's attractor, and, finally, a double-scroll Chua's attractor. Observe that now the



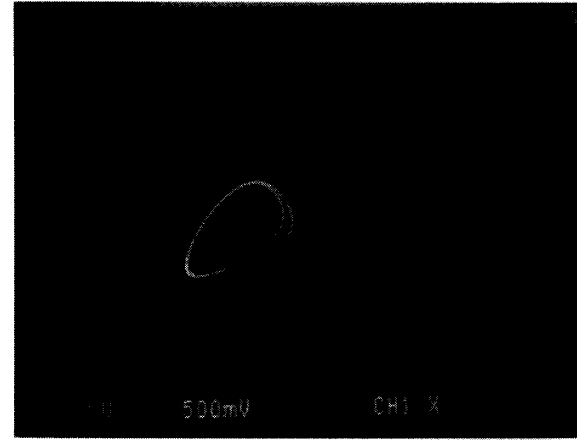
(e)



(a)



(f)



(b)

Fig. 8. (e)  $R = 1887\Omega$ , double-scroll Chua's attractor after birth. (f)  $R = 1568\Omega$ , double-scroll Chua's attractor before dying.

Fig. 9.  $\beta$ -bifurcation sequence. Experimental  $v_2$  vs  $v_1$  Lissajous figures. Vertical scale is  $500mV/div.$ ; horizontal scale is  $1V/div.$  (a)  $R_\beta = 26.0K\Omega$ , period 1. (b)  $R_\beta = 25.0K\Omega$ , period 2.

chaotic attractor does not decrease in size as we change the bifurcation parameter.

### III. INTERNAL STRUCTURE OF THE CHIP

The chip described in the previous section is implemented by using a CMOS process. In this section, we present the internal structure of the chip and describe the design procedure used. This design procedure can be used for the VLSI implementation of Chua's circuit in a different technology or with different parameters. This section is structured as follows. In the first part, we give the internal structure of the chip at the network element level. Then we detail the design of each of these elements at the transistor level for a CMOS technology. Finally, we present the physical structure of the entire chip.

#### 3.1. Internal Network-Level Structure

Fig. 10 gives the network schematic of the Chua's circuit implemented in the chip. It contains the nonlinear 2-terminal Chua's diode  $N_R$ , three capacitors  $C_1$ ,  $C_2$ , and  $C_3$ , and a

gyrator  $G$  with admittance matrix given by:

$$Y_G = \begin{bmatrix} 0 & g_d \\ -g_c & 0 \end{bmatrix} \quad (4)$$

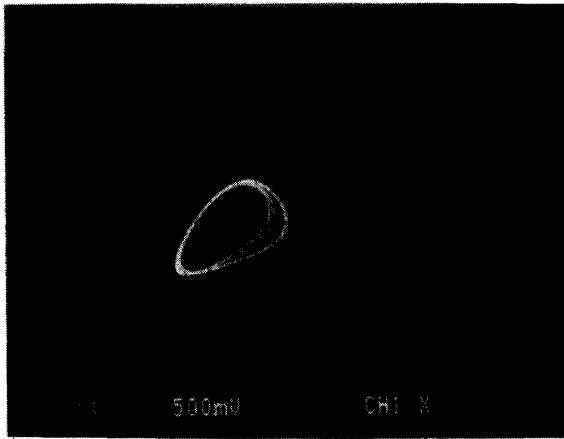
The gyrator terminated at its right port by capacitor  $C_3$  looks like an inductor of value

$$L = \frac{1}{g_c g_d} C_3 \quad (5)$$

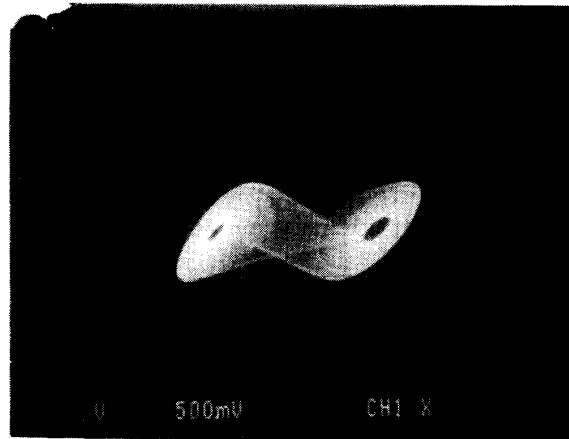
at its left port.

This circuit has three nodes. The voltage at these nodes, denoted by  $v_1$ ,  $v_2$ , and  $v_3$ , are available at the chip output. In spite of the fact that we have introduced an extra node, with respect to the circuit of Fig. 1, we have *not* introduced any other state variable into the circuit. The two new circuit variables introduced in the new circuit,  $v_3$  and  $i_{C_3}$ , have values determined by:

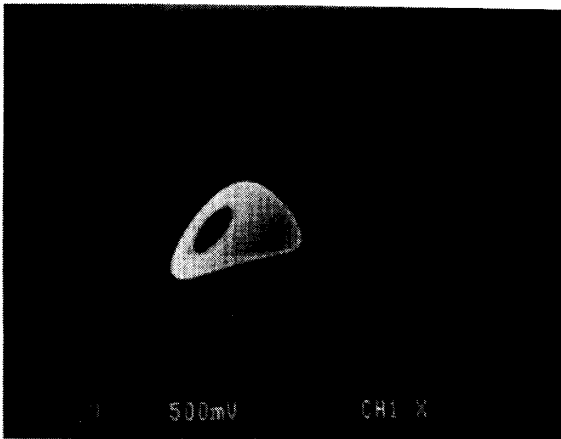
$$\begin{aligned} v_3 &= -\frac{i_L}{g_d} \\ i_{C_3} &= g_c v_2 \end{aligned} \quad (6)$$



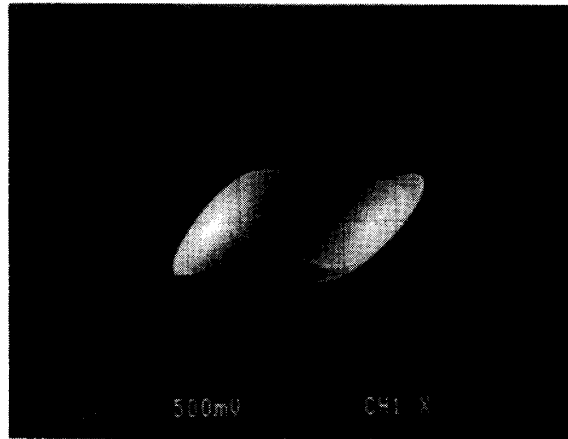
(c)



(e)



(d)



(f)

Fig. 9. (c)  $R_3 = 24.6K\Omega$ , period 4. (d)  $R_3 = 24.0K\Omega$ , spiral Chua's attractor.

Fig. 9. (e)  $R_3 = 22.0K\Omega$ , double-scroll Chua's attractor after birth. (f)  $R_3 = 18.0K\Omega$ , double-scroll Chua's attractor before dying.

Therefore, the circuits in Figs. 1 and 10 are equivalent. The latter is more suitable for VLSI implementation. Besides, the availability of the third state variable as a voltage allows us to experimentally measure this variable without introducing any measuring circuitry that could modify the dynamics of Chua's circuit.

The nonlinear resistor and the gyrator are active network elements and therefore need to be biased. We use a bias scheme in which only one external battery is used. Fig. 11 shows the entire circuit, including the bias. The floating external battery is connected to terminals  $v_+$  (pin 4) and  $v_-$  (pin 5). These terminals are internally connected to the positive and negative supply of the Chua's diode, of the gyrator, and of the bias circuit shown at the right of the figure. This bias circuit generates, at its low resistance output, a signal  $v_{GND}$  (pin 8), with voltage value in the middle of the values at the  $v_+$  and  $v_-$  nodes. This voltage  $v_{GND}$  is considered to be our ground.

### 3.2. CMOS Implementation

Fig. 12 shows the architecture of the entire circuit using CMOS amplifiers and capacitors. The two operational

transconductance amplifiers A and B, in positive feedback configuration, implement the Chua's diode [2]; the two back-to-back transconductance amplifiers C and D implement the gyrator [14]; and the serial set of CMOS diodes and the operational amplifier in negative feedback configuration implement the bias circuit.

For the implementation, we have used a  $2\mu m$  double-metal double-poly CMOS technology. The most relevant parameters of this technology are given in Table III. The capacitors have been implemented directly by using the two poly layers as capacitor plates (capacitance per unit area is  $470pF/mm^2$  in our technology). The voltage-mode operational amplifier has been designed using the two-stage Miller-compensated topology [12]. The four operational transconductance amplifiers have been designed using a topology based on simple differential pairs, because this gives the maximum effective frequency response and minimal input noise.

Fig. 13 shows the transistor schematic topology used for the OTA's. This topology is the same for all the OTA's, but each is designed to obtain a different transconductance characteristic.

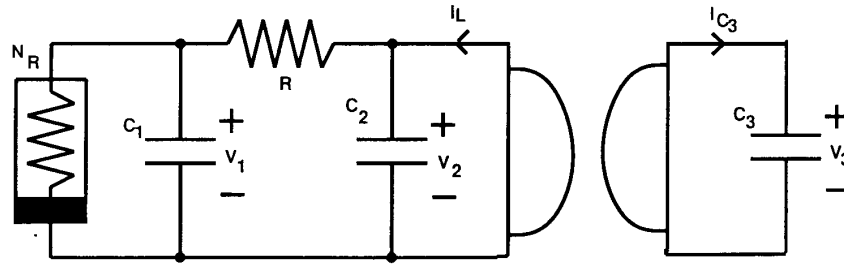


Fig. 10. Network schematic of the circuit.

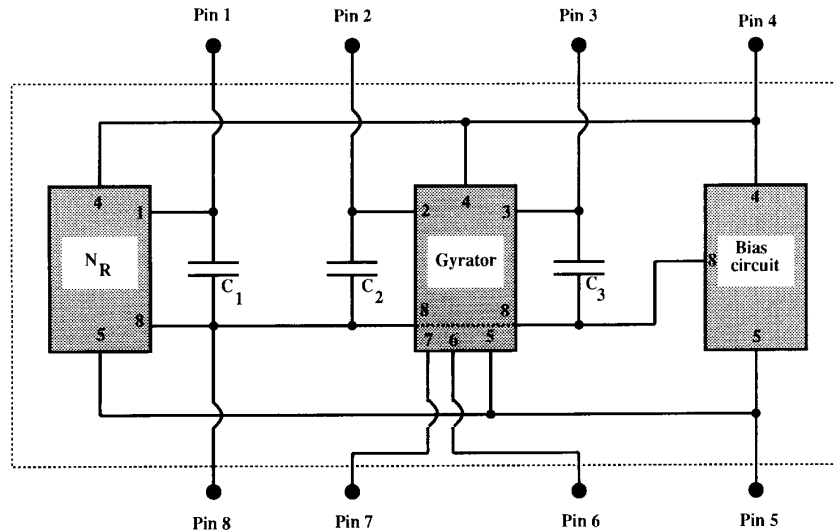


Fig. 11. Network schematic of the circuit including bias.

The transconductance gain of each of them, at the origin, is denoted as  $g_a$ ,  $g_b$ ,  $g_c$ , and  $g_d$ , respectively. Table IV gives their nominal values.

The transconductance amplifiers A and B implement the nonlinear Chua's diode. They determine the parameters  $m_0$ ,  $m_1$ , and  $E_1$ . The transconductance  $g_a$  and  $g_b$  of OTA A and OTA B should be equal to  $m_1 - m_2$  and  $-m_1$ , respectively. The output current of OTA A is limited to a constant value when  $v_1$  reaches the breakpoint  $E_1 = 0.7V$ . In this chip, the OTA A and B have fixed characteristics that are set by the self-bias circuit at the left of Fig. 13.<sup>3</sup>

The necessary nonlinearity of the circuit is produced by the cutoff of just a pair of transistors of the differential pair of OTA A: T101 (for  $v_1 \leq E_1$ ) or T102 (for  $v_1 \geq E_1$ ). Because transitions from cutoff to conduction can cause small delays, we want to prevent any other transistors in the signal path from cutting off. We achieve this by shorting the drains of T101 or T102 of OTA A with the equivalent transistors of OTA B. This connection (which does not appear in Fig. 12 to avoid clutter) is equivalent to the parallel connection of the current mirror of

<sup>3</sup>They can be adjusted if an external pin is assigned to the control line of OTA A. We have recently used that scheme in a Chua's diode chip prototype, and we have successfully used it to experimentally reproduce bifurcation phenomena by continuously varying the slope  $m_0$  (bifurcation parameter  $a$ ).

both OTA's.<sup>4</sup> The current bias of OTA B will always maintain all current mirrors in conduction. Using this scheme, we can obtain a driving-point characteristic for the Chua's diode that does not show any measurable hysteresis phenomena at the frequency of operation centered in the 160-KHz range. The design procedure to determine all the transistor dimensions of these two amplifiers can be found in [2]. For our particular bias levels, the final dimension values are given in Table V.

The transconductance amplifiers C and D implement the gyrator. They determine the parameter  $L$  according to (5). The capacitor  $C_3$  has a fixed value of 269 pF. The transconductances  $g_c$  and  $g_d$  are controllable in order to get a variable inductor. Their nominal values, given in Table IV, are obtained when the control line of OTA C (pin 7 of the chip) is left open, and the control line of OTA D (pin 6 of the chip) is connected to  $R_\beta = 20K\Omega$ , as indicated in Fig. 3. Under this condition, the gyration ratio is  $1.23 \times 10^6$ , and the emulated inductor has a value of 0.33 mH. This value can be changed in a  $\pm 50\%$  range by  $R_\beta$  adjustments. All transistor dimensions of these amplifiers are shown in Table V.

The LC circuit formed by  $C_2$  and the emulated inductor has a quality factor of  $Q = 78.5$ , which is actually higher than

<sup>4</sup>Equivalently, it is also possible merging all current mirrors of OTA A with those of OTA B, but increasing accordingly the width of their transistors.



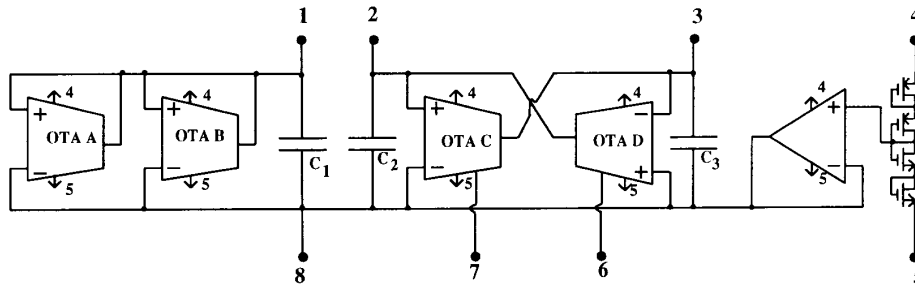


Fig. 12. Architecture of the chip.

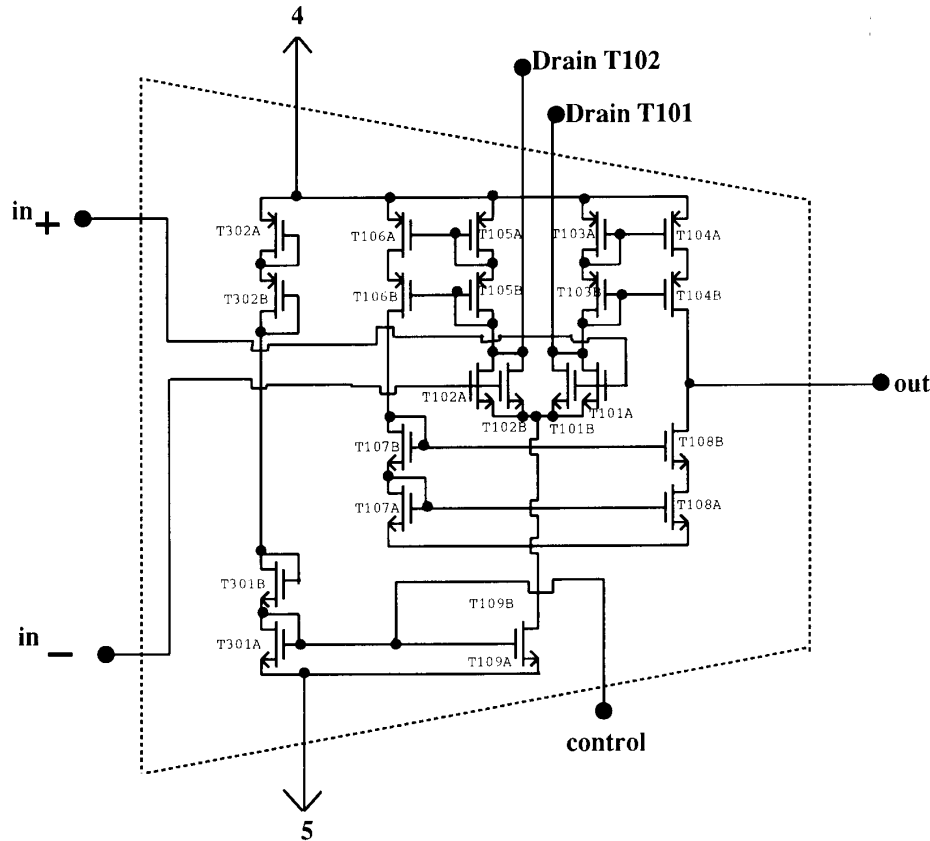


Fig. 13. Transistor schematic of the OTA's.

what is usually obtained by using discrete components.<sup>5</sup> This has been achieved by designing gyrator amplifiers with very large ratios between their transconductances and their output conductances.

A conventional operational amplifier and a set of diodes are used to implement the bias circuit. The diodes are made by gate-to-drain connected transistors. They are sized so that their midpoint voltage ( $v_{GND}$ ) is just in the middle of the values at the  $v_+$  and  $v_-$  nodes. The accuracy of this voltage division is not critical, because the circuit is, to first order, insensitive to

<sup>5</sup> A typical series resistance of  $13\Omega$  in the inductor will degrade the quality factor to approximately  $Q = 25$ .

TABLE III  
TECHNOLOGICAL DATA

Parameter	N-channel	P-channel	Unit
$V_{th}$	1.0	0.8	V
$\mu C_{ox}$	47	23	$\mu A/V^2$
$\gamma$	1.06	0.45	$\sqrt{V}$
$\Delta L$	0.54	0.42	$\mu m$
$\Delta W$	0.07	0.17	$\mu m$

variations in the dc voltage difference between  $v_{GND}$  and the supply nodes. AC variations are minimized to less than 6 mV by the use of a high-gain conventional operational amplifier with negative feedback.

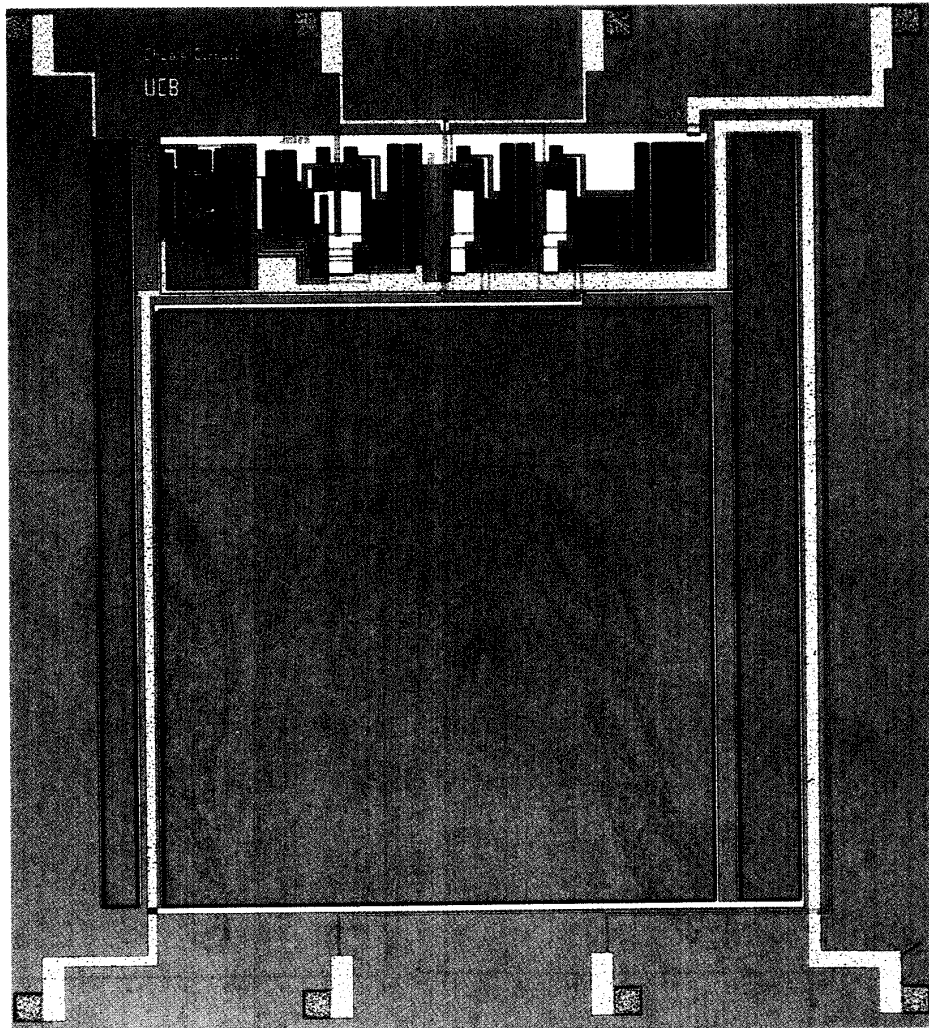


Fig. 14. Micrograph of the fabricated circuit.

TABLE IV  
TRANSCONDUCTANCE VALUES

OTA	transconductance	Unit
A	0.37	mA/V
B	0.41	mA/V
C	0.41	mA/V
D	2.00	mA/V

### 3.3. Physical Structure

The circuit has been fabricated in  $2\ \mu\text{m}$  CMOS technology of ORBIT Semiconductors [15]. Fig. 14 shows a micrograph of the fabricated circuit. It occupies a silicon area of  $2.5 \times 2.8$  mm. All the active circuitry is in the central part of the upper side of the die. The three rectangular blocks at the bottom, from left to right, are, respectively, capacitors  $C_1$ ,  $C_2$ , and  $C_3$ .

### IV. NUMERICAL SIMULATIONS

The experimental results are validated with numerical simulations. As an example, Fig. 15 shows a device-level numerical

simulation of the chip in chaotic operation, with the same conditions used to obtain the experimental results of Fig. 5. The correspondence with the experimental data shown earlier is excellent.

### V. CONCLUDING REMARKS

In this paper, we have presented a working microelectronic Chua's circuit that produces chaotic signals whose experimental dynamics are in close agreement with theoretical and numerical predictions based on the ideal Chua's equation [5]. The circuit occupies an area of 7 square millimeters in  $2\ \mu\text{m}$  CMOS technology. In a large die, it is possible to place 57 of our circuits. The number of possible circuits on a chip can be increased to about 600 by applying the scaling rules given in Appendix I.

Our major motivation for this work was the need of microelectronic circuits that can be used as a building block of several classes of systems that require the use of chaotic behavior. Some examples are secure communication systems

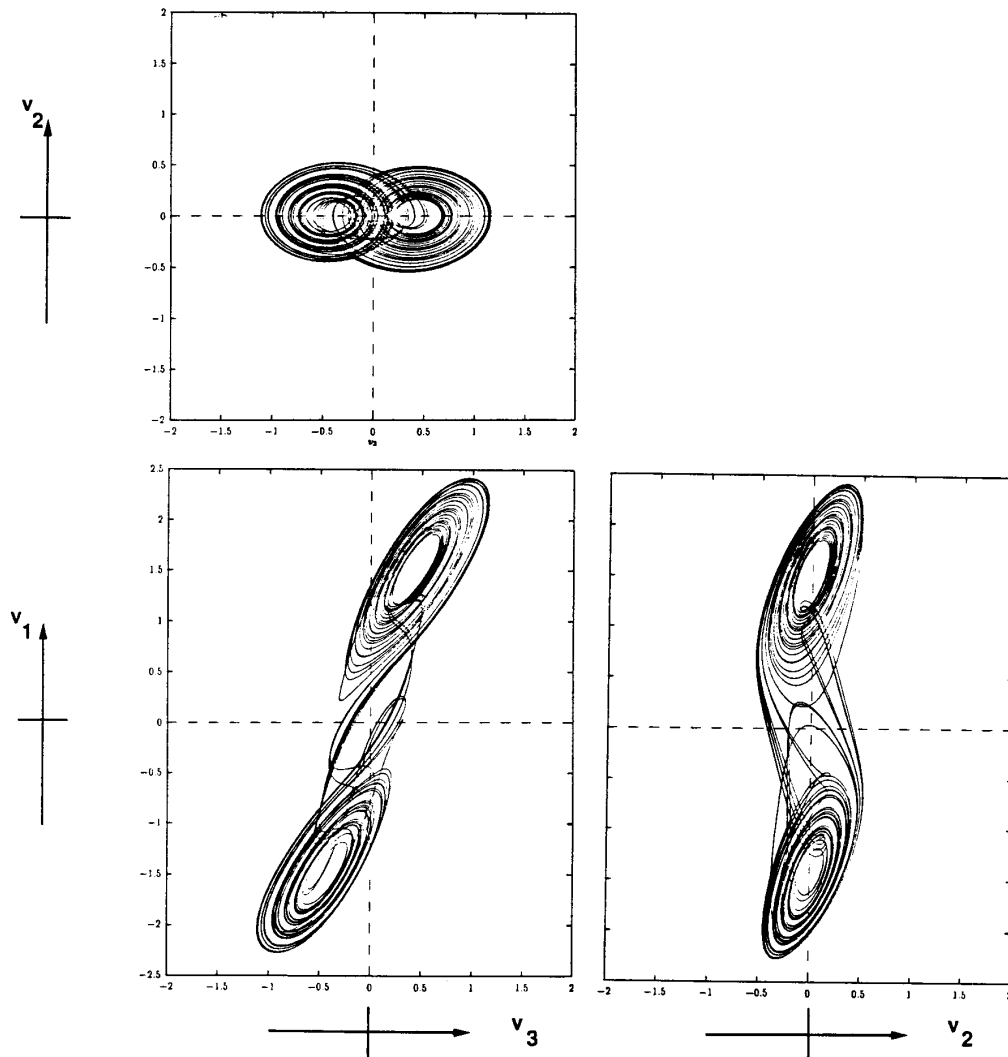


Fig. 15. Lissajous figures of the double-scroll Chua's attractor obtained by computer simulation. All scales are  $500mV/div$ .

based on chaos synchronization [10] and network arrays [11, 16] with spatially chaotic dynamics. The successful implementation of these systems relies upon the availability of a chaotic electronic component exhibiting experimental dynamics that closely resemble a mathematical model and that can be accurately controlled. We hope that our design will facilitate the VLSI implementation of those emerging classes of circuits and systems that exploit chaotic phenomena for useful applications.

#### APPENDIX I SCALING RULES FOR HIGH-DENSITY VLSI IMPLEMENTATION OF CHUA'S CIRCUITS

With our present design, it is possible to design chips containing up to 57 circuits (assuming a large die size of  $20mm \times 20mm$ ). Those interested in higher integration den-

sities can scale down the capacitor's values and the current levels. The simplest scaling scenario is a linear scaling in which the new values of capacitors and conductances are  $kC_1$ ,  $kC_2$ ,  $kC_3$ ,  $km_1$ ,  $km_2$ , and  $\frac{1}{k}R$ , where  $k$  is the scaling parameter. The scaling of the capacitors is done simply by reducing the area. The scaling of the conductances is done by reducing proportionally the width of the transistors of the input stage of the OTA A and B. The gyrator design should be unchanged.

After doing this scaling, the circuit will operate at the same frequency, and we will get the same voltage levels for all variables. All the currents, however, will be scaled according to the same factor  $k$ . Because both the capacitors and the currents are scaled with the same factor, the GBW of all transconductance amplifiers does not degrade in first order and remains above the operating frequency of the circuit.

TABLE V  
MASK DIMENSIONS OF THE INTERNAL TRANSISTORS OF THE OTA'S

Device	W ( $\mu\text{m}$ )			L ( $\mu\text{m}$ )
	OTA A	OTA 's B and C	OTA D	
$T_{101A}, T_{101B}, T_{102A}, T_{102B}$	40	15	15	6
$T_{103A}, T_{105A}, T_{106A}$	280	400	400	4
$T_{103B}, T_{105B}, T_{106B}$	280	400	400	2
$T_{104A}$	280	400	3200	4
$T_{103B}$	280	400	3200	2
$T_{107A}$	140	200	200	4
$T_{107B}$	140	200	200	2
$T_{108A}$	138	200	1600	4
$T_{108B}$	138	200	1600	2
$T_{109A}$	100	476	476	6
$T_{301A}$	50	50	50	10
$T_{301B}$	100	100	100	10
$T_{302A}, T_{302B}$	33	33	33	10

The area estimate for the entire microelectronic Chua's circuit in square millimeters is equal to  $0.5 + 6.5(k)$ , where  $0.5\text{mm}^2$  is the area of the nonscaling elements and  $6.5\text{mm}^2$  is the original area of the scalable elements. The lowest value of  $k$  is determined by several factors, including noise degradation, parasitic capacitances that affect the dynamics, and degraded amplifier phase margins and linearity ranges. If we consider a realistic lower limit of  $k = 0.02$ , this gives 634 Chua's circuits per chip. Higher densities can be achieved by using more advanced technologies.

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