Advanced Analog Integrated Circuits

Biasing

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Transistor Biasing

- **Design Parameter**
  - $g_m$, $V^*$, $f_T$

- **Layout Parameter**
  - $W$, $L$
  - Fingers $F$
  - Multiplicity $M$
Example

Design:
\[ g_m := 1\text{mS} \quad V_{\text{star}} := 120\text{mV} \quad f_T := 6\text{GHz} \]

Layout (lookup):
\[ L := 250\text{nm} \quad I_{d_w} := \frac{5}{A/m} \]

\[ I_D := 0.5 \cdot g_m \cdot V_{\text{star}} = 60\mu\text{A} \]

\[ W := \frac{I_D}{I_{d_w}} = 12\mu\text{m} \quad + \]

CMOS 180
grade=nominal

OP Analysis OP1

\begin{circuitikz}
\node (M1) at (0,0) {\text{M}\textsubscript{bias}};
\node (I1) at (1,0) {I_1=60\mu\text{A}};
\node (I2) at (0,-1) {I_2=60\mu\text{A}};
\node (M1_vgs) at (1,-0.5) {\text{v}_{gs}};
\node (M1_vds) at (1,-1) {\text{v}_{ds}};
\draw (M1) -- (M1_vgs) -- (M1_vds) -- (M1_vgs) -- (I1) -- (I1) -- (I1_vgs) -- (M1_vgs);
\end{circuitikz}
Operating Point Analysis

Instance: M1 of nmos3
Model: nfet.4
Primitive: bsim3v3

d : V(v_ds) = 523.447 mV

g : V(v_gs) = 523.447 mV

s : val(0) = 0

b : val(0) = 0

type = n

region = sat
reversed = no

ids = 60.037 uA
isub = 41.0222 aA
vgs = 523.447 mV
vds = 523.447 mV
vbs = 0 V
vgb = 523.447 mV
vdb = 523.447 mV
vgd = 1.32916 pV
vth = 502.512 mV
vdsat = 78.9438 mV
vfbeff = -1.00379 V

gm = 1.00019 mS

gds = 18.5458 uS
gmbs = 283.567 uS

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Current Sources

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Current Source Realization: Mirror

Choices for $I_{\text{ref}}$: resistor, bandgap, constant $g_m$ reference, …
Cascode Bias

- Choose $W_5 \equiv W_1/3$ such that $V_{DS1} \approx V_1^* + 50\text{mV}$ (use lookup)
- Note: ok for cascodes to have different $W/L$
- Insensitive to body-effect
Reducing Bias Network Power Dissipation

- Share bias network between several amplifiers
- Ratio mirror

Use $M$ → $M$ parallel devices (preferable over scaling $W$)
Bias Network Power Dissipation

Minimize:

- Share bias network between several amplifiers
- Ratio mirror
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Current Sources

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Noise

\[ \bar{i}_{on}^2 = \bar{i}_{n1}^2 + \bar{i}_{n2}^2 + M^2 \bar{i}_{n3}^2 \]

\[ \bar{i}_{on}^2 = 4kT\gamma g_{m1} \left\{ 1 + \frac{g_{m2}}{g_{m1}} (1 + M) \right\} \Delta f \]

\[ \bar{i}_{on}^2 = 4kT\gamma g_{m1} \left\{ 1 + \frac{V_1^*}{V_2^*} \left(1 + M\right) \right\} \Delta f \]

- **Tradeoff:**
  - Maximizing \( V_2^* \) minimizes noise
  - But reduces available output range

- Beware of noise from bias network
  - Place decoupling capacitor across \( V_{GS3} \)
Low Noise Current Source

Active (BJT or MOS)

\[ R_o = \frac{a_{vo}}{g_m} = \frac{a_{vo} V^*}{2 I_o} \]

\[ i_{no}^2 = 4kT \cdot 2\gamma \cdot \frac{I_o}{V^*} \Delta f \]

Resistor

\[ R_o = \frac{V_R}{I_o} \]

\[ i_{no}^2 = 4kT \cdot \frac{I_o}{V_R} \Delta f \]

For equal voltage headroom \( (V_R = V^*) \), active device has larger \( R_o \) but somewhat worse noise: low noise costs headroom!