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Low-Power CMOS RC Oscillators Based on Current Conveyors

J. Popović, B. Nikolić, K. W. Current, A. Pavasović, D. Vasiljević

Abstract - Experimental results for new low-power, reliable start-up CMOS RC oscillators are presented. The oscillators use a modified Fabre-Normand translinear current conveyor. Measurements show reliable oscillation start-up for power supply voltages that range from 1.5V to 5V with current consumption from 100nA to 1.2mA, respectively. Oscillation frequencies up to 55MHz have been observed in circuits fabricated in a modest 2μm CMOS technology.

I. INTRODUCTION

RC oscillators based on current conveyors have received substantial attention in the past decade [1]. Many descriptions of harmonic RC oscillator circuits with current conveyors can be found in the open literature [2, 3, 4, 5]. The circuits vary by the number and type of current conveyors and by number of used passive components. Wien's oscillator with the current conveyor of the second type, whose oscillating frequency can be changed by changing of appropriate current in the range from 20MHz do 90MHz, is described in [6]. The circuit is implemented in 2μm BiCMOS technology. At supply voltage of 5V, the power consumption is 50mW at 50MHz, and 70mW at 80MHz.

By using translinear current conveyors, i.e. current processing of signals, wide bandwidth and large amplification are achieved. A harmonic oscillator circuit containing two tranlinear current controlled current conveyors of the second type implemented with bipolar transistors is described in [7]. The simulation results at supply voltage of ± 2.5 V and polarization current of 100 μA, show that maximum oscillating frequency is around 1 MHz.

The first relaxation oscillator with Fabri-Normand translinear current conveyor of the second type is described in [8]. It is a crystal oscillator whose active part is implemented using discrete bipolar transistors, and whose bandwidth is around 100 MHz.

The characteristics of oscillators implemented with discrete bipolar transistors are much better than those with discrete MOSFETs [8]. The maximum reported frequency of CMOS oscillators is an order of magnitude lower than that of bipolar oscillators. The reason of this poor performance of CMOS oscillators was that the discrete CMOS transistors used had very wide channels. The input capacitance of such transistors is large and it significantly reduces the frequency range of the circuit. This problem is overcome by implementing the oscillators as integrated circuits [9]. A short description of one kind of such oscillators will be given, followed by simulation and measurement results.

II. THE RC RELAXATION OSCILLATOR MODEL

The three main parts of the relaxation oscillator model (Fig. 1) are: the active part with the parasitic elements, the bias circuit and the timing circuit. The active part of the circuit is the negative impedance converter. It determines the oscillator characteristics and conditions for the timing network operation [10].

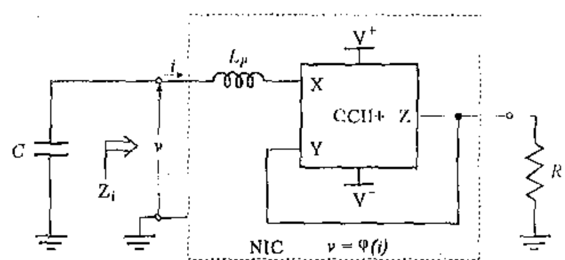


Figure 1. Oscillator with current controlled NIC.

The current-controlled negative impedance converter (NIC) is a two-port system which has an "N" shaped current-voltage characteristics: $v=\varphi(i)$ (Fig. 2). For small currents, the circuit images the resistance R from one port into a negative resistance $-R_n$ of approximately same absolute value on the other port. The characteristic can be easily adjusted to pass through the coordinate origin and there is no need to use additional biasing circuitry for placing the quiescent operating point, as is the case in some other oscillator implementations [8].

A capacitive timing network is connected on the opposite NIC port from the resistor R. The capacitive timing network allows quick, step current changes, while the voltage is continuous. The NIC parasitic input inductance L_p, of an arbitrarily small value, provides fast changes of relaxation oscillator states [10]. For convenience, it is taken out of the NIC two-port and shown at the NIC input (Fig. 1). The other parasitic elements, even if present, can be neglected, since they are lumped by the

J. Popović is with the Department of Electronics, Faculty of EE, Belgrade, Yugoslavia, E-mail: jelena@el.etf.bg.ac.yu

B. Nikolić and K. W. Current are with the Department of ECE, UC Davis, USA,E-mail bora@ece.ucdavis.edu

A. Pavasović is with Lola Institute, Kneza Višeslava 70A, Belgrade, Yugoslavia

D. Vasiljević is with ENEL, B. Revolucije 89, Belgrade

comparatively much larger capacitance C. The characteristic equation of this oscillator is [10]:

$$\lambda^2 + \frac{1}{L_p}\varphi'(i)\lambda + \frac{1}{L_p C} = 0. \qquad (1)$$

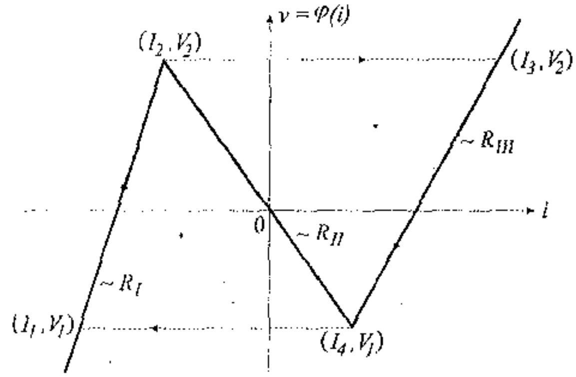


Figure 2. Current controlled NIC current-voltage characteristic.

The static characteristics of the NIC circuit can be approximated by linear segments of appropriate slope in the characteristic intervals of the control current values (Fig. 2). The quiescent point of this system is at the coordinate origin, and the first derivative of $\varphi(i)$ in the neighborhood of the coordinate origin should be constant: $\varphi'(i) = -R_n = const$. Then the solutions of (1) are:

$$\lambda_{1,2} = \frac{R_n}{2L_p} \pm j\sqrt{\frac{1}{L_p C} - \left(\frac{R_n}{2L_p}\right)^2}\,. \qquad (2)$$

Since the real part is always positive (R_n , $L_p>0$), the condition for oscillation build-up is always satisfied and does not depend on the values of the circuit parameters. The speed of the oscillation build-up depends on, and thus can be controlled by, the value of the imaged negative resistance R_n, and consequently by the value of the resistance R at the NIC input. By increasing R, the speed of the oscillations build-up is increased, but the other performances of the oscillators are degraded.

The imaginary part of the solutions (2) shows that, depending on the values of the circuit parameters, there can be two types of the oscillation build-up. If the condition:

$$R_n > \sqrt{\frac{4L_p}{C}} \qquad (3)$$

is satisfied, the solutions (2) are real and different. In the phase plane (i,v), the operating point is moving on the strait line from the coordinate origin until the point where the current or voltage are limited by the circuit static characteristics. The trajectory of the operating point during the start-up of oscillations is shown on Fig. 2. The system limit cycle is reached after the first full cycle.

The second type of oscillation build-up is present when the solutions (2) are complex, i.e. when condition (3) is not satisfied. The quiescent point in that case leaves the coordinate origin on a spiral trajectory, and stays on it until the current and voltage values reach the values determined by the turning points of the characteristics $v=\varphi(i)$, when the limit cycle is then reached.

The frequency of oscillation is determined by shape of NICs static characteristic and value of capacitor C in the timing network [10].

III. Modified CMOS Current Conveyor

The Fabre-Normand current conveyor [11] has a large bandwidth and simple CMOS circuit implementation. NICs based on the Fabre-Normand current conveyor are suitable for the design of the active part of relaxation oscillators which are easily implemented in standard IC technology.

We modified the original Fabre-Normand current conveyor for low-voltage, low-power operation [12]. The original Fabre-Normand circuit consists of a translinear cell composed of two improved Wilson current mirrors [11]. To provide low-voltage, low-power operation, we replaced improved Wilson with simple current mirrors without affecting the circuit functionality [9]. The resulting RC oscillator is shown in Figure 3. In general, when the operating voltage is lowered, the problem of the start-up of oscillations can be aggravated [13]. However, the proposed circuits have a reliable start-up even with very low supply voltages, since the oscillations startup is based on negative resistance.

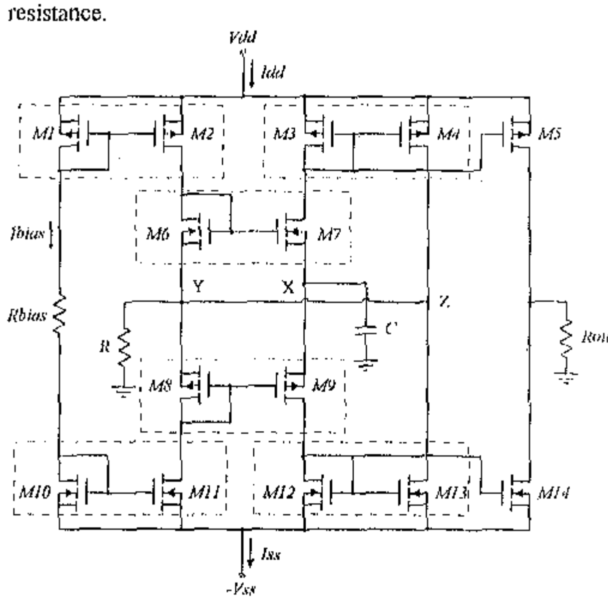


Figure 3. RC oscillator with modified Fabre-Normand circuit.

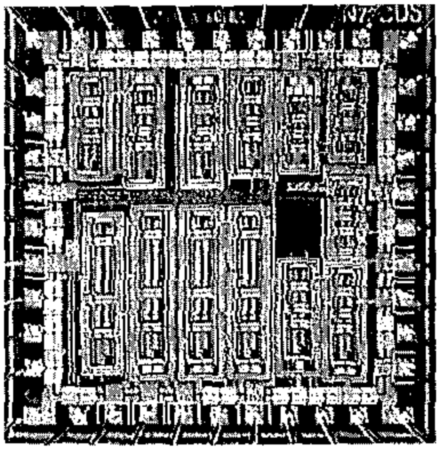


Figure 4. Die photo of the test chip, showing 13 oscillator circuits separated by guard rings.

IV. TEST CHIP

The test chip (Figure 4) was fabricated using a standard MOSIS 2μm n-well double-poly two-metal CMOS technology. The chip contains thirteen oscillators realized with three types of Fabre-Normand circuits (Table I). Type 1 oscillators are based on the original Fabre-Normand circuits and are thus not suitable for operation with low supply voltages. Oscillators of types 2 and 3 are based on modified Fabre-Normand circuits that differ from each other in their transistor sizes.

In order to minimize the random transistor mismatch and to achieve the maximal oscillating frequency, the design and layout are based on unit transistors: 16μm wide and 2μm long in type 1 and 2 oscillators, and 8μm wide and 2μm long in type 3 oscillators. Matched transistors are laid out in an interdigitized and common centeroid format. Each group of p-type transistors in the same oscillator is placed in a separate well to minimize the mutual interference. One oscillator of the each type had separated power supplies for the power consumption measurement. The other oscillators with common power supply pins are separated by the use of two n- and p-contact guard rings. In order to obtain a complete set of operating data, each oscillator type is implemented with and without the on-chip biasing circuitry and timing capacitors. Two cells are setup to allow characterization of the current conveyor.

The circuit realization of these oscillators requires implementation of two resistors (R_{bias} and R), with values in the order of kΩ. For the resistor R, which determines the slope of the NIC static characteristic, a passive implementation was chosen to provide characteristic linearity. The resistor R_{bias} in some oscillator circuits is implemented using an MOS transistor with the gate at the midpoint potential between the power rails. The load resistor shown in Figure 3, R_{out}, is always externally connected.

In a fully monolithic realization of a CMOS RC oscillator, the accuracy with which the oscillation frequency may be set depends upon the accuracy of realization of the values of R and C. Capacitor realization is sensitive to underetch effects and oxide thickness. To minimize these effects, our capacitors are realized with combinations of unit poly-poly capacitances of nominal 1pF value.

Osc. type	FN circuit	V_{dd} [V]	W_n [μm]	W_p [μm]	f_{max} [MHz]	Idd [mA]
1	original	5	32/160	80/400	34.60	1.5
2	modif.	2.5 5	32	80	35.6 54.9	0.56 2.46
3	modif.	1.5 5	8	16	0.1 44.1	100nA 1.24

Table 1: Implemented oscillators (R_{out} = 10 kΩ).

V. SIMULATION AND EXPERIMENTAL RESULTS

Oscillators performances are summarized in Table 1. Our focus is on type 2 and 3 oscillators, because the type-1 oscillator requires a relatively high supply voltages (±4V) for proper operation. I_{dd} versus frequency is shown in Figure 5.

Measurements agree within 10% to values predicted by simulations. The measured frequencies are about 10% higher than simulated, as shown in Figure 6.a, possibly due to low capacitance values.

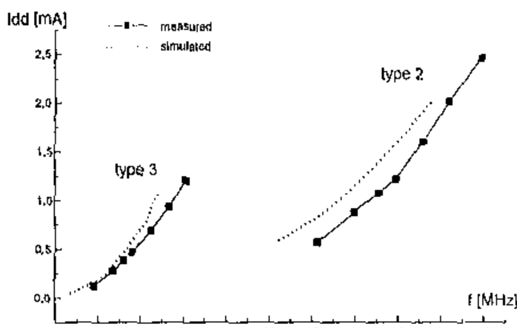
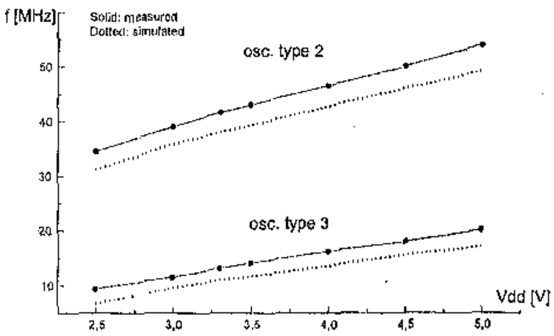


Figure 5. Current consumption vs. frequency for the oscillators of the type 2 and 3.

Four oscillators were realized without on-chip timing capacitors. An external timing capacitor is used to set the oscillation frequency. Figure 6.b shows the dependence of the oscillating frequency from the external capacitance, for three supply voltages. The parasitic impedances at the pins limit the operating frequency for this configuration.



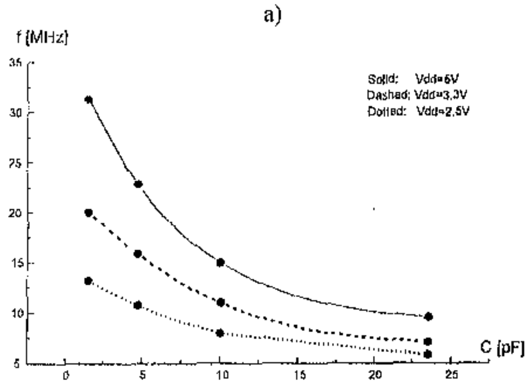


Figure 6. a. The oscillating frequency vs. supply voltage for the oscillators of type 2 and 3.

b. Oscillating frequency vs. external capacitance for different supply voltages.

VI. Conclusions

In comparison to other IC realizations of oscillators with current conveyors, the oscillators presented here have significantly smaller current consumption and similar operating frequency range. Realization of these circuits in a submicron technology should provide much wider frequency range and lower power consumption. The oscillators presented here should perform comparably to the fastest reported when realized in a finer resolution technology. As opposed to this type of negative resistance oscillator, most recently reported oscillators are feedback type.

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