A 65-nm CMOS Wideband TDD Front-End With Integrated T/R Switching via PA Re-Use

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***Abstract*— Time-division duplex (TDD) systems rely on off-chip transmit/receive (T/R) switches to isolate the RX from the high-output power of the TX, while existing on-chip T/R switching solutions are narrow-band or high loss. This paper presents a wideband integrated T/R switching technique that eliminates the conventional, lossy series T/R switch from the signal path. The system reconfigures the PA as an LNA during the receive mode, and utilizes only DC mode control switches to enable TDD co-existence. To demonstrate this technique, a polar transmitter that can be re-purposed into a common-gate LNA is implemented in 65-nm CMOS. With an integrated front-end balun transformer, the transmitter achieves 20-dBm peak output power with 32.7% peak drain efficiency. In the receive mode, the PA is reconfigured into a wideband 3.4–5.4-GHz LNA achieving −6.7-dBm P1dB, and 5.1-dB noise figure.**

***Index Terms*— Low-noise amplifier, PA re-use, polar transmitter, power amplifier, T/R switch, TDD front-end, transformer.**

I. Introduction

TIME-DIVISION duplex (TDD) co-existence with high-transmit power is conventionally enabled by discrete transmit/receive (T/R) switches (TRSWs). As mobile devices must support increasingly more wireless standards and bands, the number of discrete front-end components needed—including TRSWs—increases accordingly, resulting in greater insertion loss (IL), cost, and PCB area. Furthermore, discrete TRSWs are accompanied by additional degradations from PCB and package parasitics. Thus, there is significant interest in integrated wideband TRSWs to support modern multi-band radios.

In TDD systems, transmit and receive paths operate in the same frequency band while sharing an antenna. The TRSW selects between TX and RX as well as isolate the two from each other. In TX mode, the switch shields the receiver from high PA output power, and in RX mode, the switch prevents the idle PA from providing a leakage path or adding noise at the RX input. In addition to strong isolation, TRSWs must also have low IL to minimize degradations to PA output power, PA efficiency, and RX noise figure (NF) and sensitivity.

To meet the isolation and IL requirements, many commercial TRSW modules still use expensive materials, such as GaAs or thick-film SOI, to implement pHEMT or PIN diode switching devices [1]. Integrating TRSWs onto bulk silicon processes is challenging due to, first, the PA's high output voltage swings that are beyond those tolerated by modern CMOS devices, and second, silicon's low substrate resistance causing leakage and loss at gigahertz frequencies. In a survey of published SoC systems, many still do not have integrated T/R- or band-switching functionality [2]–[5]. Systems with integrated T/R switching have thus far been limited to low-power Bluetooth applications [6]–[8].

Enabling integrated, higher power T/R switching is an important next step toward true software-defined radios (SDRs) [9]. Existing SDR works have demonstrated RF-DAC transmitters satisfying wideband, multi-standard operations [10], and multi-band, multi-mode receivers trading off NF to operate in a wide range of frequencies [11]. Newly deployed TDD bands in LTE span 1.8–4 GHz. Covering these, along with WLAN, requires multiple off-chip narrow-band TRSWs. While traditional cellular transceivers require low NFs and high TX efficiencies, many emerging applications, envisioned to implement the machine-type communication mode of LTE, could tolerate reduced performance. These applications are expected to be sensitive to component counts, and would thus greatly benefit from integrating TRSWs with multi-mode, multi-standard wideband transceivers. We target operation at frequencies above 3 GHz due to the limited number of designs in that space.

We proposed an innovative architecture with integrated T/R switching for wideband TDD co-existence [12]. Instead of using a front-end switch to isolate and select between PA and LNA blocks, the PA is re-used as an LNA during receive mode. Fig. 1 illustrates the proposed scheme. Isolation is no longer an issue as the PA and LNA are the same block, with a single antenna port. The conventional in-line TRSW has been eliminated. Instead, there are only DC power and control switches to enable PA to LNA transformation.

As proof-of-concept for the proposed T/R switching technique, we present a TDD front-end composed of a polar transmitter, a PA re-usable as an LNA, and an integrated

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TABLE I
SUMMARY OF INTEGRATED TRSW WORKS

	Technology	Freq. (GHz)	SW Topology	IL (TX/RX) (dB)	Isolation (TX/RX) (dB)	P1dB (dBm)
[17]	0.13μm	0.9-2.4	series-shunt	0.5-0.8/1-1.2	24-29	28-31.3
[15]	90nm	2.4	resonance	0.4/0.2	30/16	30
[18]	0.18μm	2.5	series-shunt	1.3/2.7	28	33
[19]	32nm	2.4	resonance	1.3/1.1	-/32	34
[21]	90nm	5-7	transformer	2.65/2.52	42	35.7
[16]	45nm SOI	1.3-3.3	series-shunt	-/2	-	27.7

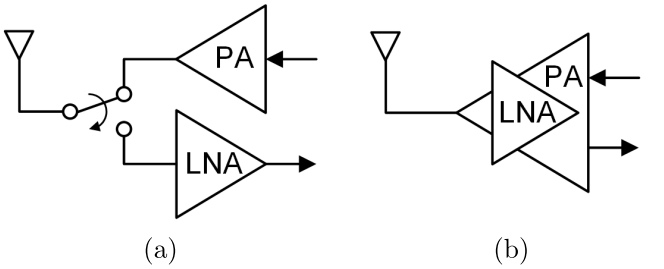

Fig. 1. TDD front end. (a) Conventional. (b) Proposed.

front-end balun. Section II gives an overview of the challenges of conventional integrated TRSW designs, and then describes our proposed solution. Section III delves into the design of the system's front-end transformer, while Section IV describes the implementation of the shared PA/LNA core. Section V summarizes the top-level TDD system implemented for this paper, and Section VI presents measurement results. Finally, Section VII concludes this paper.

II. INTEGRATED TRSWS AND PROPOSED TECHNIQUE

A. Conventional Integrated TRSWs

A conventional T/R switch is shown in Fig. 2(a). The active port—either TX or RX—connects to antenna through a series switch, while the inactive port is grounded with a shunt switch. Device gates are floated to maintain constant V_{GS} in the presence of large PA signal swings. For low IL, large series switches are needed to provide low series R_{ON}. However, for integrated TRSWs on low-resistance silicon, there is signal leakage through the switch's large parasitic capacitances to the substrate, shown in Fig. 2(b), which degrades IL and limits high frequency performance [13], [14]. When the series switch is OFF, its large C_{DS} limits isolation as well.

When the TX port is active, shown in Fig. 2(c), the off devices M2 and M3 must withstand the full TX signal swing across their drain-to-source junctions. M3 is often omitted when sufficient TX isolation is obtained with M1 alone [15] or with high PA output impedance (M1 can also be omitted in this case) [16]. M2, on the other hand, must utilize series-stacked transistors as shown in Fig. 2(d) to accommodate TX voltage levels [16]–[18]. The total voltage amplitude splits across each device in the stack, so that V_{DS} of any one device is within safe limits. This series-stacked topology enables greater power-handling in integrated TRSWs, but suffers from higher series R_{ON}, larger area, and higher parasitic capacitances.

Many TDD systems eliminate the challenging RX series switch altogether by absorbing its function into the LNA input match network [15], [19], [20], illustrated in Fig. 2(e). High power-handling capability and low loss are achieved by attenuating the TX signal swing across passive components rather than series transistors. This technique is inherently narrow-band, however, as it depends on high-Q resonance of the LC tank to present a high impedance and provide strong RX isolation. For wideband functionality, a transformer-based TRSW was proposed in [21] and illustrated in Fig. 2(f). Two transformers are stacked in series, one each for TX and RX ports, and the RX input and TX output are power-combined at the antenna port. This topology also suffers from high IL, however, as the TX and RX transformers, along with their shunt switches, de-Q each other.

Table I presents a summary of published integrated TRSWs. TDD co-existence with high-performance integrated TRSWs have thus far been limited to narrow-band systems serving 2.4-GHz BT and WLAN applications. These works rely on high-Q resonance and cannot be readily adapted for wide-band or reconfigurable radio applications. Wideband solutions have incurred higher loss, demonstrating ILs of $\sim$1$-$1.5 dB for standalone switches [17], [18], $\sim$2 dB when integrated in a transceiver [16], and $\sim$2.5 dB at higher frequencies above 5 GHz [21].

B. Proposed PA to LNA Transformation

Given the challenges of realizing high-performance wide-band, integrated TRSWs, we propose eliminating switches in the signal path altogether and instead re-using the PA as an LNA during receive mode. Mixed-signal polar transmitters employing current-switching PAs have demonstrated good power and efficiency performance at gigahertz frequencies [22]. Fig. 3(a) shows a typical inverse class-D current-switching PA. Transistors $M_{1,2}$ are the switched PA input devices, and $M_{3,4}$ are cascodes to support high PA output power. This topology of an input pair plus a cascode pair is identical to a cascode common-gate LNA, and we exploit this similarity to transform the PA into an LNA.

Fig. 3(b) shows the same structure in an LNA mode. Supply and ground have been flipped, as have the source and drain

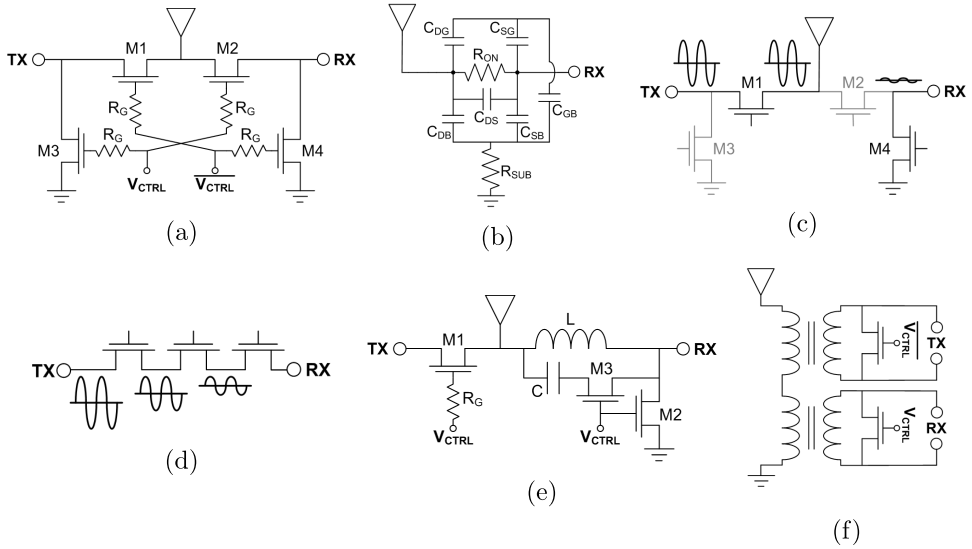

Fig. 2. Conventional integrated TRSWs. (a) Series–shunt topology. (b) Series switch parasitics. (c) TRSW in TX mode. (d) Series-stacked switch. (e) Resonance topology. (f) Transformer topology.

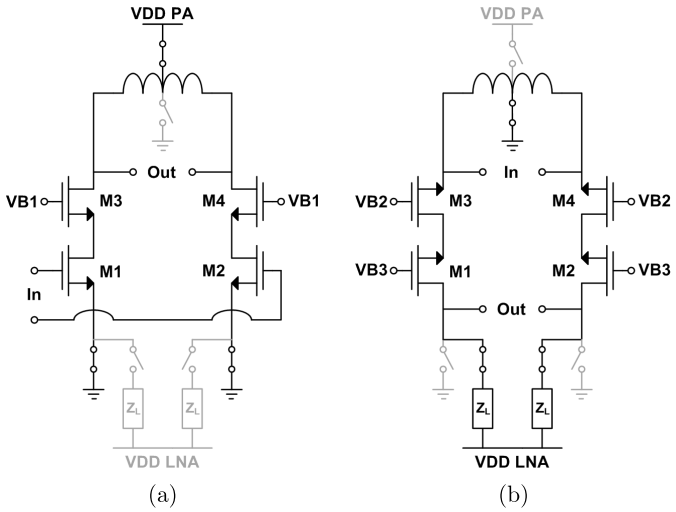

Fig. 3. PA/LNA transformation. (a) PA mode. (b) LNA mode.

of all transistors. Transistors $M_{3,4}$ are now the LNA input devices, and their source—formerly their drain and the PA output node—is now the LNA input node. Transistors $M_{1,2}$ are LNA cascodes, and their drain—formerly source in PA mode—is now the LNA output node and connected to an LNA load and supply.

The PA has thus been transformed into an LNA by using only DC power switches. The PA output and LNA input share a single port, which is connected directly to the PA and LNA devices without any series switches. There is no longer an idle PA or LNA block to isolate during either TX or RX modes, and the LNA output is grounded during TX mode, isolating any RX blocks following the LNA. Since the PA is necessarily designed to withstand its own output power, there are also no parts of the circuit that require special techniques and processes, such as stacked switches and isolated wells, to tolerate high PA signal swings.

III. Front-End Transformer Design

Front-end passive networks are a critical aspect of both PA and LNA design. Conventionally, PA output transformers provide a load impedance lower than the 50Ω antenna in order to reduce voltage swing at the PA drain for a given output power. Low-voltage swing is desirable for compatibility with the low supply and low breakdown voltages of modern CMOS devices. In contrast, LNAs are input impedance matched to 50Ω. A PA transformer that lowers antenna impedance would also attenuate signal voltage at the LNA input and severely degrade NF. In this paper, the PA and LNA's different impedance match requirements are accommodated using transformer-based power combining.

A. Stacked Transformer for Impedance Co-Design

Transformer-based power combining has been used to boost PA efficiency in power backoff regions by dynamically modulating PA load impedance [23], [24], and we utilize that impedance modulation property to provide PA/LNA co-match. Fig. 4(a) shows a transformer power combiner in PA mode. Two identical sub-PAs drive two identical stacked 1:1 sub-transformers. The load impedance seen by each sub-PA is $50\Omega/2 = 25\Omega$, which is sufficiently low for providing >20 dBm output power from modern CMOS supply voltages. A higher number of sub-transformers could be stacked to achieve even lower PA load impedance [25].

In prior work, impedance was reconfigured by shorting a sub-transformer [24], and Fig. 4(b) demonstrates how a 50Ω impedance co-match for the LNA could consequently be achieved. However, the shorted sub-transformer degrades the inductor Q of the remaining sub-transformer and contributes extra front-end IL for the LNA.

In this paper, instead of shorting the bottom sub-transformer, we re-use it to enhance performance in LNA mode, while maintaining 50Ω impedance match. Since the two sub-transformers are already stacked in series, we can treat them as

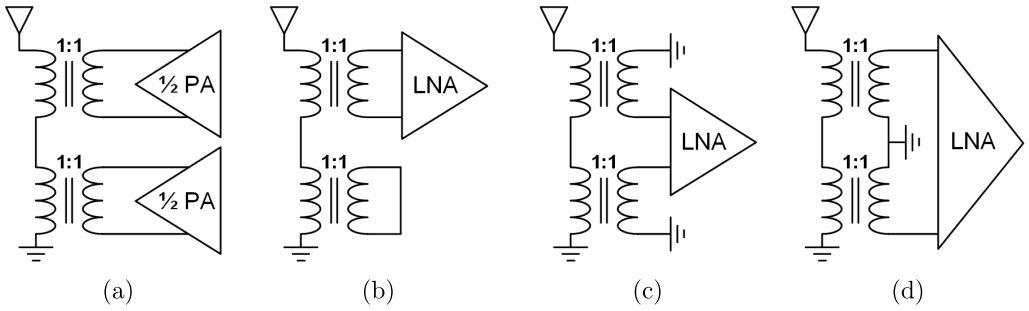

Fig. 4. Front-end transformer. (a) PA mode. (b) LNA mode with shorted sub-transformer. (c) LNA mode with combined transformer in inverting configuration. (d) LNA mode with combined transformer in non-inverting configuration.

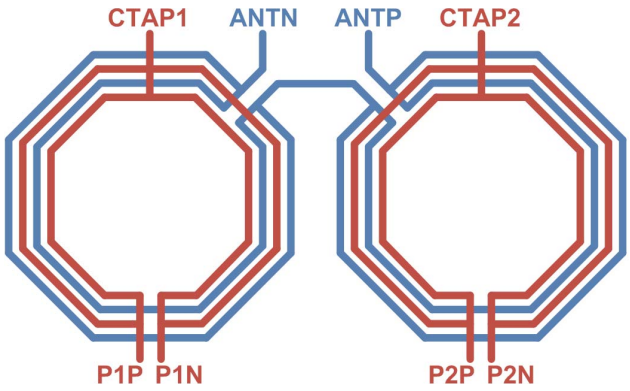

Fig. 5. Layout implementation of stacked transformer.

TABLE II
TRANSFORMER PARAMETERS

	L (nH)	Q	k
1:1 sub-xfmr	0.7	14.4	0.83
Ideally stacked 1:1 sub-xfmr	1.8	11.3	0.87
Dual loop layout	1.7	10.4	0.85
Full stacked xfmr implementation	1.8	9.6	0.81

a single, larger 1:1 transformer, as shown in Fig. 4(c) or (d). The resultant combined transformer has doubled inductance compared with Fig. 4(b), which lowers tank Q and improves wideband performance. Furthermore, this improvement was gained with no overhead or modifications to PA mode. The center tap of the combined transformer, on either side of the LNA in Fig. 4(c) or in the center in Fig. 4(d), is switched to ground using existing PA devices.

B. Transformer Implementation

Fig. 5 illustrates the implemented stacked transformer, composed of two mirrored 1:1 sub-transformers. To minimize IL, first, single-turn octagons are chosen for optimal inductor Q. Second, each coupled inductor has two parallel loops, giving larger effective metal width, improved coupling, and more uniform current distribution at RF frequencies [22]. Finally, all primary and secondary windings use two strapped thick metal layers. Each sub-transformer has 150-μm inner radius, 10-μm trace width, and 2-μm trace gap, and the two sub-transformers are separated by 20 μm. The transformer is implemented over NTN substrate.

Integrand EMX software was used to verify transformer performance. Each 1:1 sub-transformer has simulated parameters $L = 700$ pH, $Q = 14.3$, and $k = 0.83$, and the combined stacked transformer has parameters $L = 1.8$ nH, $Q = 9.6$, and $k = 0.81$. When two sub-transformers are combined, even ideally in schematic, there is significant Q degradation due to lowered self-resonance frequency (SRF) as both L and parasitic capacitance are doubled. Furthermore, Q degradation and k degradation are incurred from magnetic coupling between the two sub-transformers in an implemented dual loop layout, and from additional routing between the two loops as well as to the chip's antenna pads. Table II summarizes these transformer parameters.

The inverting and non-inverting transformer configurations for LNA mode, illustrated in Fig. 4(c) and (d), respectively, are functionally identical. However, there arises significant performance difference when the effects of interwinding capacitances and SRF are included. The transformer's interwinding capacitances are subject to Miller effect, and can appear larger or smaller depending on if they appear between the signals of equal or different strengths, and of equal or opposite polarity. To analyze the difference, we construct an SRF model for a 1:1 sub-transformer, shown in Fig. 6(a). Only transformer inductance and interwinding capacitance are included for simplicity, and front-end components that do not contribute to SRF such as antenna and LNA input resistance are not included in the analysis. Transformation ratio $n \approx 1/k$ for a 1:1 transformation, reflecting non-ideal coupling.

The 1:1 SRF model is then applied to the stacked transformer in inverting and non-inverting configurations, shown in Fig. 6(b) and (c), respectively. Both configurations are biased as baluns for LNA mode operation. In inverting configuration, this biasing forces $v_p = nv_1$ and $v_n = n(v_1\text{-}v_2)$ in Fig. 6(b). In non-inverting configuration, the biasing forces $v_p = n(v_2\text{-}v_1)$ and $v_n = -nv_1$ in Fig. 6(c). Equations (1) and (2), shown at the bottom of the next page, give the resultant impedance seen from the single-ended antenna port.

To demonstrate the relative difference in SRF between the two configurations, we can make the approximation $n \approx 1$. Equations (1) and (2) subsequently reduce to the more intuitive

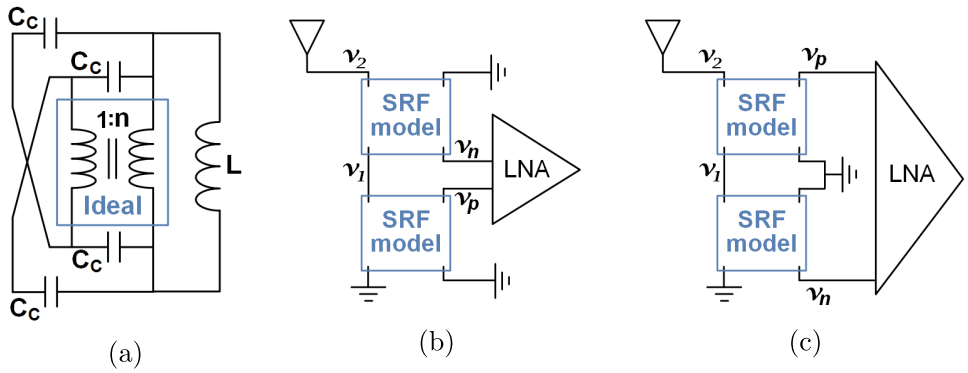

Fig. 6. SRF models for (a) Single 1:1 sub-transformer, (b) inverting stacked transformer, and (c) non-inverting stacked transformer.

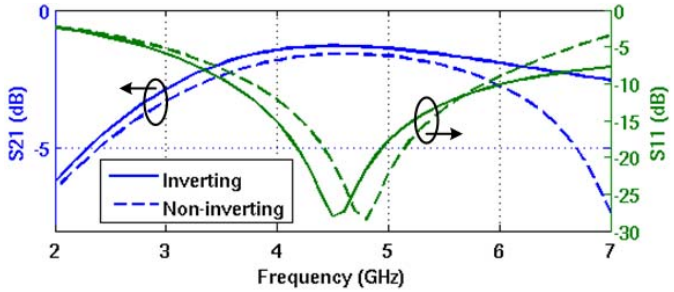

Fig. 7. Simulated S21 and S11 of stacked transformer in LNA mode.

forms

$$Z_{\text{INV}} \approx \frac{2sL}{1+10s^2LC_C} \tag{3}$$

$$Z_{\text{NON-INV}} \approx \frac{2sL(1+6s^2LC_C)}{(1+10s^2LC_C)(1+2s^2LC_C)}. \tag{4}$$

Equation (3) is the frequency response of an inductor with inductance $2L$ and SRF, $\omega_{\text{SRF}} = (1/(10LC_C))^{1/2}$. Equation (4) gives the same inductance and SRF, but with an additional zero at $\omega_Z = (1/(6LC_C))^{1/2}$, which is 1.3× SRF and forms a doublet with it. Fig. 7 plots simulated S21 and S11 of the stacked transformer in both configurations. With non-inverting configuration, degradation at the upper band edge from the doublet is apparent. Furthermore, IL across the entire band, including peak IL at midband, is degraded as well. Thus, in LNA mode, we operate the stacked transformer in the inverting configuration of Fig. 4(c). In PA mode, the two sub-transformers are separately driven, and inverting versus non-inverting coupling does not matter. Simulated IL of the stacked transformer in both PA and LNA modes is 1.3 dB. The IL achieved is comparable to the 1.3–1.5-dB PA output transformer IL of previous works [22]–[24].

IV. Shared PA/LNA Core

A. PA Core

Fig. 8(a) and (b) show the schematic and layout of the unit inverse class-D PA cell. Each cell consists of a digitally switched pseudo-differential pair, cascode devices to provide robustness for high output power, and buffers to locally regenerate the inputs to each cell. Both the input and cascode transistors are thin-oxide devices, and cascode gates are biased at 1.2 V. For higher-power applications requiring thick-oxide cascode devices, those same thick-oxide devices would have to be re-used as the LNA input devices in this paper's proposed TRSW scheme.

In this design, since thin-oxide devices can tolerate V_{GD} and V_{DS} of up to $2V_{\text{DD}}$s AC, each PA cell is robust up to 3.6-V peak drain voltage swing. Assuming a load resistance of 25 Ω, this corresponds to 24-dBm output power per sub-PA and 27-dBm total. However, in practice, the maximum tolerable output power will be about 4–5 dB lower due to non-idealities, such as finite ON resistance of the PA devices, transformer loss, harmonic distortion, and asymmetric power combining.

Fig. 9(a) illustrates simulated drain current and voltage of the implemented PA. The PA load impedance is well-controlled at only the fundamental frequency and not higher harmonics, which causes the current and voltage waveforms to deviate from ideal inverse class-D characteristics. Nevertheless, overlap time between current and voltage is low, and sufficient drain efficiency is maintained. Fig. 9(b) shows simulated voltage at maximum P_{OUT} at the stacked transformer ports P1P, P1N, P2P, and P2N. Due to the balun configuration of the stacked transformer, there exists some asymmetry from the two sub-transformers. However, the imbalance is small and peak drain voltages remain well within robustness limits.

The 8-bit PA consists of 15 thermometer cells (T0–T14) representing its upper four bits and four binary cells (B0–B3) for the lower four bits. Thermometer cells incur a large

$$Z_{\text{INV}} = \frac{2sL}{n^2} * \frac{(s^2CL/n^2)(n^2-n+1)+1}{4(s^2CL/n^2)^2(n^4+2n^2+2)+4(s^2CL/n^2)(n^2+2)+1} \tag{1}$$

$$Z_{\text{NON-INV}} = \frac{2sL}{n^2} * \frac{(1/2)(s^2CL/n^2)(3n^2+4n+5)+1}{2(s^2CL/n^2)^2(n^4+n^3+4n^2-n+5)+3(s^2CL/n^2)(n^2+3)+1} \tag{2}$$

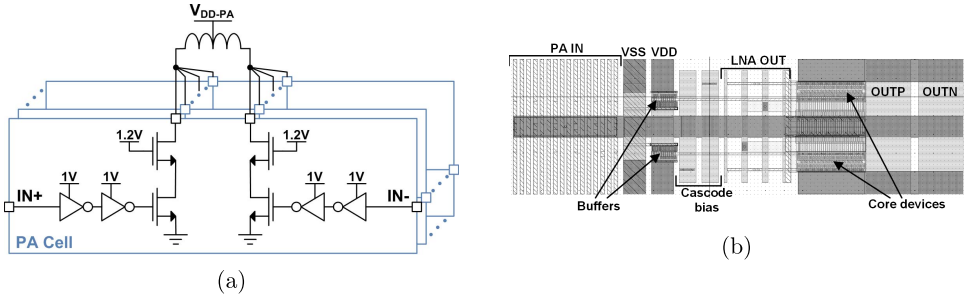

Fig. 8. PA cell. (a) Schematic. (b) Layout.

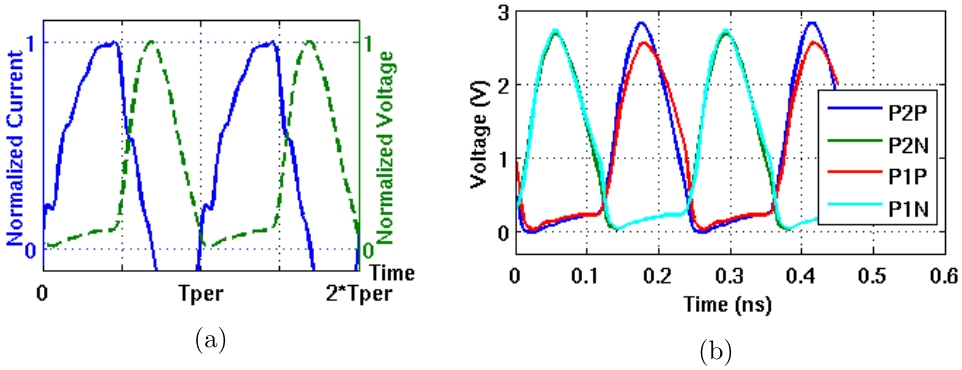

Fig. 9. Simulated PA transient waveforms. (a) Normalized drain current and voltage. (b) Drain voltage at stacked transformer ports.

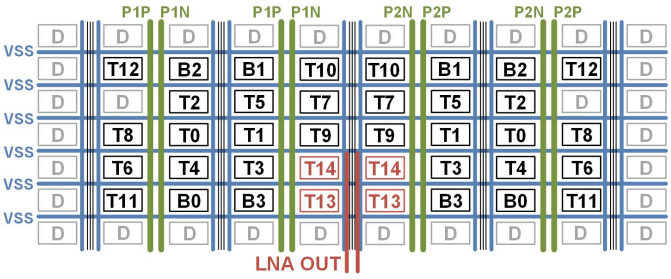

Fig. 10. Layout diagram of full PA core.

area penalty but provide improved DNL performance, and a segmented thermometer/binary architecture strikes a balance between area and mismatch. Fig. 10 shows the full PA core layout containing both sub-PAs. The two sub-PAs are mirrors of each other, and within each sub-PA, the lower thermometer cells are placed in the center, while higher cells are placed outwardly in a pattern that would average out deterministic variation. Although digital PAs are linearized with predistortion, systematic mismatch should still be minimized to a correctable level. The LNA uses the highest two thermometer cells, T13 and T14, of each sub-PA. These four cells are therefore placed in the center adjacent to each other, allowing the LNA to straddle the two sub-PAs symmetrically with minimal extraneous routing.

As illustrated in both Figs. 8(b) and 10, vertical routing channels between PA cells alternate between wide PA output traces, and thinner traces less sensitive to parasitic resistance, such as PA input, cascode bias, and VDD for the local buffers. The LNA output traces are active only in the LNA re-use cells. PA ground is routed as a mesh to minimize resistance. A summary of PA design parameters is presented in Table III.

B. PA Re-Use LNA

Fig. 11 illustrates the LNA architecture. The LNA, due to PA re-use, is by necessity a cascoded common gate (CG) topology. Capacitive cross-coupling at the LNA input boosts g_m to help noise and power performance. The effective transconductance G_M of a capacitively cross-coupled CG LNA is given in (5). The intrinsic gate-to-source capacitance of the LNA input device is $C_{\rm GS}$, and any parasitic capacitance to ground at the input device gate node is represented by C_{G0}. The base noise factor, with only input device noise included and under input match condition $G_M R_S = 1$, is given in (6)

$$G_M = g_m * \left(\frac{2C_C + C_{G0}}{C_C + C_{\rm GS} + C_{G0}} \right) \tag{5}$$

$$F = 1 + \frac{\gamma}{G_M R_S} \left(\frac{g_m}{G_M} \right) = 1 + \gamma \left(\frac{g_m}{G_M} \right). \tag{6}$$

Conventionally, $C_C \gg C_{\rm GS}$ and $C_C \gg C_{G0}$ are chosen to achieve maximum g_m-boost possible. However, this design is constrained by the amount of extra capacitance (in the form of C_C) the PA can absorb into its output tank. LNA $C_{\rm GS}$, consisting of the cascode gate capacitance of two PA thermometer cells, is about 100 fF, and $C_{G0} \approx 200$ fF due to parasitics and overhead from PA/LNA mode switching. Fig. 12 plots calculated base NF and normalized bias current as a function of C_C. In this paper, $C_C = 1$ pF is chosen to capture the

TABLE III
PA AND LNA DESIGN PARAMETERS

PA		LNA	
$(W/L)_{INPUT,CELL}$	48μm/60nm	$(W/L)_{INPUT}$	96μm/60nm
$(W/L)_{CASCODE,CELL}$	48μm/60nm	$(W/L)_{CASCODE}$	96μm/60nm
$(W/L)_{INPUT,SUB-PA}$	765μm/60nm	C_C	1pF
$(W/L)_{CASCODE,SUB-PA}$	765μm/60nm	C_L	250fF
$C_{DRAIN,SUB-PA}$	1.4pF	L_L	4.5nH
$L_{XFMR,SUB-PA}$	700pH	R_L	120Ω

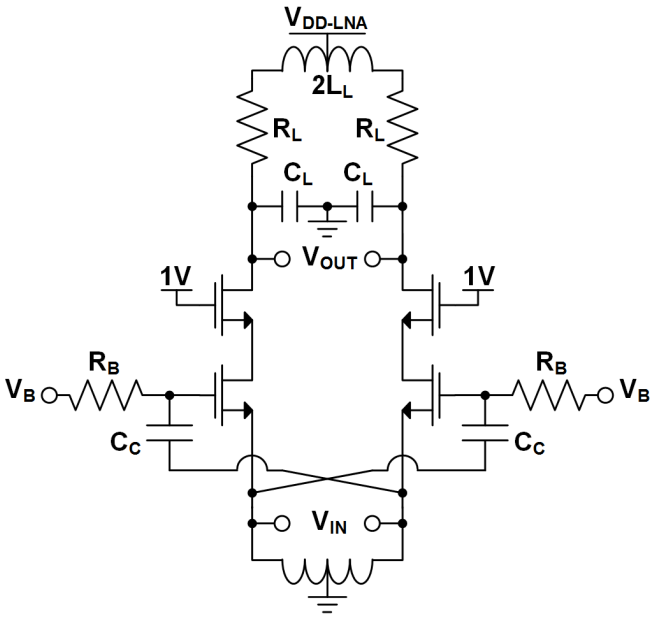

Fig. 11. Schematic of LNA architecture.

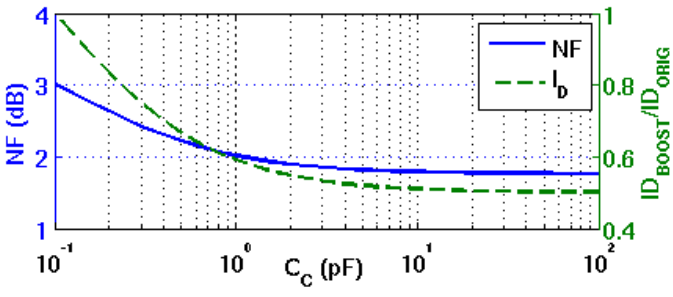

Fig. 12. Base NF and normalized bias current of capacitively cross-coupled CG LNA as a function of C_C.

majority of benefit from g_m-boost, while being small enough to be naturally absorbed into the PA output tank.

The LNA uses a shunt-peaking load to offset *RC* rolloff at gigahertz frequencies, where C_L in Fig. 11 is composed of the intrinsic and parasitic capacitances at the LNA output node. In addition to bandwidth extension, the shunt-peaking load is further used to peak the frequency response above the LNA's low-frequency gain to provide additional gain at target frequencies. The impedance of the shunt-peaking load, shown

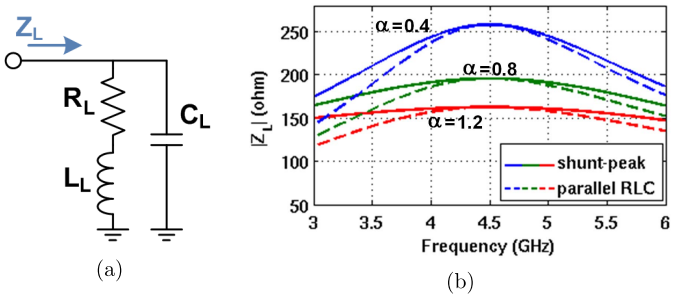

Fig. 13. LNA shunt-peaking load. (a) Schematic. (b) Frequency response for various values of α and bandwidth comparison with parallel RLC loads of equal impedance.

in Fig. 13(a), is

$$Z_L = (sL_L + R_L)\| \left(\frac{1}{sC_L}\right) = \frac{sL_L + R_L}{s^2 C_L L_L + sC_L R_L + 1}. \quad (7)$$

When gain-peaking from the shunt-peaking load exists, the peak frequency and its corresponding impedance are given below in (8) and (9), in which $\alpha = R_L^2 \times C_L/L_L$. The noise factor of the LNA, including load noise at peak frequency $\omega = \omega_o$, is given in (10)

$$\omega_o^2 = \frac{1}{L_L C_L} * (\sqrt{1+2\alpha} - \alpha) \quad (8)$$

$$|Z_{L,\text{peak}}| = R_L * \sqrt{\frac{1}{2\alpha\sqrt{1+2\alpha} - \alpha(2+\alpha)}} \quad (9)$$

$$F = 1 + \gamma \left(\frac{g_m}{G_M}\right) + \frac{4}{G_M R_L}\left(\frac{\alpha}{\sqrt{1+2\alpha}}\right). \quad (10)$$

Smaller α corresponds to higher gain and lower noise, while larger α corresponds to wider bandwidth. For a given α and bandwidth, larger C_L results in lower gain. Thus, although shunt-peaking alleviates bandwidth restrictions from *RC* rolloff, it is still advantageous to minimize C_L, the parasitic and load capacitances at the LNA output, as much as possible. For similar values of C_L, center frequency and gain, using a shunt-peaked load to gain-peak enables a more wideband response than the parallel RLC load typically used in narrowband LNAs. Fig. 13(b) plots the frequency response of $|Z_L|$ for various values of α; the responses of equivalent parallel RLC loads are also shown for comparison. As a balance between gain, bandwidth, and NF, we use $\alpha \approx 0.8$ and $R_L \approx 120\ \Omega$.

As shown in Fig. 11, the shunt-peaking inductor is implemented as a single center-tapped inductor for area efficiency. A low Q, multi-turn square inductor is used, and its parasitic resistance is absorbed into R_L. The differential inductor, consisting of $2{*}L_L$, has five turns and 60-μm inner radius, 4-μm trace width, and 4-μm trace gap. The thin trace width and large gap were used to lower parasitic capacitance and achieve adequate SRF. The implemented differential inductor has simulated $L = 7.7{\sim}12.7$ nH from 3 to 6 GHz, $Q = 5.7{\sim}7.0$, and SRF = 8.5 GHz. A summary of LNA design parameters is presented in Table III.

The LNA is sensitive to parasitics at its input node, and consequently, a significant portion of the LNA's total NF arises from front-end passive components. The contribution

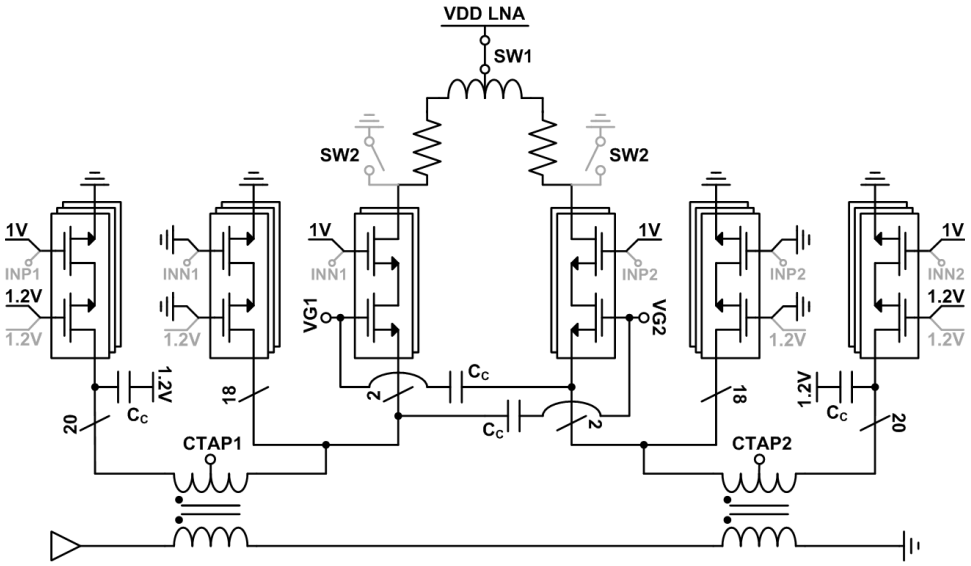

Fig. 14. Schematic of PA/LNA core with front-end transformer. LNA mode is highlighted while PA mode is in gray.

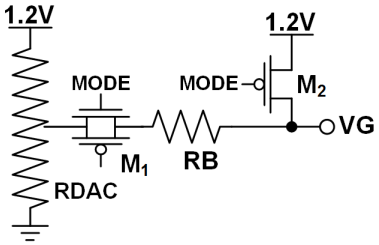

Fig. 15. Schematic of LNA gate bias network.

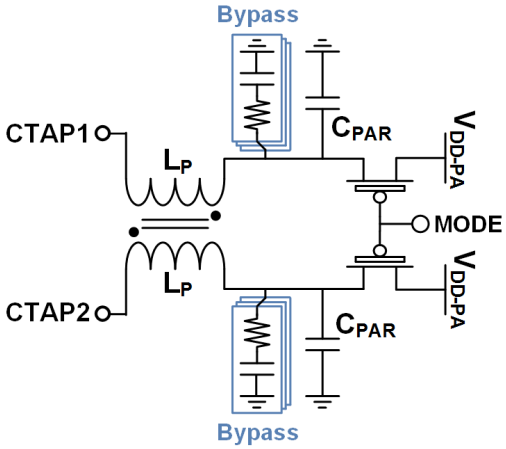

Fig. 16. Schematic of PA supply switch network.

of transformer parasitic resistance R_P to LNA NF is given in (11), where $Q_L = \omega_o L/R_P$ is transformer inductor Q, R_S is input resistance, and $Q_{\text{TANK}} = R_S/\omega_o L$

$$F = 1 + \gamma \left(1 + \frac{Q_{\text{tank}}}{Q_L}\right)^2 + \frac{R_P}{R_S}(1 + Q_{\text{tank}}^2). \qquad (11)$$

Due to the Q limitations of on-chip transformers, the Q_{TANK}/Q_L ratio in practice can be quite large (>0.2), and the square terms cause significant noise even with $R_P \ll R_S$. For these reasons, the front-end transformer contributes a simulated 1.2 dB to total LNA NF, due to both R_P noise and IL. In addition, the transformer center tap for the LNA is switched to ground with PA cells as described in Section III-A. The ON resistance of these cells, 0.6 Ω in total, contributes a further 0.5 dB to LNA NF.

C. PA/LNA Mode Switching

Fig. 14 illustrates the full PA/LNA core with the stacked transformer. The LNA straddles the two sub-transformers and uses half of two thermometer cells per sub-PA. The unused PA branches adjacent to the LNA (18 half-cells per sub-PA) are turned off and act as capacitance at the LNA input. The side PA branches (20 half-cells per sub-PA) are switched on to create the LNA's input DC connection to ground. The two C_C in the center are the g_m-boosting capacitors for the LNA, and the outer two C_Cs exist so that the PA sees a symmetric load. The sub-transformer center tap nodes $\text{CTAP}_{1,2}$ are connected to PA supply during PA mode, and in LNA mode, they are disconnected and are high impedance. The PA supply switch will be described in Section IV-D.

In PA mode, the top row of transistors are PA input devices, driven by a switching input or turned off depending on amplitude data. In LNA mode, logic in the PA driver forces the PA inputs to ground or 1 V (VDD of the PA driver) depending on cell function. This mechanism will be described in more detail in Section V. The bottom row of devices are PA cascodes, all biased at 1.2 V in PA mode. In LNA mode, aside from the LNA cells, the cascodes are driven to ground or 1.2 V with additional custom logic that uses $V_{\text{DD}} = 1.2$ V.

Aside from PA/LNA mode switching that occurs through digital logic, as well as the PA supply switch, there are three additional discrete switches in the system. SW1 and SW2, shown in Fig. 14, select between the LNA load for the LNA branches versus PA ground. The LNA supply switch SW1,

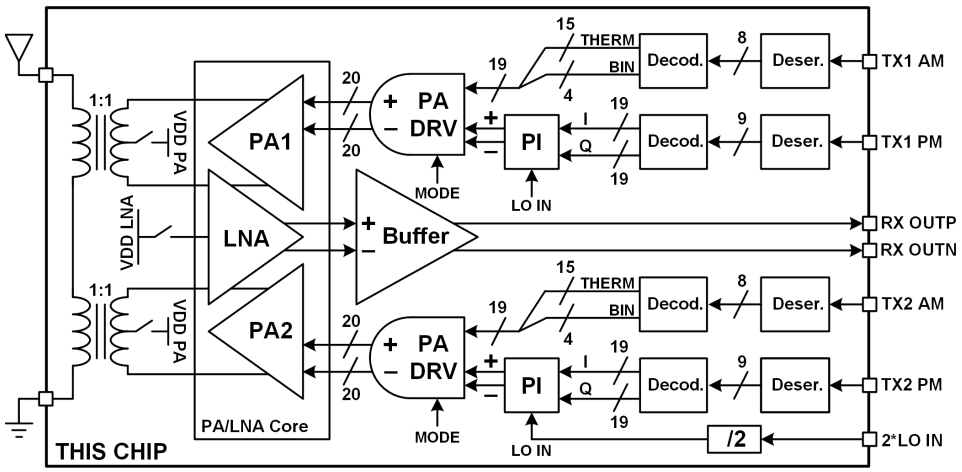

Fig. 17. Block diagram of system top level.

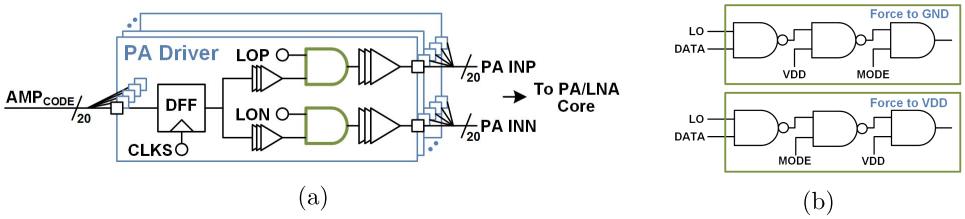

Fig. 18. PA driver. (a) Block diagram of base cell. (b) Added logic for T/R mode switching.

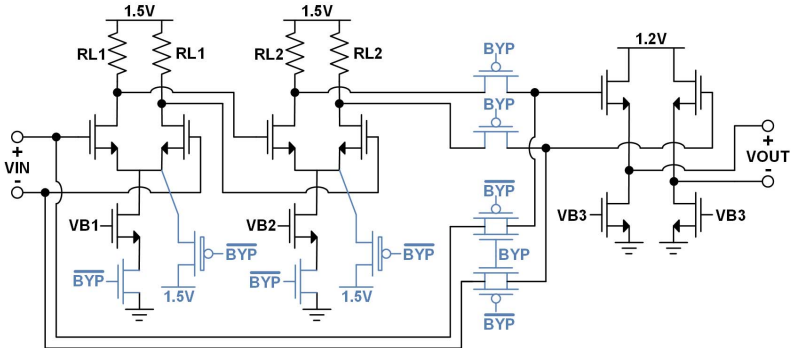

Fig. 19. Schematic of RX output buffer.

at the center tap of the LNA's shunt-peaking inductor, is outside of the signal path and can be made arbitrarily large with no adverse effect on performance.

The PA ground switch SW2, however, occurs at the LNA's output node and must be sized relatively small to minimize loading. The implemented SW2 has simulated $R_{\mathrm{ON}} = 6.3\ \Omega$ and $C_{\mathrm{OFF}} = 51$ fF. Although SW2 R_{ON} is comparable to the ON resistance of a PA cell's input and cascode devices, the resulting degradation to PA performance is actually negligible, since SW2 exists only in the highest two PA thermometer cells, when PA output power is already relatively saturated. In layout, SW2 is placed inside the PA cell to avoid long routing traces and to minimize resistance to ground.

The third "switch" encompasses the bias network for $\mathrm{VG}_{1,2}$, shown in Fig. 15. In PA mode, VG is pulled up to 1.2 V as PA cascode bias. The pull-up switch M2 must be moderately large to create a strong bias that suppresses gate swing from C_C. However, the switch's C_{OFF} loads the LNA input gate and reduces its g_m-boost. M2 has simulated $R_{\mathrm{ON}} = 3.6\ \Omega$ and $C_{\mathrm{OFF}} = 160$ fF, and it has negligible effect on PA performance. In LNA mode, VG is biased through M1 and a large resistor RB to allow voltage swing from g_m-boosting. A 6-bit resistive voltage DAC is used to generate LNA bias voltage for ease of tunability during testing.

D. PA Supply Switch

A schematic of the on-chip PA supply switching structure at $\mathrm{CTAP}_{1,2}$ is shown in Fig. 16. For good PA drain efficiency, the PA supply switches must be large with extremely low R_{ON}. Otherwise, IR drop across the switch effectively lowers the supply voltage and reduces PA output power, while additional DC power consumed by the switch degrades efficiency. In LNA mode, however, the switch has a proportionally large parasitic capacitance C_{PAR} at the sub-transformer center tap

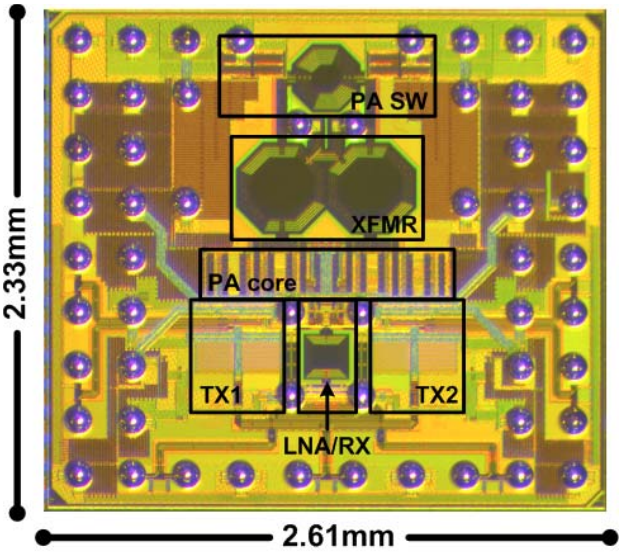

Fig. 20. Chip micrograph of implemented TDD system.

nodes. The resonance frequency of C_{PAR} with transformer inductance could easily fall in or below the band of interest, severely degrading LNA performance.

To mitigate this effect, a choke inductor L_P is inserted between the PA supply switch and $\mathrm{CTAP}_{1,2}$, isolating C_{PAR} from the front-end transformer. This solution is wideband and insensitive to exact C_{PAR} value. In fact, a larger C_{PAR} from a larger switch, layout parasitics, or other sources become beneficial, as it would tune out a smaller fraction of L_P, leaving its remaining inductance to be a stronger choke.

As shown in Fig. 16, the two choke inductors are further coupled into a transformer. With coupling, the effective center tap inductances in PA and LNA modes become

$$L_{\mathrm{EFF-LNA}} = L_P * (1 + k)$$
$$L_{\mathrm{EFF-PA}} = L_P * (1 - k). \tag{12}$$

In the LNA mode, the two CTAP nodes are differential, and the effective choke inductance at each CTAP is boosted due to transformer coupling. In PA mode, the two CTAP nodes are common mode and their choke inductances cancel. Since a low supply inductance is desirable for the PA, the coupling beneficially impacts both the PA and LNA modes. The supply transformer is designed for low resistance to minimize both degradations to PA efficiency and parasitic noise contributions to the LNA. The transformer is implemented on chip with three parallel loops per inductor and achieves simulated $L =$ 293 pH, $Q = 10.5$, and $k = 0.71$. The simulated effective inductances are 86 pH for PA mode and 555 pH for the LNA mode.

The implemented PMOS supply switch has post-extraction $R_{\mathrm{ON}} = 420\ \mathrm{m\Omega}$. With its drain capacitance no longer a concern, switch size is set by physical area and diminishing returns due to routing parasitics. The supply bypass capacitors for $V_{\mathrm{DD-PA}}$ are placed on the transformer side of the supply switch to maximize choke inductance, and a staggered *RC* bypass network similar to [26] is used. In simulation, the PA supply switching network degrades P_{SAT} by 1 dB and drain efficiency by 3.4%. In LNA mode, the supply network contributes −0.3 dB to gain and 0.1 dB to NF. These degradations compare favorably with the higher IL of conventional TRSWs from Table I. A summary of all PA/LNA mode switches and their effects on the PA and LNA performances are presented in Table IV.

TABLE IV
SUMMARY OF PA/LNA MODE SWITCH EFFECTS

Switch	Effect on PA	Effect on LNA
LNA supply (SW1)	Negligible	Negligible
PA ground (SW2)	Negligible	Contributes to C_{L} in Eq. 7
LNA gate (VG)	Negligible	Contributes to C_{G0} in Eq. 5
PA supply (CTAP)	P_{OUT}-1dB, η-3.4%	A_{V}-0.3dB, NF+0.1dB

V. SYSTEM IMPLEMENTATION

The PA re-use TDD front-end is embedded in a digital polar transmitter to demonstrate proof-of-concept. Fig. 17 shows a block diagram of the implemented system. We use the digital transmitter architecture from [24], which has an 8-bit amplitude modulator, 9-bit phase modulator, and two power-combining sub-PAs. Separate but identical TX paths are used for each sub-PA to reduce design time while allowing for potential tunability. For each sub-PA, AM and PM input data are deserialized and decoded. The eight amplitude bits resolve into 15 thermometer bits and four binary bits, each controlling a corresponding PA cell as in a DAC. The decoded phase bits control I/Q current DACs of a Gilbert-cell-based phase interpolator (PI) to generate a differential LO waveform at the desired PA output frequency and phase. The PA drivers then combine the PI's LO output with amplitude data to create the switching inputs that drive the cells of the PA core. The input LO is routed to the two TX chains driving each sub-PA using a resistive impedance-matched splitter.

Logic was inserted into the PA driver to enable PA/LNA mode switching. Fig. 18(a) shows a base PA driver cell, which is a simple AND operation between the PI output LO and amplitude code, and Fig. 18(b) illustrates the modifications for mode switching. In PA mode, when MODE = 1, the logic acts the same as the base cell and outputs the LO and amplitude code's AND result. In LNA mode, when MODE = 0, the bottom logic chain forces a steady VDD output while the top chain forces steady ground. Each PA driver cell uses the appropriate logic depending on the function of its corresponding PA cell in LNA mode. The two logic chains are delay-equalized with each other.

In RX mode, the LNA outputs are directly buffered off-chip for measurement, and a schematic of the RX buffer is shown in Fig. 19. The buffer consists of two common-source gain stages followed by a source follower output driver to provide 50-Ω output impedance. The gain stages exist to minimize the noise contribution of the output driver to system NF, and they are bypassed in LNA linearity measurements. The input node to the output driver selects between the output of the gain stages and the buffer input. In bypass mode, the gain stages are turned off, their tail current sources are disconnected, and

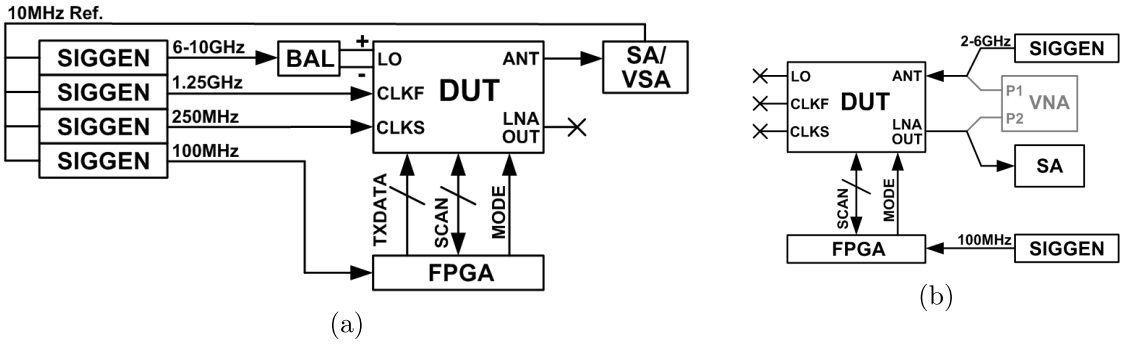

Fig. 21. Measurement setup. (a) PA mode. (b) LNA mode.

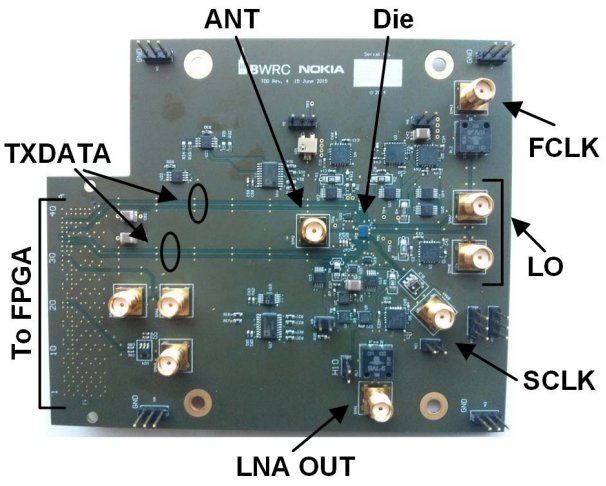

Fig. 22. Photograph of test PCB.

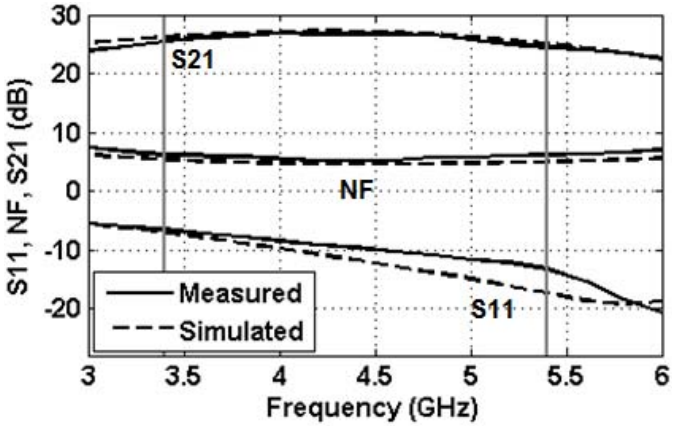

Fig. 23. Measured LNA performance across frequency.

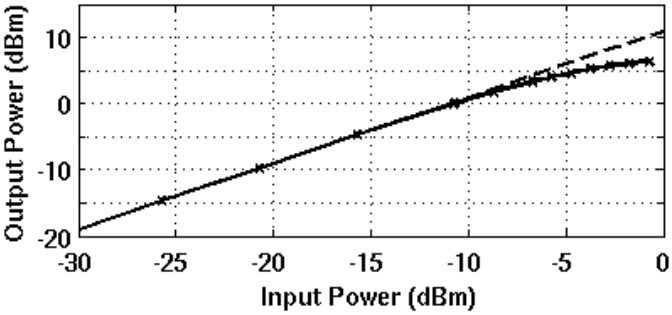

Fig. 24. Measured RX output power as a function of input power.

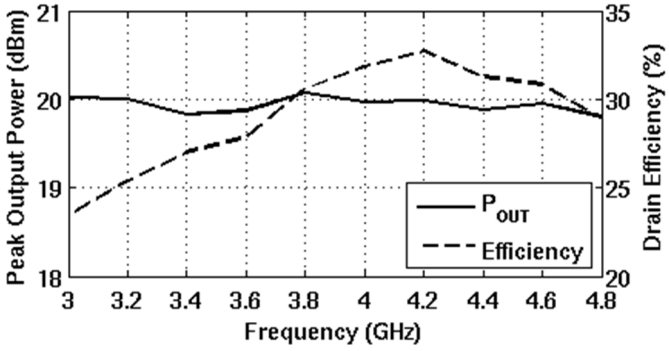

Fig. 25. Measured peak PA output power and peak drain efficiency across frequency.

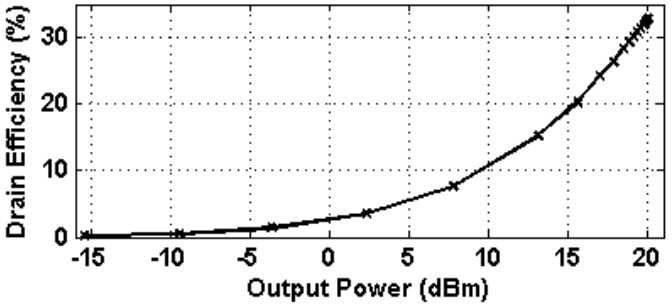

Fig. 26. Measured drain efficiency as function of PA output power.

their tail nodes are driven to VDD to prevent high voltage stress. In simulation, the RX buffer adds 0.3 dB to LNA NF in gain mode, and it does not limit LNA linearity in bypass mode.

VI. Measurement Results

A system prototype was fabricated in TSMC 65 nm GP, and a chip micrograph is shown in Fig. 20. The chip measures 2.31 mm × 2.61 mm, but is pad-limited. The core area is 1.8 mm^2. Assuming that the PA, LNA, and front-end transformer exist in comparable TDD front-ends, the area overhead used to implement T/R switching reduces to the PA supply switching structure, which has active area of 0.25 mm^2, including the supply transformer. All other mode switches are negligible in area in comparison.

The flip-chip die is attached directly to PCB with no intermediate package. High-frequency ports, such as the antenna, clocks, and TX data inputs are placed along the

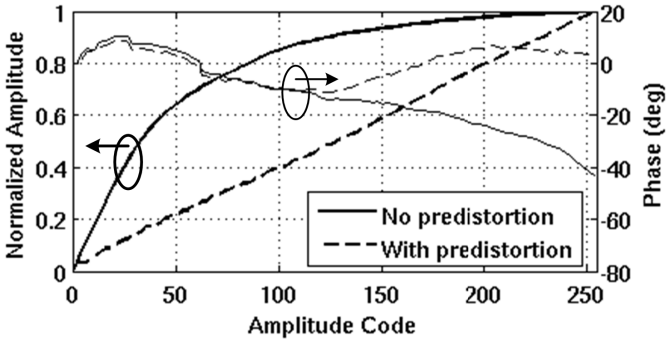

Fig. 27. Measured transmitter AM–AM and AM–PM performance across AM codes.

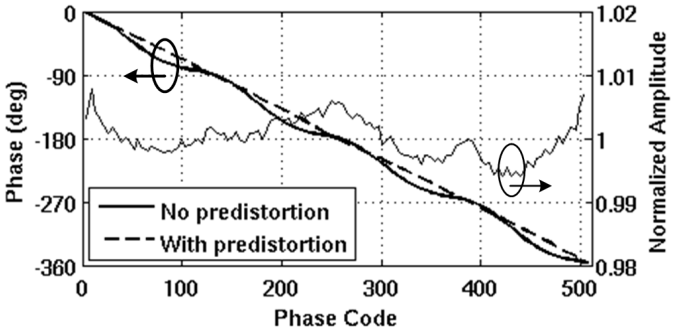

Fig. 28. Measured transmitter PM–PM and PM–AM performance across PM codes.

TABLE V
COMPARISON TABLE OF DIGITAL PA PERFORMANCE

	Chowdhury [22]	Ye [24]	Kuo [10]	This Work
Freq. (GHz)	2.25	2.2	1.2/2.2	4.2
Supply (V)	1	1.2	2.5	1.2
PA Psat (dBm)	22	23.3	27.1/24.7	20
PA Eff. (%)	44	43	52/40	32.7

perimeter of the chip, so that they are routed directly on PCB with top-layer traces. Interior pads not on the perimeter are routed with via-under-pads. Ground planes are voided under the SMA pads for all sensitive signals to reduce pad capacitance. The topmost ground layer is also voided under the transformer and inductor areas of the die to reduce leakage. On-board voltage regulators are used to provide the different PA, LNA, and digital supplies to the die.

Fig. 21 illustrates the measurement setup in PA and LNA modes. Control signals and TX data inputs are generated from a Xilinx VC707 FPGA board. A signal generator provides the 100 MHz reference clock for the FPGA. In PA mode, signal generators produce TX deserialization clocks (CLKF and CLKS) as well as the 2∗LO PA clock input. The deserialization clocks have on-board baluns while a 10-GHz SMA connector balun was used for the LO. The PA output is measured at the antenna port with a spectrum analyzer. All equipment, including the FPGA, share a common 10 MHz reference for timing alignment. A vector network analyzer and spectrum analyzer are used to perform LNA measurements. Fig. 22 shows the test PCB.

Cables and PCB traces have been de-embedded from all reported results. PCB trace loss was measured from two-port

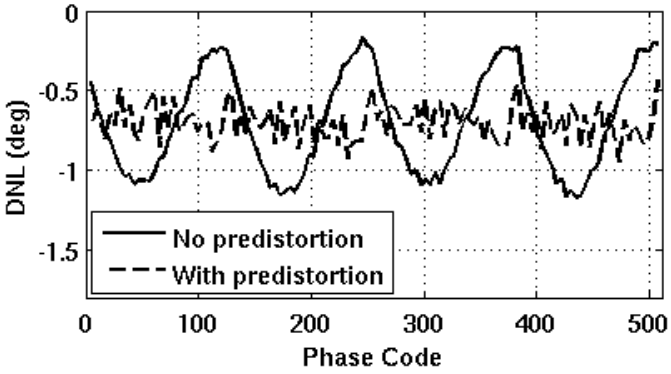

Fig. 29. DNL of measured PM–PM performance with and without pre-distortion.

re-creations of critical traces. Cable and trace loss are added directly to PA output power and LNA gain measurements, and they are de-embedded from LNA NF measurements using Friis's formula.

Fig. 23 shows measured LNA S11, S21, and NF across the frequency band of interest. Including the buffer in high-gain mode, the full RX path has peak gain of 26.8 dB and −3-dB bandwidth of 2.7 GHz. Based on simulations, the LNA's standalone gain is estimated to be about 17 dB. Measured noise figure, also including RX buffer, is 5.1 dB at its lowest point, and the NF +1 dB bandwidth is 2 GHz. LNA S11 reaches −10 dB at the midband frequency of 4.5 GHz. The LNA design targeted $S11 < -10$ dB across the band of interest, but S11 response became shifted due to pads, bonding inductance, and PCB vias and traces. Fig. 24 plots RX output power as a function of input power. The LNA's input P1dB, measured with the RX buffer in bypass mode, is −6.7 dBm. The LNA consumes 9 mA from 1.5 V.

Fig. 25 shows measured P_{SAT} and drain efficiency across frequency. With 1.2-V supply, the PA at 4.2 GHz achieves 32.7% peak drain efficiency at 20-dBm output power for a continuous-wave signal. Peak total efficiency accounting for total TX power consumption is 22%. Performance above 5 GHz was not measured due to limitations of the measurement setup related to difficulties of propagating a robust > 10-GHz 2*LO clock onto the chip. However, existing results indicate wideband PA frequency response similar to the LNA. Drain efficiency as a function of output power is shown in Fig. 26. Table V presents a comparison of PA performance to previously published digital PAs with similar architecture. The achieved efficiency is comparable to that of the other works combined with an IL ≈ 1-dB TRSW, while this work operates at greater frequencies.

Figs. 27 and 28 show the AM–AM, AM–PM, PM–PM, and PM–AM characteristics of the implemented transmitter, measured at 4.2-GHz carrier. The compressive AM–AM behavior and the AM–PM distortion are characteristics of digital PAs and can be linearized with pre-distortion. A measured AM–AM response after pre-distortion is also shown in Fig. 27. The four-quadrant curved PM–PM response is due to I/Q phase interpolation and can similarly be linearized with predistortion as shown in Fig. 28. Fig. 29 plots DNL of the measured PM–PM response both with and without

TABLE VI
COMPARISON TABLE OF INTEGRATED TRSW SYSTEMS

	Madan [18]	Fu [19]	Goswami [16]	Chen [27]	Yuksel [9]	This Work
Architecture	SW +LNA	SW +LNA	SW+PA +LNA	SW+PA +LNA	TX+RX	SW+TX +LNA
SW Topology	reso-nance	reso-nance	series-shunt	trans-former	distributed XCVR	PA re-use
Technology	180nm	32nm	45nm SOI	90nm	65nm	65nm
Freq. (GHz)	2.5	2.5	1.4-3.4[1]	5.2	0.3-1.5	3.4-5.4
LNA Gain (dB)	13	12	>14	15	32[2]	26.8[3]
LNA NF (dB)	3.0	3.5	2.8-6.0	3.2	7[2]	5.1-6.1
LNA P1dB (dBm)	-6	-5	-[4]	-13	-2[2]	-6.7
LNA Power (mW)	23.1	19.8	6.0	15.3	-	13.5
PA Psat (dBm)	-[5]	-[5]	27.6	25.9	19.5	20
PA Eff. (%)	-[5]	-[5]	30[6]	26.7[7]	18	32.7

[1]With frequency tuning. [2]Full RX chain. [3]With high-gain RX buffer.
[4]IIP3 = -7dBm [5]No PA in system. [6]Includes PA drivers. [7]PAE

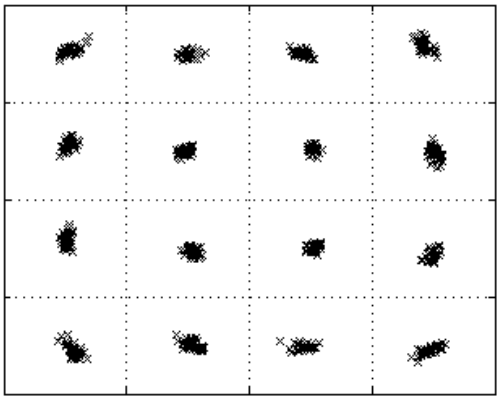

Fig. 30. Sample measured QAM16 constellation.

pre-distortion to present a magnified view of the effect of phase linearization. PM–AM distortion is negligible.

All predistortion is simply calculated by using lookup tables based on the measured results. Through the AM and PM code measurements, it has been demonstrated that the implemented transmitter is fully functional and capable of operating with modulated signals. As proof-of-concept for our TDD front-end, a QAM16 constellation measurement at 4.2 GHz and with 16.4-dBm average P_{OUT} is shown in Fig. 30. The constellation is generated from random input data, and it has EVM $= -27.7$ dB with PAPR $= 2.9$ dB.

A comparison table of T/R switching front-ends is presented in Table VI. This paper incurs somewhat higher LNA NF due to PA re-use, which compels the use of CG topology and input transformer that are avoided in other works. Nevertheless, this paper presents a wideband integrated TDD front-end without frequency tuning and including full TX, while achieving comparable performance to narrow-band systems.

VII. CONCLUSION

A TDD front-end implementing a substantially different PA re-use T/R switching technique has been presented. The transformation of a PA into a gigahertz wideband LNA was achieved while maintaining transmitter functionality and performance. Simultaneously, a wideband TDD front-end with integrated T/R switching, integrated balun, and no frequency tuning was demonstrated. TDD co-existence at RF frequencies has been achieved with no series RF switches in the signal path, and with only low-frequency mode control switches. The TDD system in the LNA mode achieves 2.7-GHz bandwidth, -6.7-dBm P1dB, and 5.1-dB NF. In PA mode, the system achieves $P_{\mathrm{SAT}} = 20$ dBm with 32.7% peak drain efficiency. This paper contributes a key innovation toward greater front-end integration and reconfigurability for modern and future multi-band radios.

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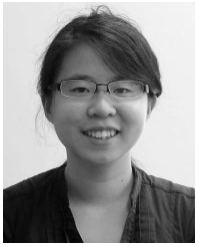

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