# An Interference-Resilient Wideband Mixer-First Receiver With LO Leakage Suppression and I/Q Correlated Orthogonal Calibration

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***Abstract*—A mixer-first receiver design in 28-nm CMOS is discussed. An embedded 5-bit mixer digital-to-analog converter provides wideband tuneability to enhance device matching and, hence, suppress the multiple local oscillator (LO) harmonics as well as to improve the overall image rejection (IR) performance. Two-stage baseband amplifiers support a 50-MHz baseband bandwidth, which covers the entire channel for long-term evolution non-contiguous carrier aggregation. The proposed design effectively reduce multiple LO harmonics down to below −62 dBm. The system achieves 2.6-dB noise figure, > 15-dBm out-of-band third-order input intercept point, and an IR ratio > 66 dB with 60-mW power, including five on-chip low dropout regulators.**

***Index Terms*—Carrier aggregation (CA), image folding, image rejection (IR), image rejection ratio (IRR), in-phase/quadrature-phase correlated orthogonal calibration (I/Q-COC), intra-band, local oscillator (LO) leakage, long-term evolution (LTE), mixer digital-to-analog converter (MxDAC), mixer-first receivers (RXs).**

## I. Introduction

DUE TO the scarcity of available wireless spectrum and never-ending demand for higher data rates, the concept of dynamic bandwidth allocation is gaining more traction. Some of the modern wireless standards such as long-term evolution advanced (LTE-A) [1] now have the capabilities to dynamically aggregate multiple frequency sub-channels to maximize spectral usage efficiency. Compared to other bandwidth reallocation techniques such as 802.11.ac's channel bonding, LTE-A's carrier aggregation (CA) is much more challenging for radio design since the sub-carriers might or might not be allocated in a continuous fashion. The receiver (RX) must be able to sense several desired and potentially weak signals in between strong undesired interferers. This results in unprecedented challenges on linearity and noise requirements in long-term evolution (LTE) RX design.

Even though various concepts of software-defined radio systems have been demonstrated with great flexibility and tuneability such as [2] and [3], they cannot meet the stringent bandwidth, linearity, and noise requirements imposed by LTE-A, as discussed in [4]. A more conventional solution for LTE CA [5] would dedicate one narrowband RX and one synthesizer to each of the subcarriers. However, it suffers from a large power and area overhead. Moreover, the system design requires careful frequency and layout planning to avoid local oscillator (LO) pulling, due to the poor frequency separation between different sub-channels. An alterative is to downconvert the entire band with a super-hetesrodyne RX [6]. In this case, the first mixer moves the entire channel to baseband, and the second downconversion extracts the few desired sub-carriers with . While this architecture avoids the power and area penalties associated with the use of multiple RXs, it lacks the capability to scale with features and technology due to its inherent complexity. To improve the scalability of previous designs, a digitally assisted RX is proposed in [4], where the image rejection (IR) calibration is implemented on a field programmable gate array (FPGA). Due to complexities of the system having been pushed into the digital domain, the RX frontend could be fairly simple and, hence, has the lowest power number among all existing LTE CA designs. However, the complexity of its digital backend poses a significant disadvantage. This architecture requires dual fast Fourier transform (FFT) blocks and multiple rounds of calculations with irrational numbers with high precision, thus incurring a penalty of large digital power. Moreover, the image rejection ratio (IRR) is tied to the filter's averaging time. This could result in high downlink latency and limits its application. Finally, a small in-phase/quadrature-phase (I/Q) signal may cause convergence difficulties for the image calibration because the I/Q signal power is the sole term in the denominators of the digital filter's coefficients [4].

This work proposes a highly linear mixer-first RX to support LTE intra-band CA. A mixer-first design [7] offers superb linearity without a large power penalty. However, it suffers from LO leakage re-radiation because it lacks the backward isolation provided by a low-noise amplifier (LNA). Also, an LTE RX needs to maintain a high IRR to reject the in-band inferences in the scenario of noncontiguous CA noted in [4], whereas mixer-first designs can only achieve limited IRR. In this work, a 5-bit mixer digital-to-analog converter (MxDAC) is integrated

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into every core mixer to provide calibration for LO leakage suppression. IRR is also improved by using a new mixed-signal calibration technique called I/Q correlated orthogonal calibration (I/Q-COC). The RX achieves a 2.6-dB noise figure (NF) and 15-dBm third-order input intercept point (IIP3) with 60 mW of power.

This paper is an expansion from [9] with a focus on decoupling the noise optimization from impedance match for a mixer-first RX. References [7] and [15] establish an impedance-frequency-translation theory for input match of a mixer-first RX, but their NF is closely tied to the input impedance, which results in a NF $\geq$ 3 dB. In Section II, we analyze three baseband designs from their impacts on the NF and input impedance and demonstrate that the baseband Op-Amp design is the key in decoupling its noise from its input impedance. Section III presents the detail of the proposed architecture in which the new IR calibration I/Q-COC is thoroughly discussed with its benefits and limitation. Moreover, an expansion about the flicker noise and a novel common-mode (CM) feedback scheme are included in Section III. The measurement results are presented in Section IV, in which we also take a closer look at the noise breakdown in the presence of a strong blocker.

## II. Impedance Match and NF Optimization

To match or not to match is more than just a rhetorical question since input matching has a profound impact on the overall NF. According to [8], the NF of a two-port network can be described by

$$F_{2\text{-port}} = F_M + \frac{R_n}{G_s}|Y_s - Y_{s,\text{opt}}|^2. \tag{1}$$

$F_M$ is the minimum achievable NF. $R_n$ and $G_s$ are the two-port model's input impedance and source conductance, respectively. The minimum NF can be achieved by designing the optimum source admittance $Y_{s,\text{opt}}$ equal to a given source admittance $Y_s$. For simplicity, assuming there is no correlation between different noise sources, then

$$Y_{s,\text{opt}} = \sqrt{\frac{G_s}{R_n}}. \tag{2}$$

$Y_{s,\text{opt}}$ has nothing to do with 50 Ω, but is instead related to the specific technology node and the architecture in use. This indicates that matching for noise instead of for power would yield a better NF. In [5], where the RF input is coming from a well-defined power splitter network, optimizing for noise match enables the low-band (LB) LNA to achieve an NF slightly above 1 dB, and the entire LB path has a total NF of 2.1 dB. However, an RX that requires the use of a specific external network is very inflexible and, hence, has very limited applications. Therefore, noise match will not be considered.

If maximal power transfer is preferred, the NF is restricted by the impedance match, and it makes the NF inherently difficult to be optimized. Most of the RXs published in the literature with $<$ 3-dB NF manage to decouple the NF from impedance match [2], [9]. The rest of this section discusses techniques for accomplishing this for a mixer-first RX shown in Fig. 1.

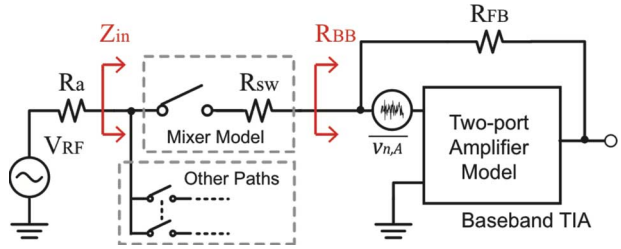



Fig. 1. General design model for a mixer-first RX architecture.

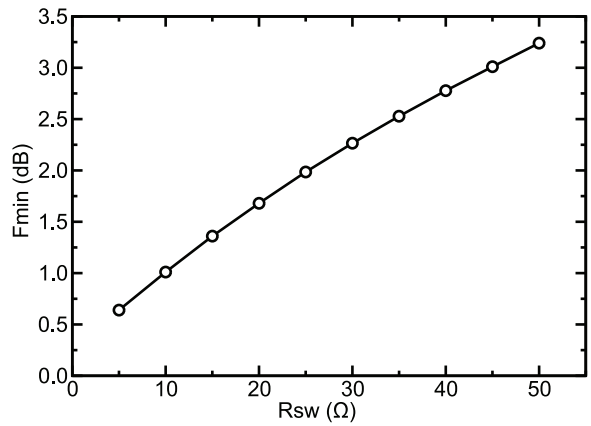



Fig. 2. Minimum achievable $F_{\min}$ due to $R$sw alone.

From [7], the NF of a mixer-first RX with eight paths is

$$F = 1 + \frac{R_{\text{sw}}}{R_a} + \left(\frac{1-8\gamma_8}{8\gamma_8}\right)\left(\frac{R_a + R_{\text{sw}}}{R_a}\right) + \gamma_8\frac{(R_a+R_{\text{sw}})^2}{R_a R_{\text{FB}}} + \frac{1}{8}\left(\frac{\overline{v_{n,A}^2}}{4kTR_a}\right)\left(\frac{(R_a+R_{\text{sw}})}{\gamma_8 R_{\text{FB}}} + 1\right) \tag{3}$$

where $\gamma_8 = 2/\pi^2(2-\sqrt{2})$ and $R_a$ is the antenna impedance. The NF is then set by the mixer switch on-impedance $R_{\text{sw}}$, the feedback resistor $R_{\text{FB}}$, and amplifier noise $\overline{v_{n,A}^2}$. The input impedance of such an RX can also be described as

$$Z_{\text{in}} = R_{\text{sw}} + \gamma_8 R_{\text{BB}} \tag{4}$$

where $R_{\text{BB}}$ is the input impedance of the baseband trans-impedance amplifier (TIA).

First of all, $R_{\text{sw}}$ in (4) sets the minimum achievable NF $F_{\min}$, which is set by the first three terms in (3),

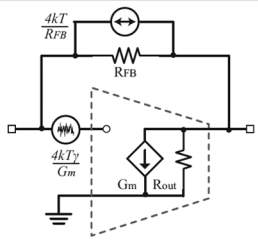
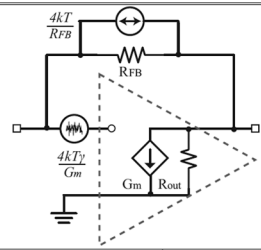
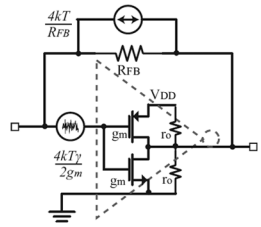
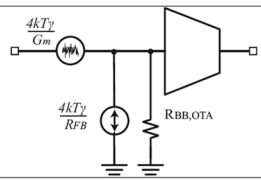
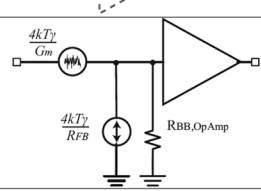
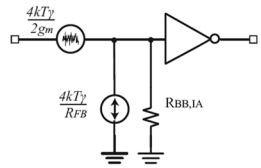
$$F_{\min} = 1 + \frac{R_{\text{sw}}}{R_a} + \left(\frac{1-8\gamma_8}{8\gamma_8}\right)\left(\frac{R_a+R_{\text{sw}}}{R_a}\right). \tag{5}$$

Fig. 2 shows the $F_{\min}$ for various sizes of $R_{\text{sw}}$. It is easy to see from (1) that the NF is at least 3 dB for a 50 Ω$R_{\text{sw}}$, with an actual $F_{\min}$ of 3.24 dB. The extra noise is because of noise folded down from high-order harmonics. Therefore, unless a noise cancellation technique like [2] is used, $R_{\text{sw}}$ should be chosen to be as small as the particular technology node allows.

For a shunt–shunt feedback system, $R_{\text{BB}}$ can be described as

$$R_{\text{BB}} = \frac{R_{\text{FB}}}{G_m(R_{\text{out}} \| R_{\text{FB}})} \tag{6}$$

TABLE I
COMPARISON TABLE FOR DIFFERENT AMPLIFIER ARCHITECTURES

| Baseband Amplifier Architecture | **OTA (One-Stage)** | **Op-Amp (One-Stage)** | **Inverter Amplifier (IA)** |
|---|---|---|---|
| A Simplified Baseband TIA Noise Model |  |  |  |
| A Simplified Baseband Input-referred Noise Model |  |  |  |
| Baseband Equivalent Noise Sources | $\overline{v_{BB}^2} = 4kT\gamma\frac{1}{G_m}$ ; $\overline{i_{BB}^2} = 4kT\frac{1}{R_{FB}}$ | $\overline{v_{BB}^2} = 4kT\gamma\frac{1}{G_m}$ ; $\overline{i_{BB}^2} = 4kT\frac{1}{R_{FB}}$ | $\overline{v_{BB}^2} = 4kT\gamma\frac{1}{2g_m}$ ; $\overline{i_{BB}^2} = 4kT\frac{1}{R_{FB}}$ |
| RF Input Impedance *Zin* | $R_{SW} + Y_8 R_{BB,OTA} \approx R_{SW} + \frac{Y_8}{G_m}$ | $R_{SW} + Y_8 R_{BB,OpAmp} \approx R_{SW} + \frac{Y_8 R_{FB}}{A_v}$ | $R_{SW} + Y_8 R_{BB,IA} = R_{SW} + Y_8(\frac{R_{FB}}{a_v} + \frac{1}{2g_m})$ |

where $G_m$ and $R_{\rm out}$ are the transconductance and the output impedance of the amplifier, respectively. For an one-stage operational transconductance amplifier (OTA), due to its high output impedance ($R_{\rm out} \gg R_{\rm FB}$), the amplifier is loaded by $R_{\rm FB}$and, hence, (6) is reduced to

$$R_{\rm BB,OTA} \approx \frac{1}{G_m}. \tag{7}$$

An Op-Amp, on the other hand, has a low output impedance ($R_{\rm out} \ll R_{\rm FB}$), therefore, for a one-stage Op-Amp with a voltage gain $A_v$,

$$R_{\rm BB,OpAmp} \approx \frac{R_{\rm FB}}{G_m R_{\rm out}} = \frac{R_{\rm FB}}{A_v}. \tag{8}$$

Finally, for an inverter amplifier (IA), $G_m$ and $R_{\rm out}$ are related to intrinsic small-signal device parameters as $2g_m$ and $r_o/2$. With $a_v = g_m r_o$, (6) can then be rewritten as

$$R_{\rm BB,IA} = \frac{R_{\rm FB}}{2g_m\left(\frac{r_o}{2} \parallel R_{\rm FB}\right)} = \frac{R_{\rm FB} + \frac{r_o}{2}}{g_m r_o} = \frac{R_{\rm FB}}{a_v} + \frac{1}{2g_m} \tag{9}$$

$a_v$ is the intrinsic small-signal gain. For CMOS devices with a certain channel length, $a_v$ is a technology constant. When $R_{\rm FB} \gg a_v/2g_m$, (9) reduces to $R_{\rm FB}/a_v$, which is similar to (8). However, when $R_{\rm FB} \ll a_v/2g_m$, (9) is similar to (7) as $1/2g_m$.

Table I compares the noise sources and input impedances of three types of amplifier structures. From [10], the noise due to the feedback resistors $R_{\rm FB}$ and the input-referred noise of the amplifiers $\overline{v_{n,A}^2}$ in the second row of Table I can be simplified to two noise sources at the input of the amplifiers, as shown in the third row of Table I. Their expressions are summarized in the fourth row of the table. Finally, the overall input impedances $Z_{\rm in}$ for RXs employing different amplifiers are derived by combining (4) and (7)–(9) and are listed in the last row of Table I.

The $\overline{v_{\rm BB}^2}$ and $Z_{\rm in}$ expressions of both the OTA and IA contain the inverses of their transconductances ($1/G_m$ and $1/2g_m$). This suggests that their baseband equivalent noise and input impedance are tied to each other. However, the Op-Amp's $Z_{\rm in}$ is independent from $G_m$. Furthermore, even though both the $\overline{i_{\rm BB}^2}$ and $Z_{\rm in}$ of an Op-Amp include $R_{\rm FB}$, the input impedance is primarily determined by $A_v$. Therefore, an Op-Amp-based TIA succeeds in decoupling the noise optimization from input matching.

From (4) and Table I, for an RX with single-stage OTA, (3) can be revised to

$$F_{\rm OTA,1stg} = F_{\rm min} + \gamma_8\frac{(R_a + R_{\rm sw})^2}{R_a R_{\rm FB}} + \frac{1}{8}\left(\frac{1}{R_a}\right)\left(\frac{\gamma}{\gamma_8}\right) \cdot \left(\frac{1}{R_a - R_{\rm sw}}\right)\left(\frac{R_a + R_{\rm sw}}{\gamma_8 R_{\rm FB}} + 1\right). \tag{10}$$

Similarly, for an RX with one-stage Op-Amps,

$$F_{\rm OpAmp,1stg} = F_{\rm min} + \gamma_8\frac{(R_a + R_{\rm sw})^2}{R_a R_{\rm FB}} + \frac{1}{8}\left(\frac{1}{R_a}\right)\left(\frac{\gamma}{\gamma_8}\right) \cdot \left(\frac{R_{\rm out}}{R_a - R_{\rm SW}}\right)\left(\frac{R_a + R_{\rm sw}}{\gamma_8 R_{\rm FB}} + 1\right). \tag{11}$$

Moreover, when $R_{\rm FB} < a_v(R_a - R_{\rm SW})$, the NF for an RX with IAs can be derived from (3), (4), and Table I,

$$F_{\rm IA} = F_{\rm min} + \gamma_8\frac{(R_a + R_{\rm sw})^2}{R_a R_{\rm FB}} + \frac{1}{8}\left(\frac{1}{R_a}\right)\left(\frac{\gamma}{\gamma_8}\right) \cdot \left(\frac{1}{R_a - R_{\rm SW} - \frac{R_{\rm FB}}{a_v}}\right)\left(\frac{R_a + R_{\rm SW}}{\gamma_8 R_{FB}} + 1\right). \tag{12}$$

Fig. 3 shows the simulated NF for a range of $R_{\rm FB}$ values when different types of baseband amplifiers are adpoted.

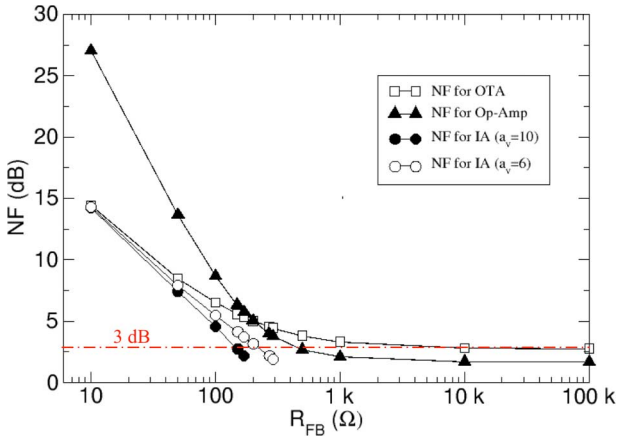



Fig. 3. NF for OTA, Op-Amp, and IA with $a_v = 6$ and $a_v = 10$ with a different size of $R_{\rm FB}$.

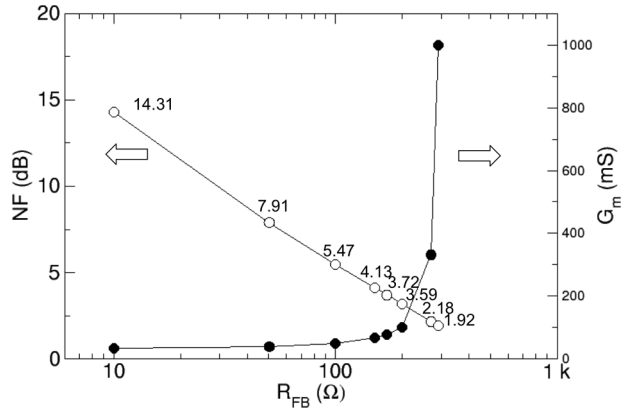



Fig. 4. Simulated NF and $G_m$ required for different value of $R_{\rm FB}$ for an IA with $a_v = 10$.

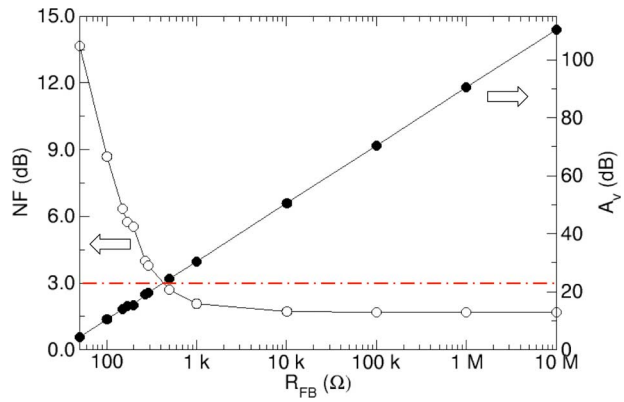



Fig. 5. Simulated NF and $A_v$ required for different value of $R_{\rm FB}$ for a one-stage Op-Amp.

Without losing generality, $R_{\rm sw}$, $\gamma$, and $R_{\rm out}$ (for Op-Amp only) are set to 20 Ω, 2/3, and 200 Ω, respectively.

From (7) and Table I, the OTA relies on $1/G_m$ for input matching when $R_{\rm FB}$ is reasonably large. The OTA's equivalent noise resistor $R_{\rm eq}$ also contains $1/G_m$, resulting in an NF that saturates $\sim$ 3 dB beyond a certain value of $R_{\rm FB}$ in Fig. 3. The NF asymptotically approaches 2.77 dB to be precise. It is $<$ 3 dB in this case because $\gamma < 1$ is assumed in this analysis.

On the other hand, with a small $R_{\rm FB}$, the IA behaves like the OTA in Fig. 3. However, since $a_v$ is a constant related to technology and the devices' channel length, the IA cannot provide input matching for arbitrarily large $R_{\rm FB}$. For instance, from Table I, for $a_v = 10$, and $R_{\rm FB} = 10$ kΩ, $Z_{\rm in} > 1$ kΩ. This can also been seen from (12), where the last term would be negative if $R_{\rm FB} > a_v(R_a - R_{Sw})$. Hence, (12) will no longer be valid when $R_{\rm FB}$ is too large.

When $R_{\rm FB}$ is relatively small, the Op-Amp requires a small $G_m$ to match to the 50 Ω$Z_{\rm in}$; therefore its NF suffers. On the other hand, as $R_{\rm FB}$ increases, $G_m$ has to be scaled up in proportion to maintain the same $Z_{\rm in}$. As a result, as shown in Fig. 3, the input-referred noise of the TIA is improved, and the NF approaches the value of $F_{\rm min}$ as predicted by (5).

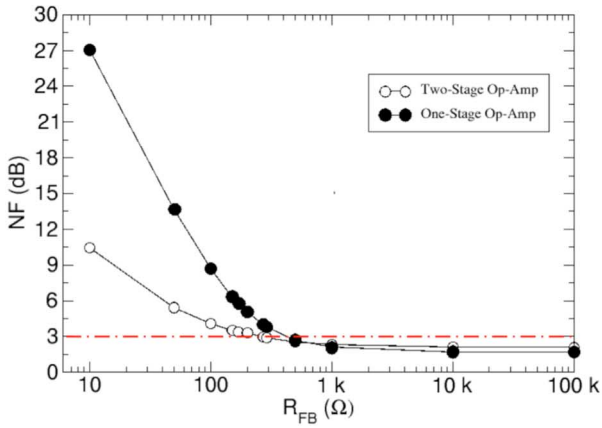
Interestingly, Fig. 3 shows that in theory both the IA and Op-Amp are able to achieve an NF less than 3 dB. However, in reality the IA requires a daunting $G_m$ value ($G_m = 2g_m$) to push the NF below 3 dB, as demonstrated in Fig. 4. To reduce the NF of an IA with $a_v = 10$ from 3.59 to 2.18 dB, the required $G_m$ increases from 81 to 333 mS. Furthermore, to achieve a 1.92-dB NF, the $G_m$ needs to exceed 1000 mS, which requires prohibitively large devices. It is clearly a rapidly diminishing return. Moreover, the RX system linearity would be severely degraded with such a large transconductance.

On the other hand, an Op-Amp design does not rely on $G_m$ for the impedance match, therefore with a large $R_{\rm FB}$, NF can penetrate 3 dB and asymptotically approach $F_{\rm min}$. However, to achieve a sub-3-dB NF, a large $A_V$ is required. Fig. 5 shows the NF and $A_V$ required for different values of $R_{\rm FB}$ for a one-stage Op-Amp. From Table I, both the $\overline{i_{\rm BB}^2}$ and $Z_{\rm in}$ of an Op-Amp include $R_{\rm FB}$. To achieve a better NF, it is preferable to have a large $R_{\rm FB}$. However, as shown in Table I, a large $R_{\rm FB}$ needs to be compensated with a large $A_V$ to maintain input matching. This is why $A_V$ scales linearly with $R_{\rm FB}$ in Fig. 5. For $R_{\rm FB} =$ 10 kΩ, $A_V$ needs to be as large as $\sim$ 50 dB, which is impractical for a one-stage design on a state-of-art CMOS technology with a limited 1-V supply.

Fortunately, the above issue can be easily resolved with a two-stage (or multi-stage) Op-Amp design, where the small-signal gain $A_v$ no longer sets a practical limit. As far as loop stability and system linearity are concerned, the baseband structure should remain as few stages as possible. One subtlety of a multi-stage design is that its $\overline{v_{n,A}^2}$ is dominated by the noise associated with the first stage $G_{m\_1{\rm stAmp}}$. The $G_{m\_1{\rm stAmp}}$ in a multi-stage design is always smaller than $G_{m\_1{\rm stAmp}}$ in a single-stage Op-Amp, but it can now be optimized independently of the required $A_v$. Untangling $G_{m\_1{\rm stAmp}}$ from the required $A_v$ is crucial because it does not require an excessively large $G_m$, as in the case of an IA, to achieve a good NF. From (3), (5), (8), and the analysis above, the expressions for the NF and gain of a multi-stage Op-Amp can be shown as

$$F_{{\rm OpAmp},M-{\rm stg}} = F_{\rm min} + \gamma_8 \frac{(R_a + R_{\rm SW})^2}{R_a R_{\rm FB}} + \frac{1}{8}\left(\frac{\gamma}{\gamma_8}\right) \cdot \left(\frac{1}{G_{m\_1{\rm stAmp}} R_a}\right)\left(\frac{R_a + R_{\rm sw}}{\gamma_8 R_{\rm FB}} + 1\right) \quad (13)$$

$$A_v = \frac{\gamma_8 R_{\rm FB}}{R_a - R_{\rm sw}}. \quad (14)$$




(a)

| Design Parameter | Design Value | Parameter Definition |
|---|---|---|
| $R_a$ | 50 Ω | Impedance of the Input Port |
| $R_{SW}$ | 20 Ω | On-Impedance of the Mixer Switch |
| $R_{FB}$ | 10 Ω - 10 MΩ | Baseband Feedback Resistor |
| $\gamma_8$ | $2/\pi^2\,(2-\sqrt{2})$ | Scaling factor for noise folding [7] |
| $\gamma$ | 2/3 | Noise coefficient for MOSFET |
| $G_{m\_1stamp}$ | 100 mS | Transconductance of the first stage of a two-stage Op-Amp |
| $A_v$ | $\frac{\gamma_8 R_{FB}}{50 - R_{SW}}$ | Small signal Gain (Same for one-stage and two stage design) |

(b)

Fig. 6. Simulation results for NF of one- and two-stage amplifiers. (a) Simulated NF for one- and two-stage Op-Amps with different value $R_{\rm FB}$. (b) Design values used in plotting (a).

TABLE II
SAMPLE SET OF DESIGN VALUES FOR A MIXER-FIRST RX WITH A TWO-STAGE OP-AMP TO BREAK THE 3-dB NF BARRIER

| Design Parameter | Design Value | Parameter Definition |
|---|---|---|
| $R_a$ | 50 Ω | Impedance of the Input Port |
| $R_{SW}$ | 20 Ω | On-Impedance of the Mixer Switch |
| $R_{FB}$ | 10 kΩ | Baseband Feedback Resistor |
| $\gamma_8$ | $2/\pi^2\,(2-\sqrt{2})$ | Scaling factor for noise folding [7] |
| $\gamma$ | 2/3 | Noise coefficient for MOSFET |
| $G_{m\_1stamp}$ | 100 mS | Transconductance of the first stage |
| $A_v$ | 50 dB | Small signal Gain |
| **NF** | **2.105 dB** | **Noise figure of the RX** |

Fig. 6(a) compares the simulated NF between a one-stage Op-Amp with that of a two-stage design for various $R_{\rm FB}$ based on (5), (11), and (13). For the two-stage design, $G_{m\_1{\rm stAmp}}$ is set to 100 mS regardless of the value of $R_{\rm FB}$. Even though the two-stage Op-Amp saturates to a slightly higher NF with a large $R_{\rm FB}$, the degradation is quite acceptable: for instance, for $R_{\rm FB} = 10$ MΩ the NF increases from 1.685 dB for a one-stage design to 2.08 dB for a two-stage amplifier. Most importantly, a mixer-first design can now finally break the 3-dB NF bottleneck with a set of practical design values of $R_{\rm SW}R_{\rm FB}A_v$ and $G_{m\_1{\rm stAmp}}$. A sample set of such values and the estimated NF have been listed in Table II.

For the sake of completeness, it is also important to address the limitations of the above analysis. Equation (10)–(13) do not cover the thermal and flicker noise from the clock generation and distribution circuit, nor do they include the flicker-noise component from the baseband amplifiers. The flicker-noise upconversion in the clock generation has been discussed in [11], and it will not be repeated here. As shall be further covered in Sections III and IV, at low frequency, the NF is dominated by flicker noise from the amplifier and the clock circuit, so it deviates from the value predicted by (13). Therefore, extensive simulations are always recommended and necessary to accurately model the NF of the RX. Lastly, $\gamma$ used throughout the above analysis is 2/3, which is only true for long-channel devices in strong inversion. Hence, the results for short-channel transistors in the sub-threshold region could be worse. Nevertheless, the analysis above still serves as a good starting point for optimizing the NF of a mixer-first RX.

## III. CIRCUIT IMPLEMENTATION

### A. System Overview

Fig. 7 shows an overview of the proposed RX system. A single-ended RF input signal is down-converted through eight different paths, each of which is controlled by a non-overlapping 12.5% duty-cycle clock. When the path outputs are combined with appropriate weights, the eight-phase down-conversion rejects the third and fifth harmonics. It also reduces the amount of noise folded down from higher order harmonics [7], [8]. Each of the mixer units consists of two parts: a core mixer and an additional 5-bit MxDAC to provide fine-tuning capability. Moreover, the baseband circuit is implemented with two stages of amplification of $A_1$ and $A_2$ to provide the desired large $A_v$, as discussed in Section II. This allows the use of a large feedback resistor $R_{\rm FB}(\sim 8\ {\rm k}\Omega)$ that contributes very little noise. As shown in Fig. 7, $A_1$ serves as a transconductor, whereas $A_2$ is configured as a TIA. To provide a wide baseband bandwidth (50 MHz) and high slew rate while simultaneously maintaining low power consumption, the baseband low-noise amplifier (BLNA) $A_1$ is designed as an IA. Five low dropout regulators (LDOs) are implemented on chip for better isolation between different supplies. An on-chip clock divider generates all of the required clock phases from an external $4\times$ LO. The digital core of I/Q-COC monitors the digital outputs and fine tunes the code words of MxDACs at start up. Finally, a digital least mean square (LMS) IR filter similar to the one reported in [12] further enhances the IRR during runtime prior to the digital downconversion.

Two major issues with a mixer-first RX are LO leakage and limited IRR. LO leakage is a direct result of mismatches among the mixers and LO buffers. In this design, the embedded MxDAC can fine tune the mixer devices to alleviate this issue. Moreover, since the MxDAC improves the matching of the mixers, it improves the second-order input intercept point (IIP2) performance. High IRR, on the other hand, is desirable for an LTE RX since it can reduce image folding from other in-band subcarriers to the desired band. IRR is limited by the phase and the gain mismatches of different paths [12]. The gain mismatch can be calibrated by adjusting the baseband feedback resistor $R_{\rm FB}$, but the phase mismatch is more difficult to be corrected.

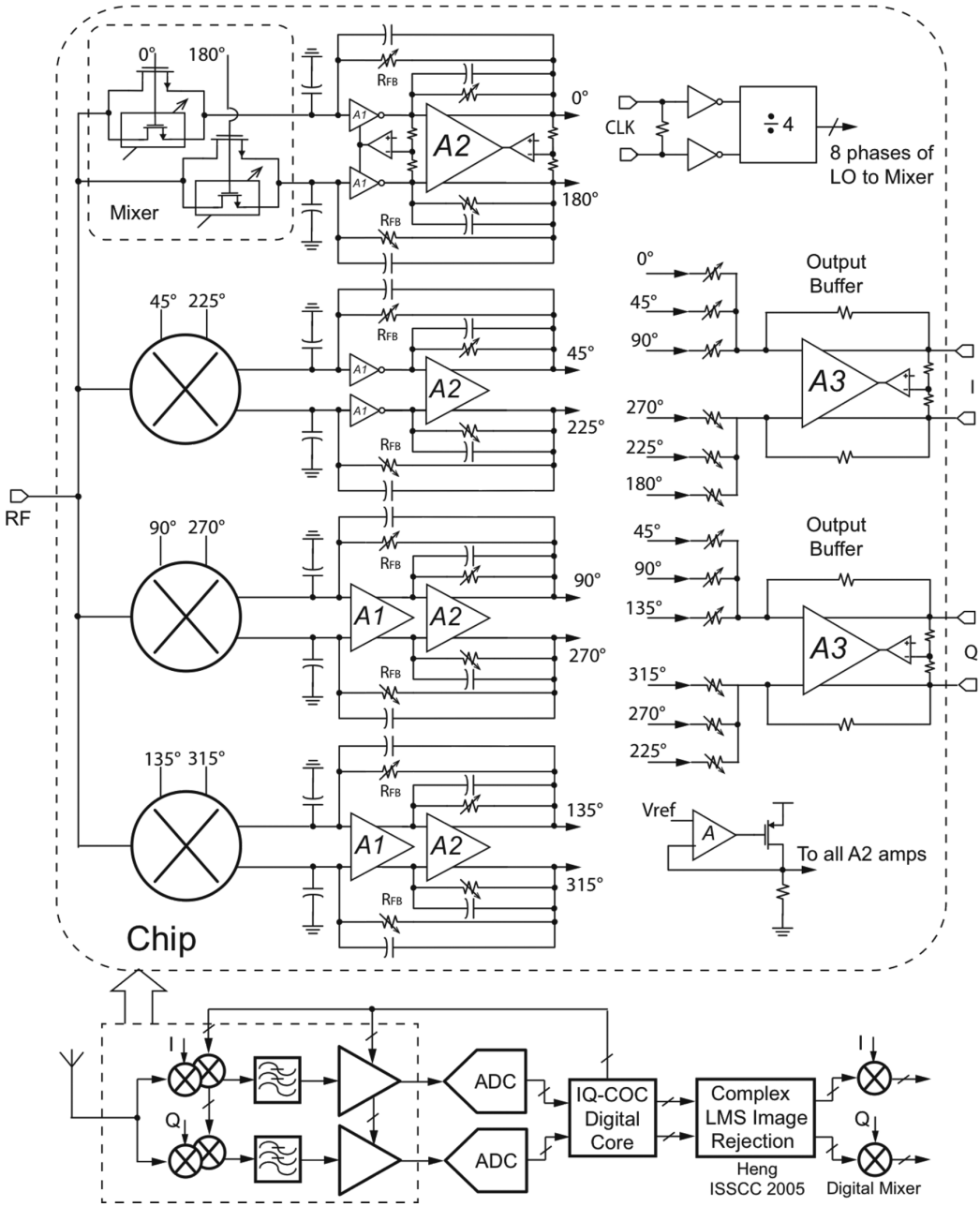



Fig. 7. Architectural design and system overview of the proposed passive mixer-first LTE RX system.

### *B. I/Q-COC*

An in-depth discussion of IRR for a typical RX is included in [12], where $I + jQ$ is described as

$$I + jQ = e^{j\omega t} + \left(\frac{\alpha - j\theta}{2}\right) e^{-j\omega t}. \tag{15}$$

The IRR sensitivity for a typical RX is thus shown to be

$$\left|\frac{\partial \mathrm{IRR}_{\mathrm{typ}}}{\partial \sigma_{A\_\mathrm{typ}}}\right|^2 = \frac{1}{4}\sigma^2_{A\_\mathrm{typ}} \tag{16}$$

$$\left|\frac{\partial \mathrm{IRR}_{\mathrm{typ}}}{\partial \sigma_{\varphi\_\mathrm{typ}}}\right|^2 = \frac{1}{4}\sigma^2_{\varphi\_\mathrm{typ}} \tag{17}$$

where $\sigma^2_{A\_\mathrm{typ}}$ and $\sigma^2_{\varphi\_\mathrm{typ}}$ are the variances of the gain and phase mismatches respectively. Appendix A shows the derivation of a harmonic rejection (HR) RX's IRR sensitivity. The results of (A14) and (A15) are repeated here for the readers' convenience,

$$\left|\frac{\partial \mathrm{IRR}}{\partial \sigma_A}\right|^2 = \frac{1}{8}\sigma^2_A$$

$$\left|\frac{\partial \mathrm{IRR}}{\partial \sigma_\varphi}\right|^2 = \frac{1}{16}\sigma^2_\varphi.$$

$\sigma^2_A$ and $\sigma^2_\varphi$ are the variances of the gain and phase mismatches for an HR RX. Comparing (A14) and (A15) to (16) and (17), one can see that an HR RX has a slightly better IRR than a typical RX. For example, with 1% gain mismatch, (16) predicts that a typical RX will have an IRR of 46 dB, whereas (A14) suggests that an HR RX can be 3 dB better. On the other hand, with 1% phase mismatch, (17) predicts a 46-dB IRR for a typical RX, while (A15) predicts a 52-dB IRR for an HR RX. Still, the

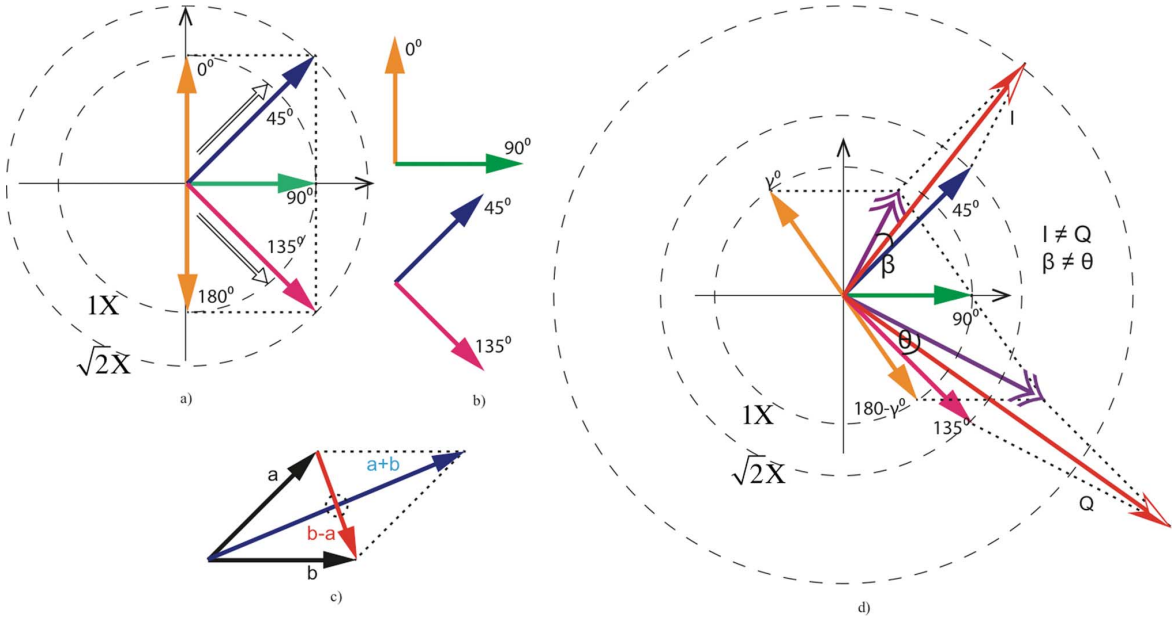



Fig. 8. Basic principles of I/Q vector formation and uncalibrated I/Q vector generation. (a) HR vector summation. (b) 2 Pairs of vectors of HR. (c) Orthogonal vector reference generation. (d) Uncalibrated I\Q generation.

marginal improvements from (A14) and (A15) are not enough to satisfy the stringent IRR required by LTE-A [4].

Fig. 8 demonstrates the principles of the I/Q vector formation. In an HR RX, as demonstrated in Fig. 8(a) and (b) , there are two pairs of orthogonal vectors (0° and 90°, 45° and 135°). Also, as shown in Fig. 8(c), a pair of perfectly orthogonal references can be generated by the vector summation and subtraction of a pair of vectors. Reference [12] shows that phase mismatch alone can result in both phase and gain mismatches in the final I/Q products, and a graphical illustration of such a process for an HR RX is demonstrated in Fig. 8(d).

To alleviate this issue, the concept of I/Q-COC is proposed by taking advantage of the eight downconverted paths in an HR system. As shown in Fig. 9(a), the pair of 0° and 90° signals can be first used to create the orthogonal references to calibrate the 45° and 135° pair. Afterwards, the calibrated 45° and 135° pair can, in turn, be used to correct the phase mismatch in the 0° and 90° pair. We are not trying to remove the phase mismatches to retain each vector's absolute phase value, rather we only aim at preserving the 90° phase difference between each orthogonal pair. A complete vector formation after I/Q calibration is demonstrated in Fig. 9(b). The computations of vector summation and subtraction are implemented in the digital domain to avoid introducing additional errors (such as noise or nonlinearity) from an analog adder or subtractor. Finally although the phase values of different paths would change after I/Q-COC, as in Fig. 9(b), the IRR or error vector magnitude (EVM) performance would not be degraded because I/Q-COC only causes the final resulting signal constellation to rotate. This can easily to be re-adjusted in the digital domain.

In theory, I/Q-COC reduces the phase mismatches of an HR RX and, hence, can improve both the IRR and harmonic rejection ratio (HRR) with additional calibration iterations on the I/Q channels. In practice, however, this is not feasible, due to limitation in device matching of a modern CMOS technology. As shown in Fig. 10, for third-order harmonics, the resultant vectors of different downconversion paths rotate by 3×, resulting a 3× phase mismatch amplification. Similarly, to reject the fifth-order harmonic, the phase mismatch requirement would be 5× more stringent. Therefore, to achieve a 60-dB third- or fifth-order HR, the MxDAC has to be excessively large, which would limit the RX's functional RF frequency range.

### C. Mixer and MxDAC

Fig. 11 details the mixer design. The mixers are biased at 0.65 V. In this work, the mixer switch resistance $R_{\rm sw}$ is substantially reduced to $<$ 15 Ω by utilizing 28-nm technology. 28-nm technology provides superior switches with significantly lower on-impedance, as well as reduced switching power. The MxDAC is unit weighted, with each unit cell sized approximately 1% the size of the mixer core, to ensure monotonicity across all DAC codes.

### D. BLNA $A_1$

The BLNA $A_1$ in Fig. 7 has an inverter-based thick oxide design to supply the $G_m$ required in (13) to achieve a good NF while maintaining high power efficiency. The details of the design are shown in Fig. 12. Table III compares simulated noise contributions from the mixer's thermal noise and flicker noise from the BLNA and clock generation for different noise bandwidths. As discussed towards the end of Section II and supported by the data in Table III, flicker noise can have a major impact on the overall NF. At low frequencies, in addition to the mixer's thermal noise, the flicker noises from the BLNA and the clock generation circuit are also significant. Therefore, a large amount of design effort has been invested towards balancing the BLNA's dimensions and its biasing conditions to achieve the optimum tradeoff between its $G_m$, system linearity, and its flicker noise performance.

Furthermore, to improve power supply rejection ratio (PSRR), the CM amplifier is designed as a low-dropout (LDO)

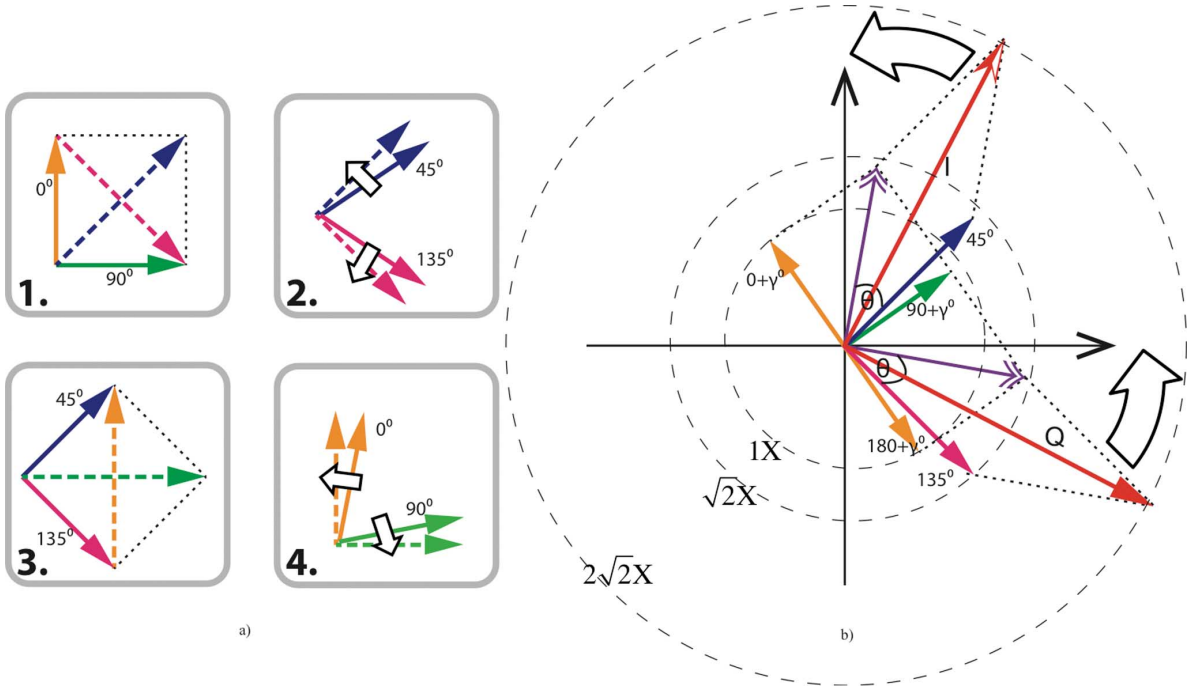



Fig. 9. I/Q calibration procedure and a graphical representation of the vector formation process of I/Q-COC. (a) I\Q-COC calibration procedures. (b) Calibrated I\Q generation.

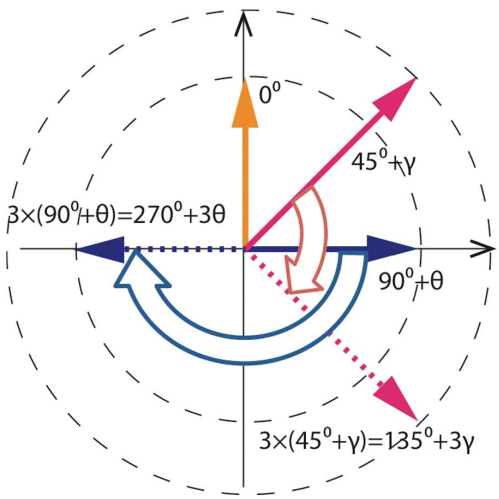



Fig. 10. Illustration showing why HR is more sensitive to mismatches.

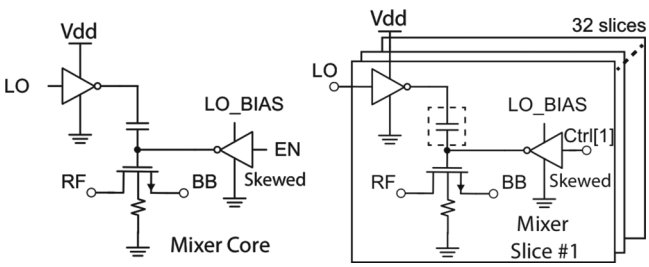



Fig. 11. Mixer core and the 32 slices of the MxDAC.

amplifier. The LDO reference comes from a local replica bias. All LDOs operate at 1.5 V.

### *E. Second-Stage Op-Amp $A_2$*

The second amplifier $A_2$ in Fig. 7 must be able to maintain a high gain and wide bandwidth, which is quite challenging with a

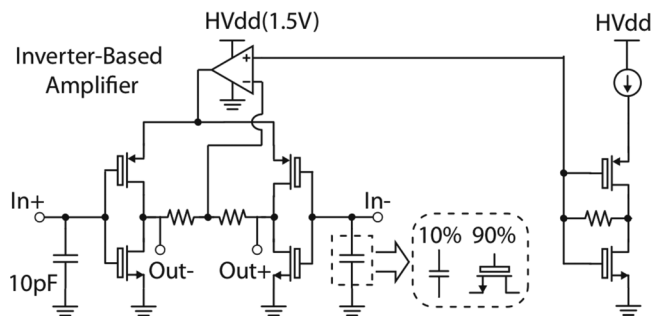



Fig. 12. Inverter-based baseband LNA $A_1$.

TABLE III
NOISE CONTRIBUTION OF THE MIXER' S THERMAL NOISE, FLICKER NOISE FROM THE BLNA, AND CLOCK GENERATION AT DIFFERENT NOISE BANDWIDTHS

| Noise Bandwidth | **Up to 100 kHz** | **Up to 170 kHz** | **Up to 10 MHz** |
|---|---|---|---|
| No.1 Noise Source | Flicker – BLNA (29.07%) | Thermal – Mixer (34.49%) | Thermal – Mixer (68.84%) |
| No. 2 Noise Source | Flicker – Clk Gen (20.11%) | Flicker – BLNA (21.47%) | Flicker – BLNA (6.72%) |
| No. 3 Noise Source | Thermal – Mixer (17.63%) | Flicker – Clk Gen (14.57%) | Flicker – Clk Gen (1.19%) |

1-V supply. A two-stage design can meet the gain requirement with ease, but it has a limited bandwidth and slew rate due to the *Cc*'s large size. Moreover, a two-stage amplifier suffers from CM instability with a low supply. Figs. 13 and 14 demonstrate this issue. Fig. 13(a) shows a two-stage amplifier in shunt–shunt feedback used as a TIA. A CM amplifier senses the output CM voltage and adjusts the bias of the NMOS loads accordingly. With a 1-V supply, only limited headroom can be allocated for the tail current source, which leads to a poor $r_{ds}$. Also, due to limited headroom, the input pair and the tail current source are

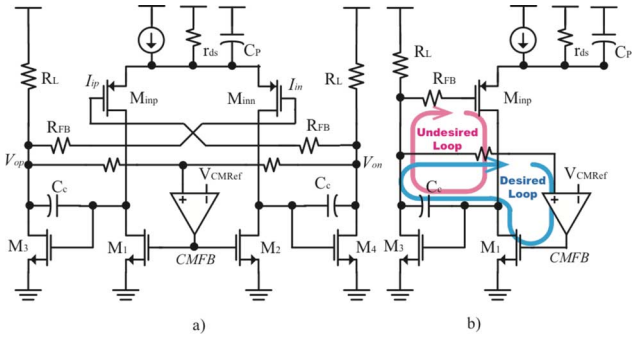



Fig. 13. Illustration of the CM instability issue for a two- stage amplifier with a low supply. (a) Differential two-stage TIA with CMFB. (b) CM half circuit of the two-stage TIA.

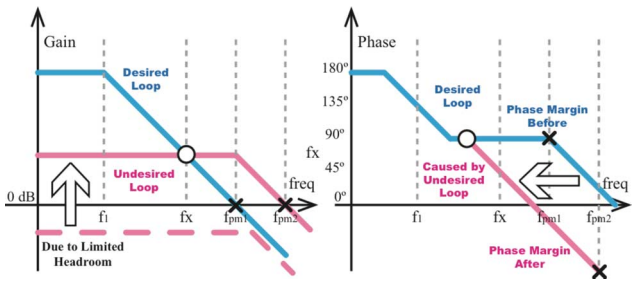



Fig. 14. Simplified frequency responses (gain and phase) explaining how the undesired positive feedback is competing with the desired CM loop.

forced to operate with small overdrive voltages, which results in the need for large transistors and, hence, a large parasitic $C_p$ at the virtual ground. For the TIA in Fig. 13(a), the two inverting stages form an undesired wideband CM positive feedback loop, as highlighted in Fig. 13(b). Usually this undesired loop has a loop gain $< 1$ because the input pair's CM gain is heavily degenerated by the tail current source's high output impedance [10]. However, in this case, the large $C_p$ together with small $r_{ds}$ lower the output impedance of the current source so that the CM gain of the first stage is still high. This strong positive loop has a negative effect on the overall CM stability.

In general, the desired negative CM loop is strong, but narrowband [10]. As shown in Fig. 14, the undesired positive loop will take over when the gain of the desired negative CM loop diminishes. As a result, the phase margin of the CM loop suffers, and the overall CM stability is degraded.

An ac-boosting compensation (ACBC) scheme [13] provides a better alternative to the two-stage design in addressing CM stability. A major benefit of the ACBC design is its use of three inverting stages, guaranteeing that global CM feedback is always negative. As shown in Fig. 15, a PMOS input pair is adopted for better flicker noise performance. The input signal is also fed forward to the output stage to create a feed-forward zero, which allows for the use of smaller compensation capacitors and, hence, higher slew rate. The simulated unity-gain frequency of this design is beyond 1.2 GHz based on simulation. Finally, the output stage has a class-AB structure to enable further slew rate and linearity improvements.

### F. Calibration Procedure

The calibration procedure begins with an iterative sweep through all codes of each MxDAC to achieve a balanced suppression of leakages from multiple LO harmonics. The gains

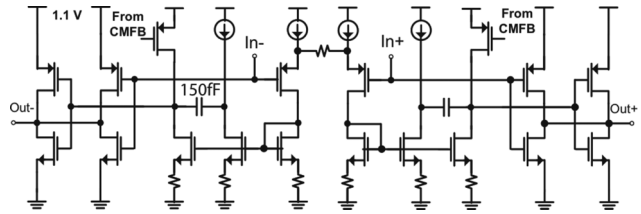



Fig. 15. Second-stage amplifier based on ACBC architecture.

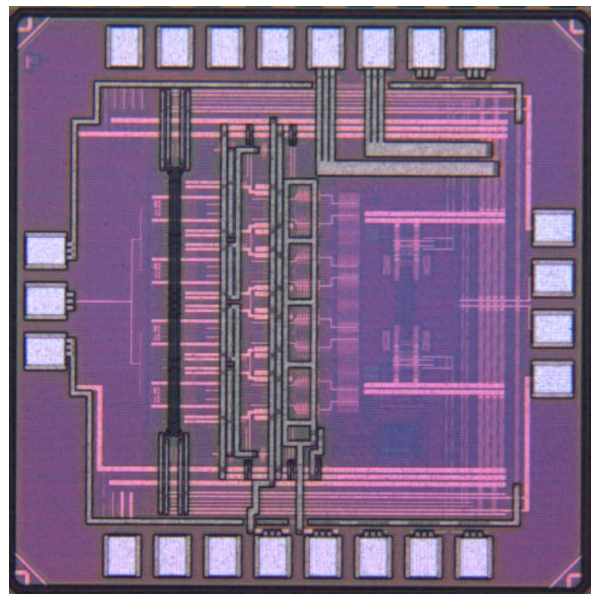


Fig. 16. Chip microphotograph.

of the baseband amplifiers are then fine tuned through $R_{\mathrm{FB}}$ to reduce the gain mismatches among different paths. Afterwards, I/Q-COC is applied to the system one orthogonal pair of channels at a time to fine tune the code word to each MxDAC. Finally, the digital LMS filter in the backend is enabled to further enhance the overall IRR in the background.

## IV. Measurement Results

The design is implemented in a general-purpose 28-nm technology with a 1-V supply and an active area of 460 $\mu$m by 500 $\mu$m, as shown in Fig. 16.

Fig. 17 shows measured $S_{11}$ from 250 MHz to 3.5 GHz. This work maintains a good input matching over a wide frequency range, as compared to a noise cancelation RX [2] whose input matching is degraded due to additional loading at the RF terminal from the auxiliary path,

To quantify the NF, the conversion gain is first measured at $\sim$ 35 dB. The output noise is then integrated with the off-chip losses are accurately de-embedded. Finally, the NF is extracted by dividing the output noise by the conversion gain. As shown in Fig. 18, the measured double-sideband NF integrated up to 10 MHz varies from 2.4 to 2.6 dB. The spot NF for this work at 20-kHz offset is 7.5 dB. From Table III, we believe it is limited by the flicker noise from the BLNA and the clock generation. In comparison, the noise cancelation RX reported in [2] not only is able to achieve a 1.9-dB NF at 1-MHz offset, but also effectively suppresses the flicker noise to achieve a 3.5-dB NF at 20-kHz offset.

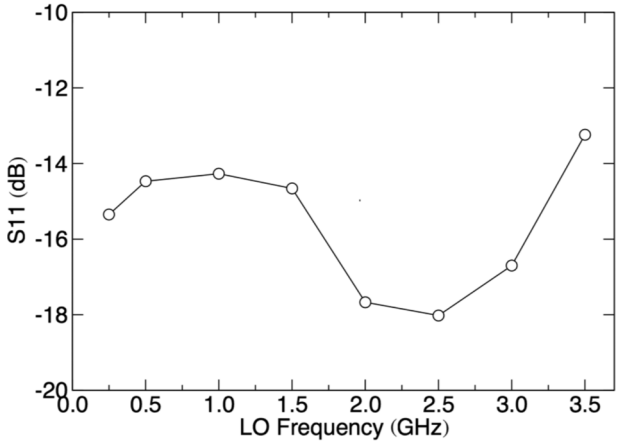



Fig. 17. Measured $S_{11}$ over wide frequency of operation.

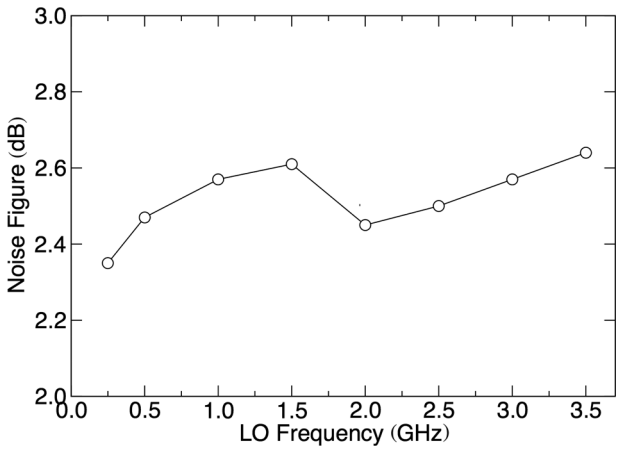



Fig. 18. Measured NF from 250 MHz to 3.5 GHz.

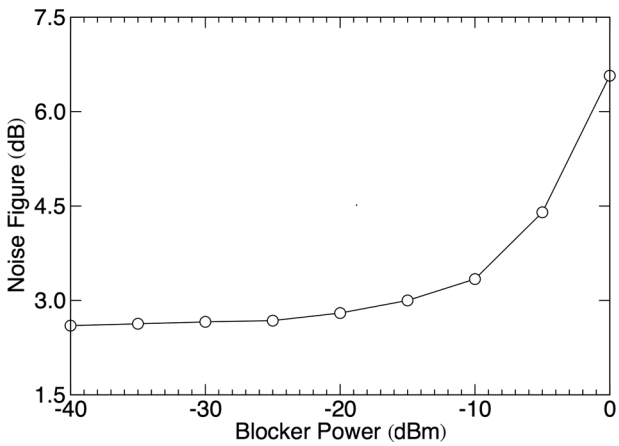



Fig. 19. Measured NF with different blocker power level.

Fig. 19 shows the measured NF in the presence of a single-tone interferer injected 50 MHz from the band edge. The NF is 3.2 dB for a −10-dBm blocker and 6.5 dB for a 0-dBm blocker. Fig. 20 breaks down simulated noise contribution for the RX in the presence of strong interference. Aside from reciprocal mixing, there are two causes for NF degradation. First, the RX fails to maintain its differentiality. Therefore, it is sensitive to the LDOs' bias and CM noise. Second, the blocker disrupts mixers' bias condition, which causes them to generate flicker noise during the large signal transient. In summary, to minimize the NF when strong interferers are present, noise contribution

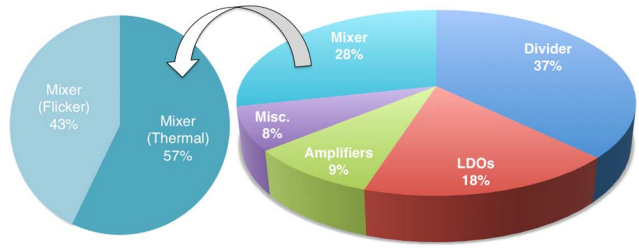



Fig. 20. Noise breakdown based on noise simulation with a strong blocker.

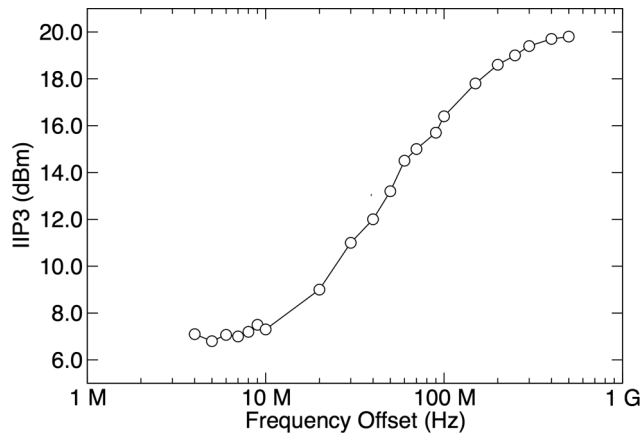



Fig. 21. Measured IIP3 for various two-tone spacings.

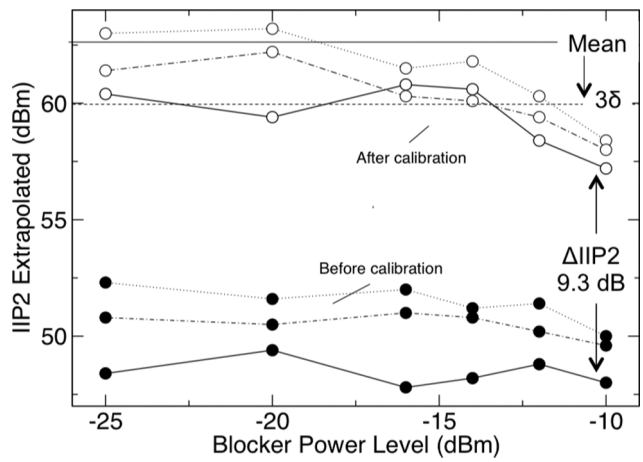



Fig. 22. Measured IIP2 before and after calibration.

from all components must be considered. Hence we carefully modeled and optimized the noise performances of all LDOs, the bias network, and the CM circuit. NF under a strong blocker can be further enhanced by the noise cancellation technique, as [2] reports a 4.1-dB NF for a 0-dBm blocker.

Fig. 21 shows the measured IIP3. The RX achieves an IIP3 $>$ 15 dBm IIP3 for a tone spacing larger than 50 MHz. The LO leakage calibration also improves the IIP2 performance. As shown in Fig. 22, the improvement in IIP2 from the three silicon samples is at least 9.3 dB. The IIP2 observed after calibration is in good agreement with the simulation results (mean value and its distribution), which are overlaid on top of the measurement results in Fig. 22.

LO leakage measurements at 1.5-GHz operating frequency are detailed in Fig. 23. The calibration suppresses leakage at multiple LO harmonics from −48 dBm (fourth harmonic—worst case spur without calibration) down to −62 dBm

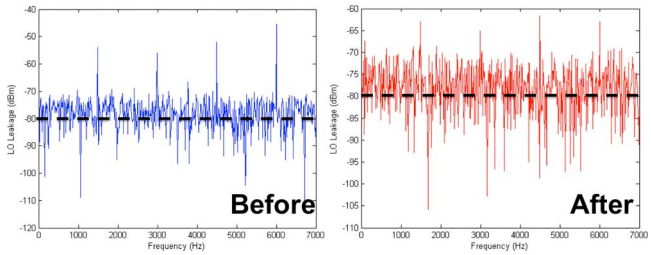



Fig. 23. Measured LO leakage at 1.5 GHz for before and after calibration.

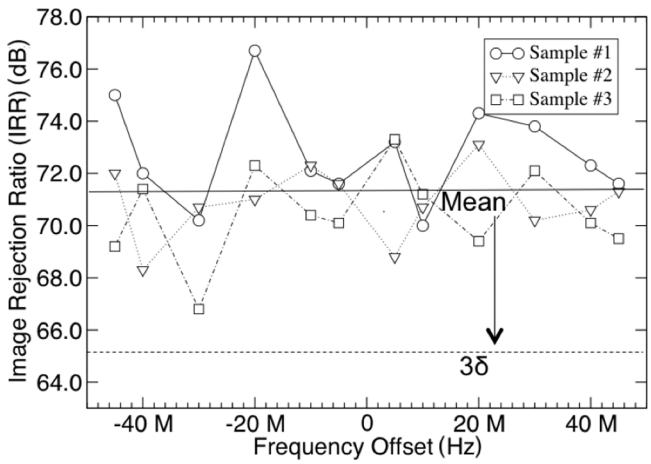



Fig. 24. Measured data for IRR at 2 GHz across three silicon samples.

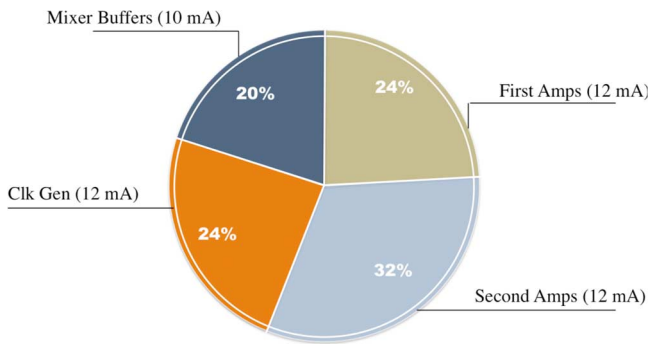



Fig. 25. Power breakdown for the major circuit components at 2 GHz.

(third harmonic—worst case spur after calibration). While the 10-bit dc tuning DACs in [14] reduce only the fundamental LO tone to $\sim -80$ dBm, this work manages to suppress multiple LO harmonics all together. Additionally, Fig. 24 shows the IRR at an operating frequency of 2 GHz. The measured IRRs of three chip samples exceed 66 dB across the 100-MHz complex baseband bandwidth, which agrees with the simulation data (included on top of the IRR measurement results).

Fig. 25 shows a power breakdown of the RX. Up-sizing the clock generation circuitry and the mixer buffers in order to reduce their flicker noise contribution (listed in Table III) results in non-negligible dynamic power dissipation. Also, most of the amplifier power is due to the requirement to achieve a wide baseband bandwidth (50 MHz) for LTE-A and to maintain system linearity. Overall, at 2 GHz of operation, the RX consumes 50 mW from the local 1-V supplies, or 60 mW from the global 1 and 1.5 V including all the LDOs.

Finally, Table IV summarizes the RX performance and compares it with the other state-of-the-art designs.

## V. Conclusion

This work has demonstrated a mixer-first RX designed in 28-nm CMOS. Its 5-bit MxDAC provides a wideband tunable match to suppress leakage from multiple LO harmonics. The baseband BLNA together with the ACBC amplifier provides a 50-MHz baseband bandwidth. It supports intra-band CA for LTE-A in a power-efficient manner. The circuit achieves 2.6-dB NF, $>$ 15-dBm IIP3, and 35-dB gain with 60-mW power accounting for five separate on-chip LDOs from the 1- and 1.5-V supplies.

## Appendix

Firstly, analysis on the impact of the gain and phase mismatches on IRR for a conventional RX has been shown in [12]. This section analyzes the sensitivity of IRR to the gain and phase mismatch in an eight-path HR RX. If $\alpha_0\alpha_1$ and $_{\alpha 2}$ are the gain mismatches in the 0°, 45°, and −45° paths and $\beta_0\beta_1$ and $_{\beta 2}$ denote the phase mismatches in the same three paths then

$$S_{0^\circ}(t) = (1+\alpha_0)\cos(\omega_{\rm LO}t+\beta_0) \tag{A1}$$
$$S_{45^\circ}(t) = (1+\alpha_1)\cos(\omega_{\rm LO}t+45^\circ+\beta_1) \tag{A2}$$
$$S_{-45^\circ}(t) = (1+\alpha_2)\cos(\omega_{\rm LO}t-45^\circ+\beta_2) \tag{A3}$$
$$S_{90^\circ}(t) = \cos(\omega_{\rm LO}t+90^\circ). \tag{A4}$$

Using (A1)–(A3) when the signals from the 0°, 45°, and −45° paths are weighted by $(1,\sqrt{2},1)$, the I channel output can be expressed as

$$\begin{aligned} I(t) &= S_{-45^\circ}(t)+\sqrt{2}S_{0^\circ}(t)+S_{45^\circ}(t)\\ &= (1+\alpha_1)\cos(\omega_{\rm LO}t+45^\circ+\beta_1)\\ &\quad+\sqrt{2}(1+\alpha_0)\cos(\omega_{\rm LO}t+\beta_0)\\ &\quad+(1+\alpha_2)\cos(\omega_{\rm LO}t-45^\circ+\beta_2)\\ &= \frac{(1+\alpha_1)}{2}(e^{j\omega_{\rm LO}t}e^{j(\beta_1-45^\circ)}+e^{-j\omega_{\rm LO}t}e^{-j(\beta_1-45^\circ)})\\ &\quad+\frac{\sqrt{2}(1+\alpha_0)}{2}(e^{j\omega_{\rm LO}t}e^{j\beta_0}+e^{-j\omega_{\rm LO}t}e^{-j\beta_0})\\ &\quad+\frac{(1+\alpha_2)}{2}(e^{j\omega_{\rm LO}t}e^{j(\beta_2+45^\circ)}+e^{-j\omega_{\rm LO}t}e^{-j(\beta_2+45^\circ)}). \end{aligned} \tag{A5}$$

Characterized by the same weighting factors, the signal at the Q channel can be constructed with 45° 90° and 135° (where the inverted −45° is used instead) and it can then be written as

$$\begin{aligned} Q(t) &= S_{45^\circ}(t)+\sqrt{2}S_{90^\circ}(t)-S_{-45^\circ}(t)\\ &= -\frac{(1+\alpha_1)}{2j}(e^{j\omega_{\rm LO}t}e^{j(\beta_1-45^\circ)}-e^{-j\omega_{\rm LO}t}e^{-j(\beta_1-45^\circ)})\\ &\quad-\frac{\sqrt{2}}{2j}(e^{j\omega_{\rm LO}t}-e^{-j\omega_{\rm LO}t})\\ &\quad-\frac{(1+\alpha_2)}{2j}(e^{j\omega_{\rm LO}t}e^{j\beta_2+45^\circ}-e^{-j\omega_{\rm LO}t}e^{-j(\beta_2+45^\circ)}). \end{aligned} \tag{A6}$$

TABLE IV
PERFORMANCE SUMMARY AND COMPARISON TABLE

| | **Andrews ISSCC 10[7][15]** | **Borremans ISSCC 11 [16]** | **Lu ISSCC 11 [17]** | **Murphy ISSCC 12[2][18]** | **Park ISSCC 14 [19]** | **Chen ISSCC 15 [20]** | **This work** |
|---|---|---|---|---|---|---|---|
| Architecture | Mixer-first | NC-LNA & Voltage mixer | Saw-less Narrowband | FTNC RX | RF-Feedback LNA | Reconfigurable SDR RX | Mixer-first |
| Frequency (GHz) | 0.1-2.4 | 0.4-6 | 0.85/0.9/1.8/1.9 | 0.08-2.7 | 0.05-2.5 | 0.5-3 | 0.4-3.5 |
| RF Input | Single-ended | Differential | Differential | Single-ended | Differential | Differential | Single-ended |
| Gain (dB) | 40-70 | 70 | 60 | 72 | 38 | 20-50 | 35 |
| Bandwidth | 2 MHz | 100 kHz | 100 kHz | - | 0.4-20 MHz | 1-30 MHz | 100 kHz-50 MHz |
| NF (dB) | 4±1 | 3 | 2.7-2.9 | 1.9/4 | 2.9 | 3.8-4.8 | 2.4-2.6 |
| NF w/ 0dBm Blocker (dB) | - | 15 (20 MHz@2 GHz) | 7 (80 MHz@2 GHz) | 4.1 (80 MHz@1.5 GHz) | 5.4 (23 MHz@2 GHz) | 8.3-9.3 (40 MHz@1 GHz) | 6.5 (50 MHz@2 GHz) |
| OB-IIP3 (dBm) | 25 (20 MHz@1 GHz) | 10 (20 MHz@2 GHz) | - | 13.5 | 10 | 10 (200 MHz@1 GHz) | 16 (50 MHz@2 GHz) |
| IIP2 (dBm) | 56 | 70 | >50 | 54 | - | - | >60 |
| P1dB (dBm) | 4 (40 MHz@1 GHz) | -8 (20 MHz@2 GHz) | 1 | -2 (50 MHz@2 GHz) | - | -9 (50 MHz@1 GHz) | 4 (50 MHz@2 GHz) |
| LO Leakage | - | - | N/A | - | - | N/A | <-62 dBm |
| Active Area | 2 $mm^2$ | 2 $mm^2$ | 1.4 $mm^2$ | 1.2 $mm^2$ | 0.82 $mm^2$ | 7.82 $mm^2$ | 0.23 $mm^2$ |
| Supply (V) | 1.2/2.5 | 1.1/2.5 | 2.8 | 1.3 | 1.2 | 1.2/2.5 | 1.1/1.5(LDO) |
| Power (mW) | 37-70 | 30-55 | 92.5 | 35-78 | 20 (@2 GHz) | RX: 96/168 LO: 54-194 | 38-75 |
| Technology | 65 nm | 40 nm | 65 nm | 40 nm | 65 nm | 65 nm | 28 nm |

Knowledge of the signal content in the positive sideband can be extracted from $I(t)+jQ(t)$ after substituting (A5) and (A6), resulting in

$$\begin{aligned} I+jQ =& \frac{\sqrt{2}(1+\alpha_0)}{2}\{e^{-j\omega_{LO}t}[(e^{-j\beta_0}+1)+(e^{j\beta_0}-1)]\} \\ &+\frac{(1+\alpha_1)}{2}\{e^{-j\omega_{LO}t}(e^{-j(\beta_1-45^\circ)}+e^{-j(\beta_1+45^\circ)}) \\ &\quad +e^{ij\omega_{LO}t}(e^{j(\beta_1-45^\circ)}-e^{j(\beta_1+45^\circ)})\} \\ &+\frac{(1+\alpha_2)}{2}\{e^{-j\omega_{LO}t}[e^{-j(\beta_2-45^\circ)}+e^{-j(\beta_2+45^\circ)}] \\ &\quad +e^{j\omega_{LO}t}[e^{j(\beta_2-45^\circ)}-e^{j(\beta_2+45^\circ)}]\}. \end{aligned} \tag{A7}$$

Due to the gain and phase mismatches, (A7) contains both the desired signal and the image leakage. By collecting the common terms, and (A7) can be rewritten as

$$I+jQ = S_{\text{Desired}}(t)+S_{\text{Leakage}}(t) \tag{A8}$$

$$\begin{aligned} S_{\text{Desired}}(t) =& \frac{1}{2}e^{-j\omega_{LO}t}[\sqrt{2}(1+\alpha_0)(e^{-j\beta_0}+1) \\ &+(1+\alpha_1)(e^{-j(\beta_1+45^\circ)}+e^{-j(\beta_1-45^\circ)}) \\ &+(1+\alpha_2)(e^{-j(\beta_2+45^\circ)}+e^{-j(\beta_2+45^\circ)})] \end{aligned} \tag{A9}$$

$$\begin{aligned} S_{\text{Leakage}}(t) =& \frac{1}{2}e^{j\omega_{LO}t}[\sqrt{2}(1+\alpha_0)(e^{j\beta_0}-1) \\ &+(1+\alpha_1)(e^{j(\beta_1+45^\circ)}-e^{j(\beta_1-45^\circ)}) \\ &+(1+\alpha_2)(e^{j(\beta_2+45^\circ)}-e^{j(\beta_2+45^\circ)})] \\ \approx& \frac{1}{2}e^{j\omega_{LO}t}\big[\sqrt{2}(1+\alpha_0)(j\beta_0-1) \\ &+j(1+\alpha_1)e^{j(45^\circ)}(\beta_2-\beta_1) \\ &+j(1+\alpha_2)e^{-j(45^\circ)}(\beta_1-\beta_2)\big]. \end{aligned} \tag{A10}$$

Output contained the desired signal at the positive half sideband is described by (A8), while (A10) is the undesired image leakage from the other sideband. If we assume that there are no mismatches, (A9) simply reduces to $2\sqrt{2}$, while (A10) disappears. Therefore,

$$|S_{\text{Desired}}|^2 = (2\sqrt{2})^2 = 8. \tag{A11}$$

Recognizing the fact that the gain or the phase mismatches of different paths have the same variances for statistical distribution ($\sigma_A^2$ for gain and $\sigma_\varphi^2$ for phase), the sensitivity of the IRR to gain and phase mismatches can then be derived from (A9)–(A11) as

$$\begin{aligned} \left|\frac{\partial S_{\text{Leakage}}}{\partial \sigma_A}\right|^2 &= \sigma_A^2\left[\frac{(e^{j(45^\circ)}-e^{j(-45^\circ)})^2+(e^{j(-45^\circ)}-e^{j(45^\circ)})^2}{4}\right] \\ &= 2\sigma_A^2\sin^2(45^\circ) \\ &= \sigma_A^2 \end{aligned} \tag{A12}$$

$$\begin{aligned} \left|\frac{\partial S_{\text{Leakage}}}{\partial \sigma_\varphi}\right|^2 &= 2\sigma_\varphi^2\left[\frac{(e^{j(45^\circ)})^2+(e^{j(-45^\circ)})^2+1}{4}\right] \\ &= 2\sigma_\varphi^2\left[\cos^2(45^\circ)-\frac{1}{4}\right] \\ &= \frac{\sigma_\varphi^2}{2} \end{aligned} \tag{A13}$$

$$\begin{aligned} \left|\frac{\partial \text{IRR}}{\partial \sigma_A}\right|^2 &= \frac{\left|\frac{\partial S_{\text{Leakage}}}{\partial \sigma_A}\right|^2}{|S_{\text{Desired}}|^2} \\ &= \frac{1}{8}\sigma_A^2 \end{aligned} \tag{A14}$$

$$\begin{aligned} \left|\frac{\partial \text{IRR}}{\partial \sigma_\varphi}\right|^2 &= \frac{\left|\frac{\partial S_{\text{Leakage}}}{\partial \sigma_\varphi}\right|^2}{|S_{\text{Desired}}|^2} \\ &= \frac{1}{16}\sigma_\varphi^2. \end{aligned} \tag{A15}$$

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