

A Yield Optimization Methodology for Mixed-Signal Circuits

Aikaterini Papadopoulou and Borivoje Nikolic

Berkeley Wireless Research Center, University of California at Berkeley, CA

Abstract—With technology scaling in the nanometer regime relative variability increases and becomes more complex, making traditional statistical modeling insufficient. To optimize yield, circuit designers need to determine effects of variations on particular circuit designs, which requires statistical modeling. This paper presents a methodology for simple, fast, design-specific yield optimization that is accessible to the circuit designer. The methodology utilizes backward propagation and convex optimization techniques to customize existing statistical model cards to a given design. The methodology is verified using comparator offset measurements on a 28nm FDSOI technology. The customized model achieves a mean absolute percentage error of $< 4\%$ compared to a 30% error in the original models.

Keywords—statistical modeling; yield optimization; design centering; process variation; circuit design

I. INTRODUCTION

Dimensional and functional scaling of CMOS processes is continuing to increase the analog circuit performance while decreasing cost [1]. While achieving extreme performance is now possible, it is often limited by an increase in variability due to shrinking of dimensions into the deep submicron regime. Both within-die and die-to-die relative variations are shown to increase when scaling from 90nm to 45nm [2] and are expected to increase even more as devices scale to sub-10nm, causing both traditional sources of variation, like random dopant fluctuations, to become more pronounced, and new sources of variation, like fin geometry variations or line edge roughness, to arise [3].

In response to the increase in variability, statistical modeling methods have been developed to help designers improve yield and, therefore, decrease cost. This involves starting with a large set of correlated model parameters and reducing to a smaller and more manageable set of uncorrelated parameters, typically using some variation of principal component analysis (PCA) [4]. In newer models some parameter correlations may be preserved in order to improve accuracy. Corner modeling involves extracting variation data from devices, and assigning values to the model parameters such that the device performance that is being measured is pushed n standard deviations away from its mean value. As variability rises, more corners become necessary in new models, including corners for analog design, based on device I-V curves, and corners for digital design, typically based on delay-chain measurements. Corner modeling is simple and computationally efficient, however in newer technologies it can result in overly optimistic or pessimistic results, as the nature of variability becomes more complex. Fig. 1 illustrates how pessimistic some of the model corners may be, comparing to a Monte-Carlo (MC) simulation in a 28nm FDSOI technology.

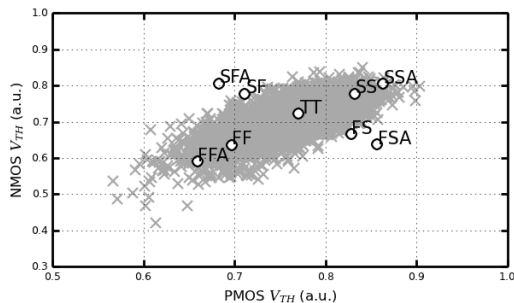


Fig. 1. Design space and corners derived from a 28nm FDSOI technology.

Another commonly used method for accounting for the impact of random variations on yield is Monte-Carlo simulation. Similarly, variation data are extracted from a set of devices. The data are then used to assign variances to a reduced set of model parameters, in order to represent the measured distribution. Similar to corner modeling, I-V data are typically used for this, and therefore topology-specific and layout-induced effects are ignored.

II. RELATED WORK

Shortcomings of traditional variation modeling approaches have given rise to exploration of design-specific or performance-aware modeling. The main concept is illustrated in Fig. 2 and involves identifying the actual design space and moving the design in order to increase the margin from failure. In [5] the authors apply backpropagation of variance in order to evaluate model parameter variances based on measurements. Though a generally efficient model for simple systems, its dependency on handpicked parameters and complexity when a large number of parameters are needed limit its applicability. Other approaches involve design-specific corner extraction employing convex semi-definite programming [6] or using simulation data to train accurate circuit-specific non-linear models [7]. These represent design-specific variation more accurately, but are far complex for practical designs.

In this paper, we present a methodology for optimizing statistical models customized to a given class of designs. The methodology builds on the existing body of modeling, employs the backward propagation of variance technique to improve the variation assigned to each model variable, performs automated parameter selection and is adapted to include existing model parameter correlations. We then formulate the problem as a constrained convex optimization problem, including parameter selection as well as the addition of physical, model-derived constraints by the designer. This enables the creation of

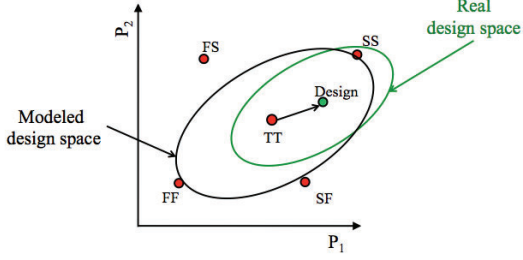


Fig. 2. Illustration of design centering

customized model cards for robust design of high-performance circuit blocks and rapid yield ramp-up in highly scaled technologies. We validate the approach on a 28nm FDSOI technology and demonstrate significant yield prediction improvement when design-specific customized models are used.

III. CENTERING ALGORITHM

A. Mathematical Formulation

Given a set of device models, we can represent any circuit output vector $\mathbf{y} = [y_1, \dots, y_m]^T$ as a function of the model parameter vector $\mathbf{p} = [p_1, \dots, p_n]^T$ as $\mathbf{y} = f(\mathbf{p})$. In order to incorporate variability to the models, each of the parameters in \mathbf{p} is treated as an independent random variable (RV) P_i and assigned a normal distribution with standard deviation σ_i , $i = 1, \dots, n$, and therefore we have:

$$\mathbf{Y} = f(\mathbf{P}) \quad (1)$$

Assuming small perturbations and taking the Taylor expansion around the nominal point \mathbf{P}_0 of (1) we get:

$$\begin{aligned} \mathbf{Y} &= f(\mathbf{P}_0) + \mathbf{J} \cdot \Delta\mathbf{P} \Rightarrow \\ \Delta\mathbf{Y} \cdot \Delta\mathbf{Y}^T &= \mathbf{J} \cdot \Delta\mathbf{P} \cdot \Delta\mathbf{P}^T \cdot \mathbf{J}^T \Rightarrow \\ \mathbf{R}_{\Delta\mathbf{Y}} &= \mathbf{J} \cdot \mathbf{R}_{\Delta\mathbf{P}} \cdot \mathbf{J}^T \end{aligned} \quad (2)$$

where $\mathbf{R}_{\Delta\mathbf{Y}}$, $\mathbf{R}_{\Delta\mathbf{P}}$ the autocorrelation matrices of $\Delta\mathbf{Y}$ and $\Delta\mathbf{P}$, respectively. Since P_i are independent, the matrix $\mathbf{R}_{\Delta\mathbf{P}}$ is diagonal. Denoting the k^{th} unit vector \mathbf{u}_k as a vector with all zeros except a one on the k^{th} row, we can derive an expression for the k^{th} diagonal element of $\mathbf{R}_{\Delta\mathbf{Y}}$ by using (2):

$$\sigma_{\Delta Y_k}^2 = \mathbf{u}_k^T \cdot \mathbf{R}_{\Delta\mathbf{Y}} \cdot \mathbf{u}_k = \mathbf{u}_k^T \cdot \mathbf{J} \cdot \mathbf{R}_{\Delta\mathbf{P}} \cdot \mathbf{J}^T \cdot \mathbf{u}_k \quad (3)$$

Let $\mathbf{v}_k^T = \mathbf{u}_k^T \cdot \mathbf{J}$, where $k = 1, \dots, m$. It is evident that \mathbf{v}_k^T is the k^{th} row of the Jacobian matrix \mathbf{J} . From the above, we can now transform the problem to a linear optimization problem of the form $\mathbf{b} = \mathbf{A} \cdot \mathbf{x}$, relating the variances of the outputs on the left-hand side to the squares of the sensitivities and the input variances on the right-hand side.

$$\underbrace{\begin{pmatrix} \sigma_{\Delta y_1}^2 \\ \sigma_{\Delta y_2}^2 \\ \vdots \\ \sigma_{\Delta y_m}^2 \end{pmatrix}}_{\mathbf{b}} = \underbrace{\begin{pmatrix} J_{11}^2 & J_{12}^2 & \dots & J_{1n}^2 \\ J_{21}^2 & J_{22}^2 & \dots & J_{2n}^2 \\ \vdots & \vdots & \ddots & \vdots \\ J_{m1}^2 & J_{m2}^2 & \dots & J_{mn}^2 \end{pmatrix}}_{\mathbf{A}} \cdot \underbrace{\begin{pmatrix} \sigma_{\Delta p_1}^2 \\ \sigma_{\Delta p_2}^2 \\ \vdots \\ \sigma_{\Delta p_n}^2 \end{pmatrix}}_{\mathbf{x}} \quad (4)$$

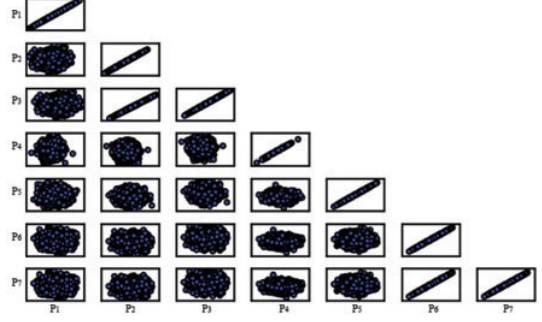


Fig. 3. Scatter plots of a subset of the parameters used.

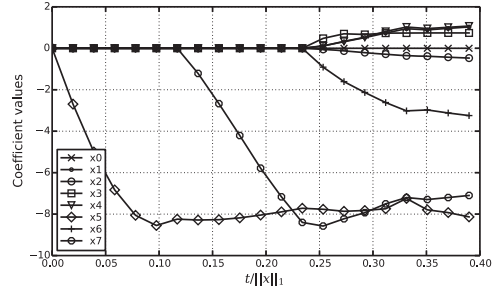


Fig. 4. Elastic net solution with $\rho = 0.5$ on artificially generated data.

Although typically PCA is used in order to get an independent model parameter set, in some cases parameter correlations may be preserved by the models, which is the case with some of the models used in this work (Fig. 3). As long as the covariance of the correlated parameters can be calculated using the given model, the above function can be altered to incorporate correlations. If, for example, two parameters with indices u and v are correlated, a term $2 \cdot J_{ku} \cdot J_{kv} \cdot cov(\Delta p_u, \Delta p_v)$ is added to the right-hand side of the equation for the k^{th} output variance. From here, given a set of observations of the output vector extracted by test structures, we can calculate the variances of the parameters by solving (4).

B. System solution

The resulting $m \times n$ system of equations has, in the general case, more inputs than outputs ($m < n$), therefore it is an underdetermined system with an infinite number of solutions. Commercial solvers typically return a minimum norm solution to such problems. However, in circuit design there is only a limited set of solutions that are physically acceptable, and a minimum norm solution may not be one of them. Model parameters typically need to be constrained in order to fit the given model specifications. Additionally, we can exploit the fact that the sensitivity matrix will have some degree of sparseness, depending on the given design, which means that some parameters may be eliminated without significant loss of accuracy.

In order to achieve both parameter shrinkage and selection, we use regularization via the elastic net [8]. The elastic net

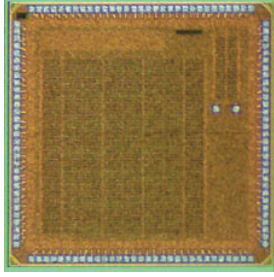


Fig. 5. Die photo of the designed testchip.

formulation is shown in Eq. 5.

$$\begin{aligned} & \text{minimize } \|\mathbf{b} - \mathbf{A} \cdot \mathbf{x}\|_2^2 \\ & \text{subject to } (1 - \rho)\|\mathbf{x}\|_1 + \rho\|\mathbf{x}\|_2 < t \end{aligned} \quad (5)$$

This type of regularization constraints the l_2 -norm of the solution, like ridge regression, which helps shrink large coefficients to reduce overfitting, and also constraints the l_1 -norm both for shrinkage and parameter selection. Fig. 4 shows the magnitude of the coefficients for different values of t . We observe that as a stricter constraint is applied to t , more and more coefficients are forced to zero, while the magnitude of the non-zero coefficients converges for higher values of t .

IV. CUSTOMIZED MODELS

In order to validate the methodology for AMS circuit design data-extraction test structures were implemented in a 28nm FDSOI technology (Fig. 5). The test structure of choice is a strong-arm comparator, one of the most widely used mixed-signal circuits. The performance chosen was comparator offset, which was measured after noise averaging from 224 comparators per die, organized in a compact array structure (Fig. 6). Statistical parameters were assigned to all devices except the pre-charge devices (Fig. 7) for simulation speedup, as they do not affect offset. Measurement acquisition, circuit simulation and model customization were controlled entirely by Python.

The Jacobian matrix was extracted from the given simulation model using finite differences. Table I shows the extracted percent sensitivities of the output with respect to various model parameters assigned to each device, and therefore contains the elements of matrix \mathbf{J} . The resulting optimization problem of

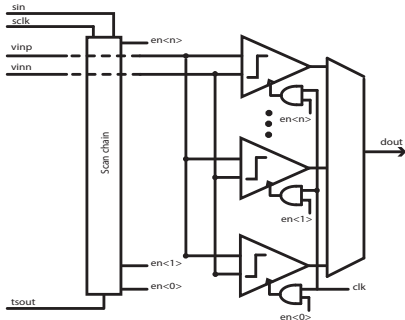


Fig. 6. Offset characterization array.

TABLE I. COMPARATOR OFFSET SENSITIVITY TO STATISTICAL PARAMETERS

Instance:	N_{in1}	N_{in2}	N_{cc1}	N_{cc2}	P_{cc1}	P_{cc2}
p_1	-1.018	1.018	-0.491	0.491	0.107	-0.107
p_2	1.890	-1.890	0.810	-0.777	-0.864	0.799

Eq. 5 is then solved using a commercially available convex programming package. Parameter ρ is set to 0.5 and parameter t is selected such that the root-mean-square error remains small. An explicit constraint of $\mathbf{x} \geq 0$ is added, since the unknowns represented parameter variances (Eq. 4).

Fig. 8 shows a comparison of the histograms extracted by simulation using both the original and customized models at two different supply voltages and Fig. 9 shows the corresponding quantile-quantile plots. It is evident that for the customized model the predicted distribution matches more accurately both the body and the tails of the measured data, comparing to the original models. The measured standard deviation of the offset

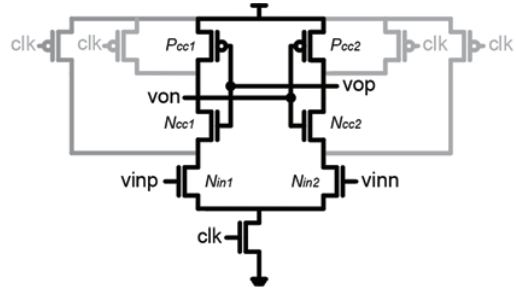


Fig. 7. Strong-arm latch used for design centering. The greyed-out devices were not assigned statistical parameters.

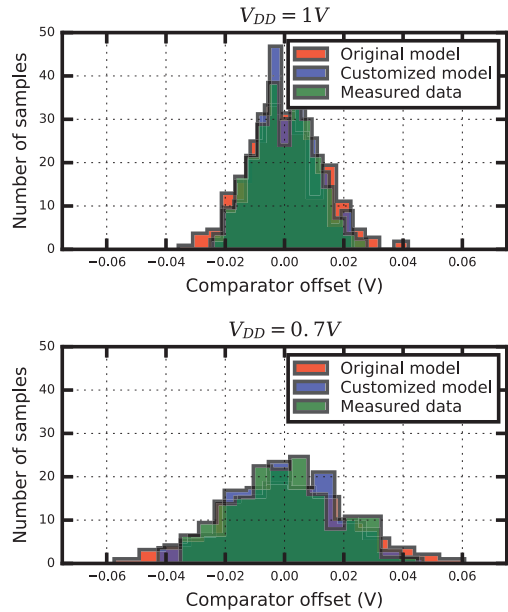


Fig. 8. Comparison of histograms predicted by the original and customized models at nominal and scaled supply voltage.

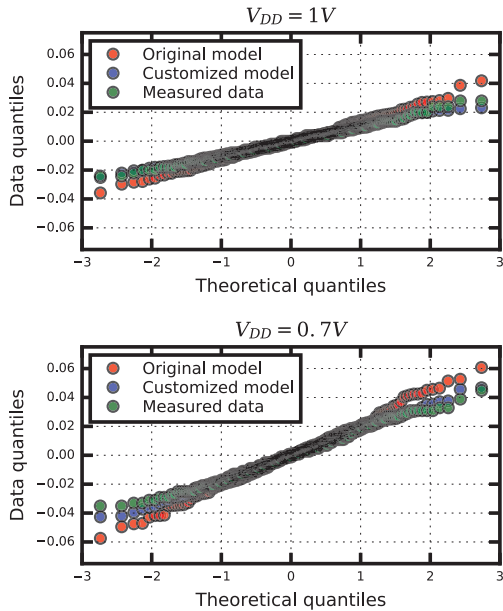


Fig. 9. Comparison of QQ plots predicted by the original and customized models at nominal and scaled supply voltage.

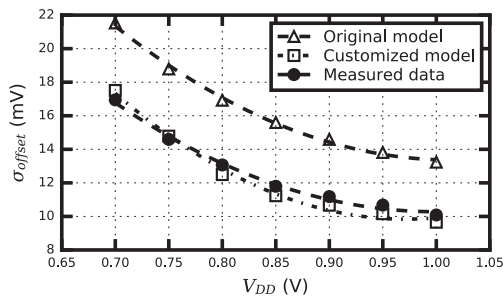


Fig. 10. Comparison of offset standard deviation across supply voltage, when the customized model is calibrated at each voltage step.

across different supplies is shown in Fig. 10, where design centering is applied at each step of the supply voltage, showing superior performance of the customized models. The presented methodology allows design centering at various supplies and biases, however it may be more practical for the designer to select a few supply/bias points to use. Fig. 11 shows the same as Fig. 10, but in this case the model are customized using only one supply point. We observe that although at scaled supplies the offset prediction deviates from the measured data, the customized model still remains superior to the original one. Table II summarizes the mean absolute percentage error of each model.

TABLE II. MEAN ABSOLUTE PERCENTAGE ERROR COMPARISON

	Original model	Customized model (all supplies)	Customized model (nominal supply)
$V_{DD} = 1V$	-30.1%	3.96 %	3.96 %
$V_{DD} = 0.7V$	-28.7%	-4.79 %	11.4 %

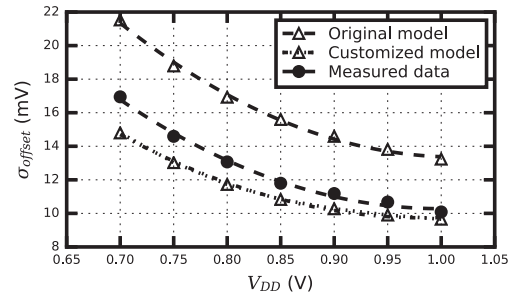


Fig. 11. Comparison of offset standard deviation across supply voltage, when the customized model is calibrated only at nominal supply.

V. CONCLUSION

This paper presented a methodology for centering of mixed-signal integrated circuits by customizing models to a specific design. The goal is to shorten the design manufacturing process by designing dedicated test structures to enable model customization and yield optimization at an early design stage.

The methodology uses backward propagation of variance and formulates the problem as a regularization problem that is easily and robustly solvable by commercial convex programming tools. The system solution consists of the parameter variances needed to customize the models. We demonstrate the methodology's capability of improving accuracy of the output distributions and reducing the error. This methodology enables the designer to utilize data from test structures in order to create performance-aware models to account for variability, including topology and layout-specific effects.

ACKNOWLEDGMENT

The authors wish to acknowledge the contributions of the students, faculty and staff of the Berkeley Wireless Research Center, wafer fabrication donation of STMicroelectronics, and funding in part by the Semiconductor Research Corporation (SRC).

REFERENCES

- [1] *International semiconductor technology roadmap*, www.itrs.net
- [2] L.T. Pang et al., "Measurement and Analysis of Variability in 45 nm Strained-Si CMOS Technology", *IEEE JSSCC*, Aug. 2009
- [3] A. Asenov, "Simulation of statistical variability in nano MOSFETs", *VLSI Symp. Tech. Dig.*, Jun. 2006
- [4] J.A. Power et al., "Relating Statistical MOSFET Model Parameter Variabilities to IC Manufacturing Process Fluctuations Enabling Realistic Worst Case Design", *IEEE Trans. Semiconductor Manufacturing*, Aug. 1994
- [5] C.C. McAndrew, "Statistical modeling for circuit simulation", *Proc. IEEE ISQED*, 2003
- [6] H. Zhang et al., "Efficient Design-Specific Worst-Case Corner Extraction for Integrated Circuits", *ACM/IEEE DAC*, 2009
- [7] T. McConaghy et al., "CAFFEINE: template-free symbolic model generation of analog circuits via canonical form functions and genetic programming", *Proc. ESSCIRC*, 2005
- [8] H. Zou et al., "Regularization and variable selection via the elastic net", *Journal of the Royal Statistical Society*, 2005