Implementing Memristor Based Chaotic Circuits

Bharathwaj Muthuswamy

Electrical Engineering and Computer Sciences
University of California at Berkeley

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1 Introduction

The memristor was postulated as the fourth circuit element by Leon O. Chua in 1971 [2]. It thus took its place along side the rest of the more familiar circuit elements such as the resistor, capacitor, and inductor. The common thread that binds these four elements together as the four basic elements of circuit theory is the fact that the characteristics of these elements relate the four variables in electrical engineering (voltage, current, flux and charge) intimately. Fig. 1 shows this relationship graphically [1].

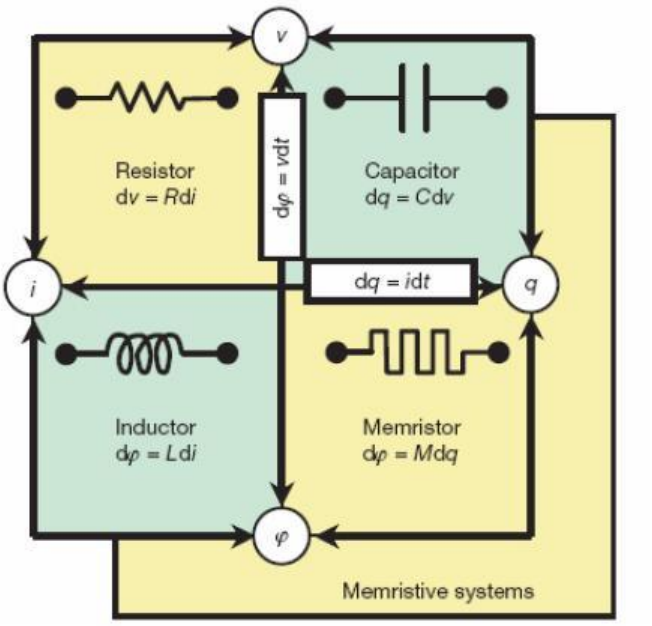


Figure 1: The four basic circuit elements

The memristor is a two terminal element, in which the magnetic flux (ϕ) between the terminals is a function of the electric charge that passes through the device [1] [3]. The memristor M used in this work is a flux controlled memristor that is characterized by its incremental menductance [1] function $W(\phi)$ describing the flux-dependent rate of change of charge:

$$W(\phi) = \frac{dq(\phi)}{d\phi} \tag{1}$$

The relationship between the voltage across ($v(t)$) and the current through ($i(t)$) the memristor is thus given by:

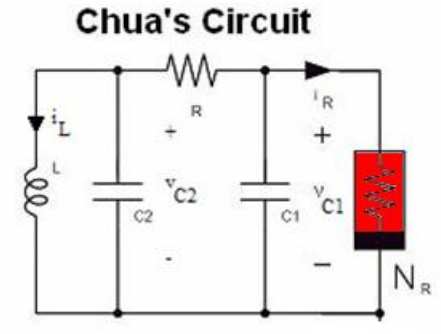
$$i(t) = W(\phi(t))v(t) \tag{2}$$

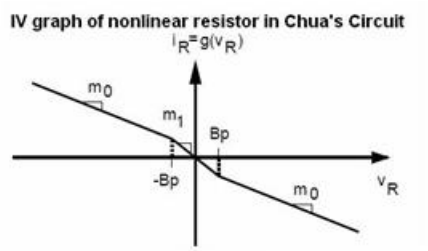
Memristor is an acronym for *memory-resistor* because in Eq. 2, since $W(\phi(t)) = W(\int v(t))$, the integral operator on the menductance function means the function *remembers* the past history of voltage values. Of course, if $W(\phi(t)) = W(\int v(t)) = constant$, a memristor is simply a resistor. For over thirty years, the memristor was not significant in circuit theory. In 2008, Williams et. al. [1] fabricated a solid state implementation of the memristor and thereby cemented its place as the 4th circuit element. They used two titanium dioxide films, with varying resistance which is dependent on how much charge has been passed through it in a particular direction. As a result of this realization, it is possible to have nonvolatile memory on a nano scale. However, as of the writing of this report, memristors are commercially unavailable. Therefore, this report proposes an analog circuit implementation of a memristor. This memristor is used to synthesize a chaotic circuit on a breadboard. To our knowledge, this is the first breadboard implementation of a memristor and a chaotic circuit based on the memristor. The report is organized as follows: the next section gives an overview of the memristor based chaotic circuit. Section 3 then describes the practical implementation of the memristor. Section 4 shows the limit cycles and strange attractors obtained from this circuit. Section 5 is the conclusions followed by acknowledgments and references.

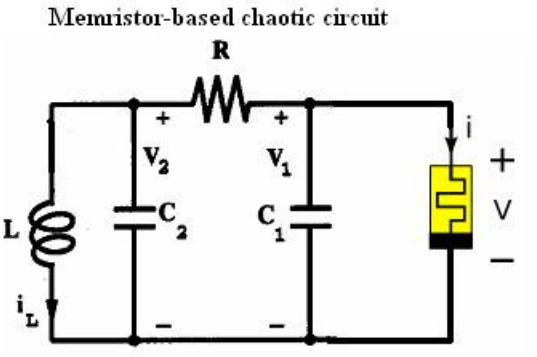
2 Overview of Canonical Memristor Based Chaotic Circuit

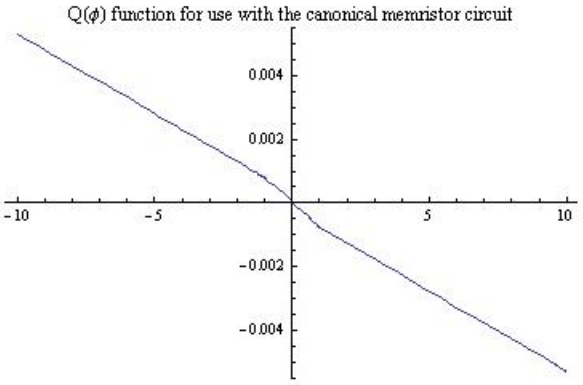
Refering to Table 1, we derived the memristor-based chaotic circuit by simply replacing the nonlinear resistor in Chua's circuit [4] with a flux-controlled memristor. Note that we derived the menductance nonlinearity by using the constraint of hyperbolic equilibrium points (condition 1 of Shilnikov's Theorem [4]).

Table 1: In order to obtain the memristor based chaotic circuit, we replaced the nonlinear resistor in Chua's circuit with a memristor.







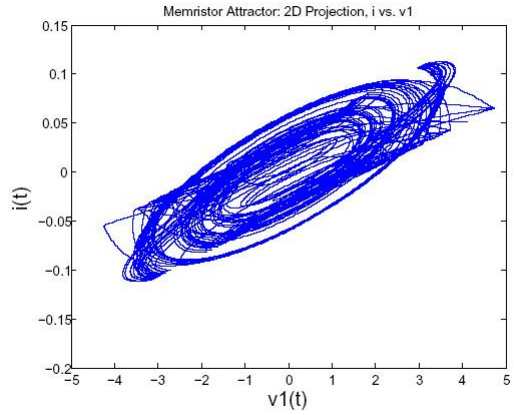


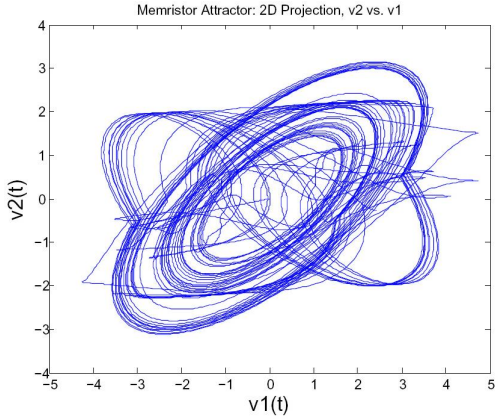
The equations governing our memristor-based chaotic circuit are:

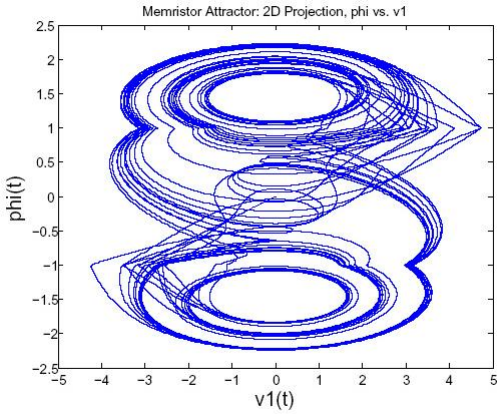
$$\begin{aligned}
\frac{d\phi}{dt} &= v_1(t) \\
\frac{dv_1(t)}{dt} &= \frac{1}{C_1}\left(\frac{v_2(t)-v_1(t)}{R} - W(\phi(t))\cdot v_1(t)\right) \\
\frac{dv_2(t)}{dt} &= \frac{1}{C_2}\left(\frac{v_1(t)-v_2(t)}{R} - i(t)\right) \\
\frac{di_L(t)}{dt} &= \frac{v_2(t)}{L}
\end{aligned} \tag{3}$$

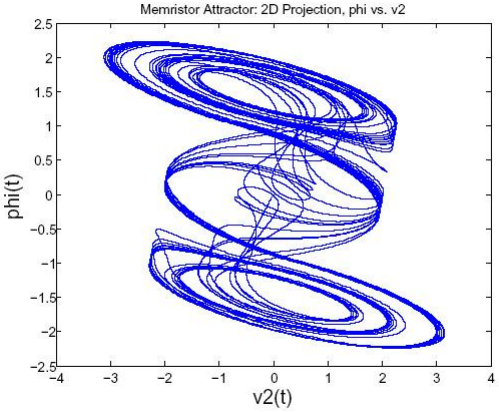
The intuitive justification for dimensional extension is that an active nonlinearity is very important for obtaining a chaotic circuit. The dimensional extension not only preserves the active nonlinearity, it also introduces another nonlinearity in terms of the product $(W(\phi(t))v_1(t))$ in the equation above. These two nonlinearities should combine to give rise to chaos, as we observed. We call this the *canonical memristor based chaotic circuit* since the circuit has been derived from the canonical Chua's circuit. For details such as Lyapunov exponents please refer to [3].

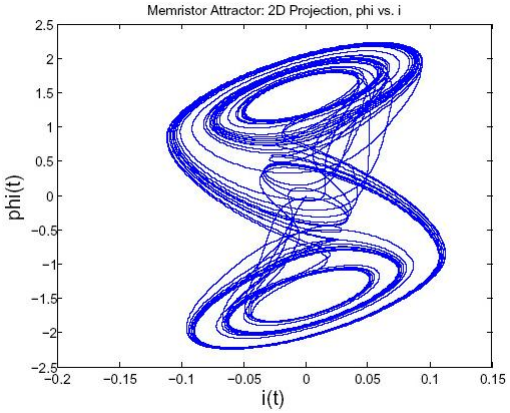
Table 2: Attractors from the state-scaled canonical memristor-based circuit

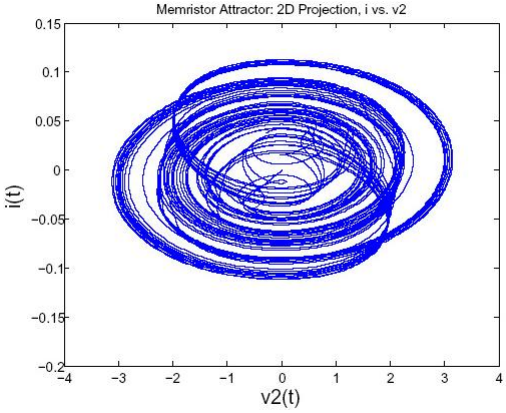












3 Practical Implementation of the Memristor and the Chaotic Circuit

Since the circuit proposed in the previous section has been *derived* from Chua's circuit, it is possible that replacing the *piecewise-linear menductance* with a *smooth menductance a'la* Zhong [5] should still result in chaotic behavior. The advantage of the smooth menductance nonlinearity is that it can be easily synthesized, as this section shows.

Consider the $Q(\phi)$ given below.

$$Q(\phi) = \alpha\phi + \beta\phi^3 \tag{4}$$

The expression for $i_m(t)$ can be derived from Eq. 4 and basic definitions Eqs. 1 and 2:

$$\begin{aligned} i_m(t) &= \frac{dq}{d\phi}\frac{d\phi}{dt} \\ &= \frac{d}{d\phi}\left(\alpha\phi + \beta\phi^3\right)\cdot v(t) \\ &= \left(\alpha + \beta\cdot 3\phi^2\right)\cdot v(t) \\ &= W(\phi(t))\cdot v(t) \end{aligned}$$

Since $\phi(t) \triangleq \int v(t)dt$, we have the following expression for the current through our memristor with a cubic nonlinearity:

$$i_m(t) = \left(\alpha + \beta\cdot 3\left(\int v(t)dt\right)^2\right)\cdot v(t) \tag{5}$$

The basic circuit to realize the current expression above is the multiplier circuit in a feedback loop from [5]. A block diagram view of the circuit along with an integrator is shown in Fig. 2. The circuit in Fig. 2 is the analog implementation of our memristor. In Fig. 2, $U1$ is the integrator for implementing $\phi(t) = \int v(t)dt$. $U2$ is the multiplier that implements $\frac{\phi(t)^2}{10}$. Multiplier $U3$ implements $\frac{\phi(t)^2}{10}\cdot\frac{v(t)(R_4+R_5)}{10\cdot R_4}$. Refer to the AD633 four-quadrant analog multiplier datasheet for further information. $U4$, op-amp AD711kN, is the current inverter and implements the function (if $R_1 = R_2$):

$$i(t) = \frac{-v}{R_3} + \left(\frac{\left(\int v(t)dt\right)^2}{10}\frac{v\cdot(R_4+R_5)}{10\cdot R_4}\right)\frac{1}{R_3} \tag{6}$$

In Eq. 5, we will choose $\alpha = -0.599\cdot 10^{-3}$ and $\beta = 0.0218\cdot 10^{-3}$. These parameters were obtained from [5]. For these parameters, a Mathematica plot of the charge versus flux and the menductance function is shown in Fig. 3. Using the values of α and β in Eq. 6, we get the following values for the components in Fig. 2: $R_1 = R_2 = 2k,\ R_3 = 1.69k,\ R_4 = 30k,\ R_5 = 29k$. Practically speaking,

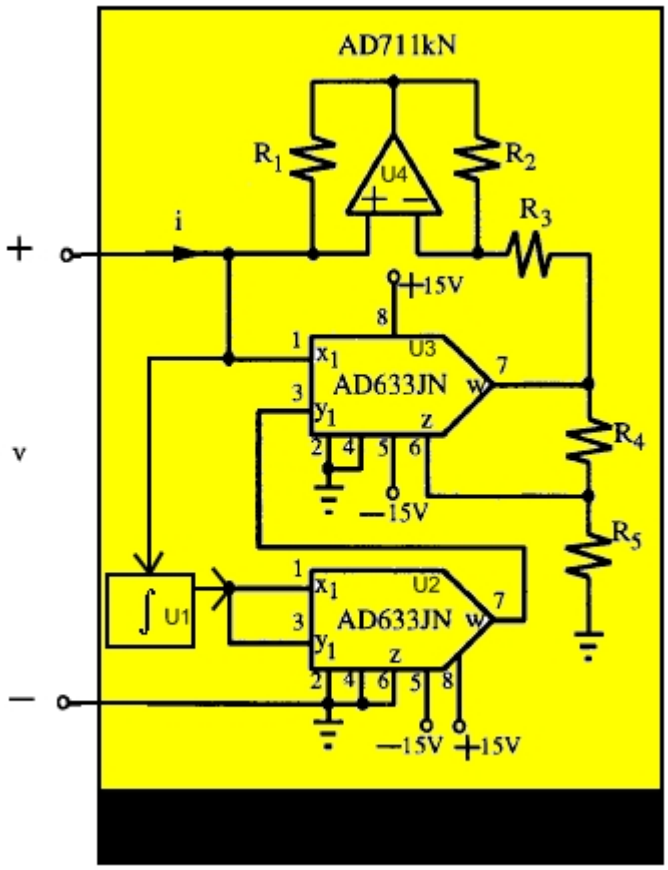


Figure 2: Practical Circuit for Realizing a memristor.

$R_4 > 1\ k\Omega$ and $R_5 < 100\ k\Omega$ [5]. Now, the "memory" for the system is in the integrator in Eq. 6. Therefore, in order to realize a practical integrator circuit we rescaled the state variables in Eq. 3 to get the equations below.

$$\begin{aligned}
\frac{d\phi}{dt} &= -1000 \cdot v_1(t) \\
\frac{dv_1(t)}{dt} &= \frac{1}{C_1}\left(\frac{v_2(t)-v_1(t)}{R} - (\alpha + \beta 3 \cdot \phi^2) \cdot v_1(t)\right) \\
\frac{dv_2(t)}{dt} &= \frac{1}{C_2}\left(\frac{v_1(t)-v_2(t)}{R} - i(t)\right) \\
\frac{di_L(t)}{dt} &= \frac{v_2(t)}{L}
\end{aligned} \tag{7}$$

The menductance parameters have already been defined. The circuit parameters

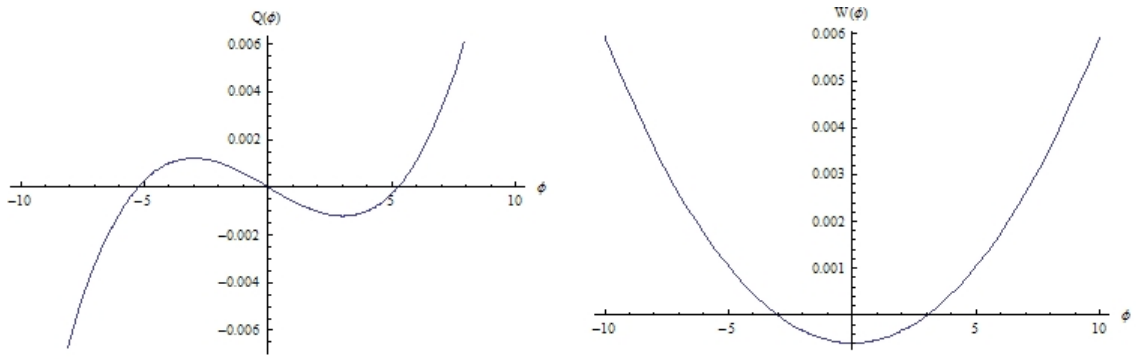


Figure 3: Plot of Charge vs. Flux along with a plot of the menductace function for our memristor

in Eq. 7 are $C_2 = 68\ nF,\ C_1 = 6.8\ nF,\ L = 18\ mH$ (parameters from [5]). We now have all the parameters necessary to synthesize the circuit. The complete circuit schematic is shown in Fig. 4. We use a voltage buffer $U1_1$ to avoid loading effects.

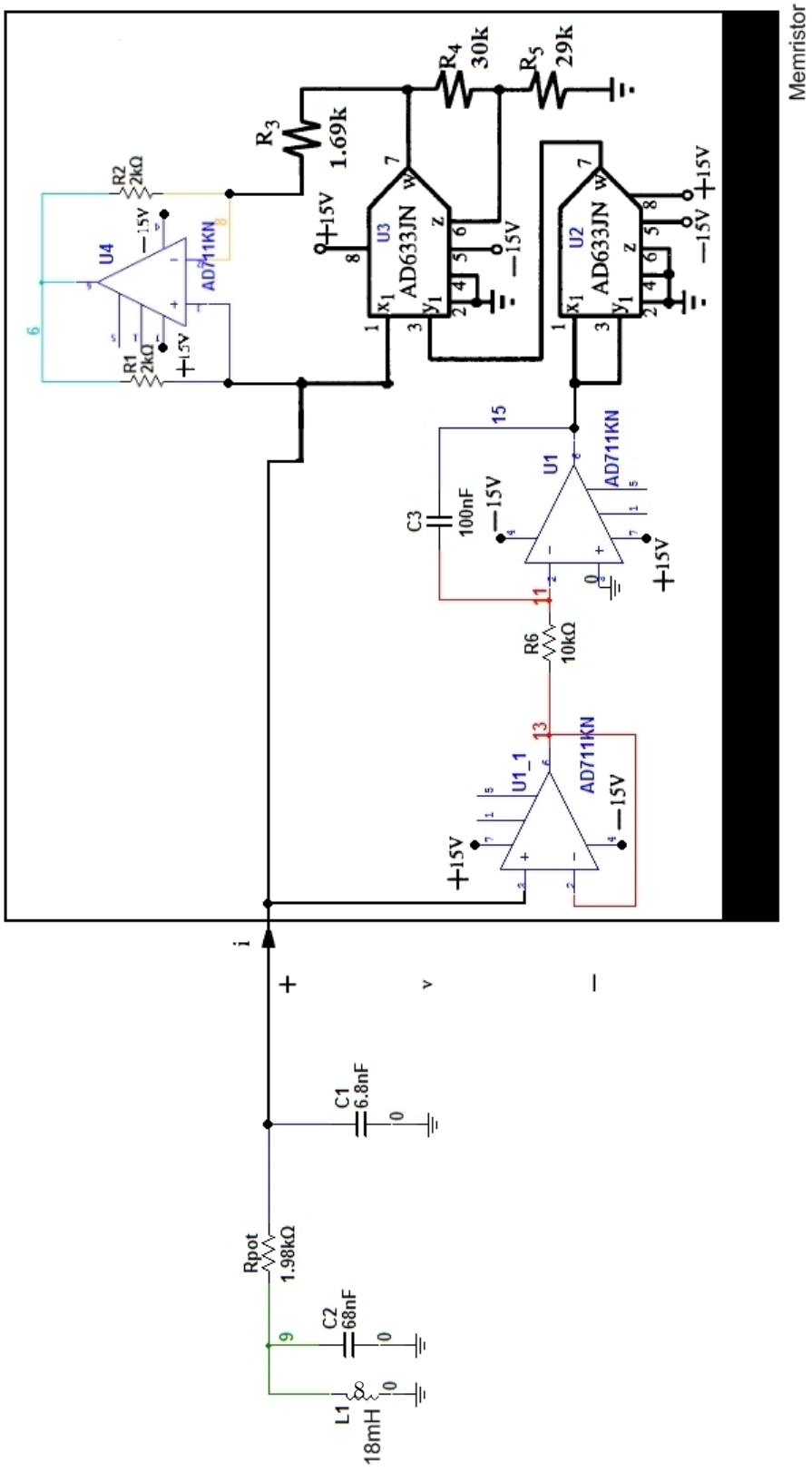


Figure 4: Schematic of the memristor based chaotic circuit.

4 Limit Cycles, Strange Attractors and Power Spectra from the Memristor Chaotic Circuit

Fig. 5 shows a limit cycle and a chaotic attractor from the memristor based chaotic circuit. The images were taken using a Agilent Intuilink and National Instruments software. The oscilloscope used is an Agilent 54600D.

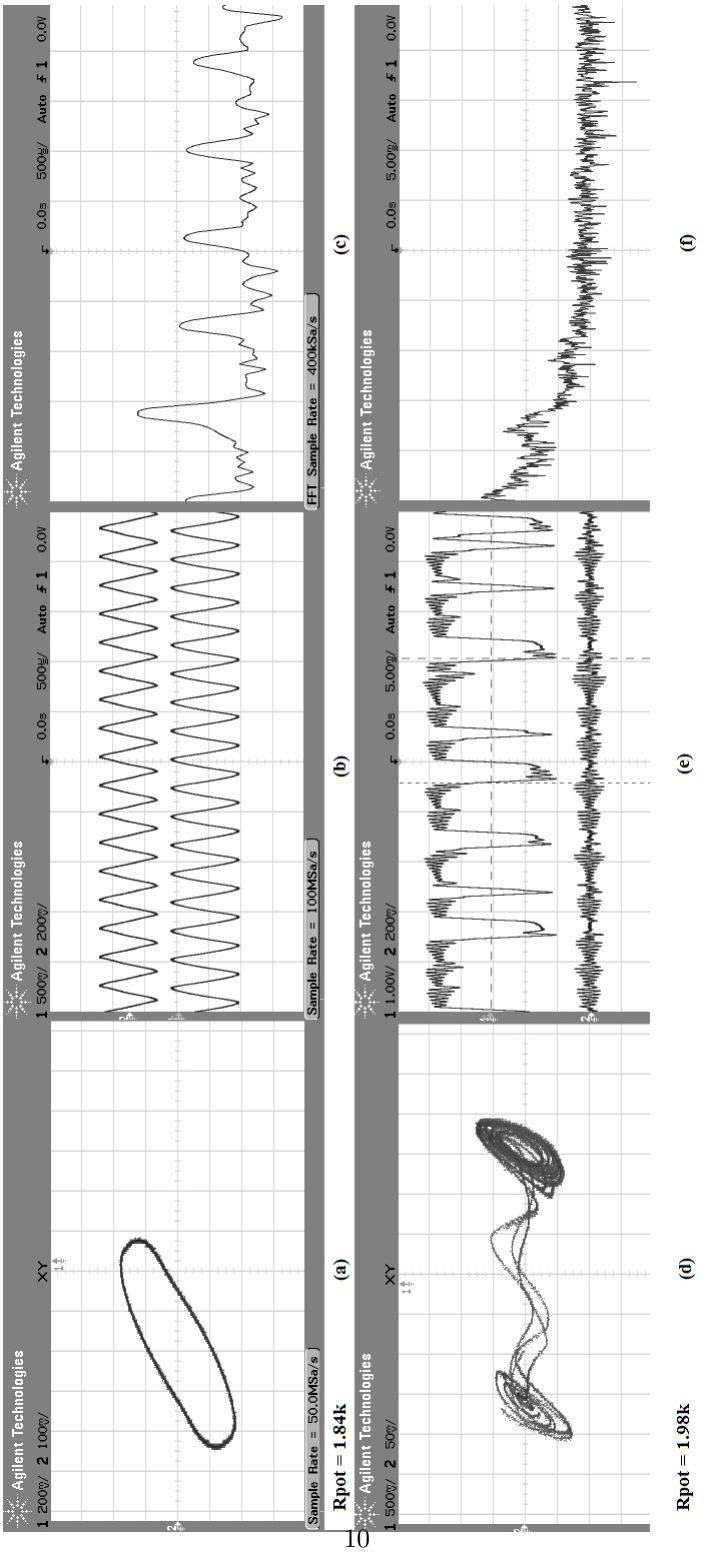


Figure 5: Phase plot, time domain waveforms and power spectra for a limit cycle and a strange attractor from the memristor based chaotic circuit. Channel 1 (X) is across $\phi(t)$ (Node 15 in Fig. 4) and Channel 2 (Y) is across $v_2(t)$ (Node 9 in Fig. 4).

Notice the difference in the frequency spectra between the limit cycle and the attractor. The fourier transform suggests that the limit cycle is periodic. The frequency spectrum of the attractor is wideband, suggesting chaotic behavior.

5 Conclusions

In this report we have proposed a practical circuit for realizing a memristor and a chaotic circuit based on the memristor. The advantage of this circuit is that polynomial menductance functions could be implemented using more analog multipliers. It would be interesting to implement memristor chaotic ircuits with higher order menductance functions.

6 Acknowledgments

The author would like to thank Dr. Leon O. Chua for his guidance and support.

References

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