INPUT/OUTPUT BUFFERS FOR ASP

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Abstract

A well characterized library of Input/Output (I/O) buffers is presented in this document. The library was designed for the Advanced Silicon compiler in Prolog (ASP). This document outlines the basic steps used to develop the buffers and also discusses general design issues for I/O buffers. Finally, there is a discussion of future trends in I/O buffer design.

Acknowledgements

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1. Introduction

This report describes my investigation of the design and implementation of I/O buffers for ASP. The Advanced Silicon compiler in Prolog (ASP) [10] is an automatic translation tool based on Prolog – a computer programming language that is used for solving problems that involve *objects* and the *relationships* between objects. ASP converts a behavioral description to a mask level description. The designer is not required to be familiar with Metal Oxide Semiconductor (MOS), circuits or physical layout design.

Of all the aspects of chip design and layout, Input/Output (I/O) buffer design requires the most amount of expertise. Our I/O buffers are designed to be TTL compatible. They serve as building blocks for the I/O frame of any VLSI design generated by ASP. The design is based on 1.2um Hewett Packard process technology. As process technology advances, the minimum feature size of a Complementary Metal Oxide Semiconductor (CMOS), becomes smaller. To make the design somewhat technology independent, circuit layout was done on the Magic [9] layout system with scalable CMOS technology. Layout in Magic is done on virtual grids. Each grid unit represents one lambda unit which in turn is equal to half of the minimum physical feature size. With technology changes, the physical geometry of the layout is preserved by changing the physical dimension represented by one virtual grid. However, electrical parameters of the I/O buffers, such as rise and fall times, must be extracted from circuit simulation in order to fully characterize the buffers. Refer to the section on design in this report for further discussion.

2. Tools and Techniques

I made extensive use of Computer-Aided Design (CAD) tools in every phase of the design and implementation of the I/O buffers. Use of these tools was essential due to the complexity and accuracy required for the design.

To obtain an accurate simulation result, the circuit simulator BSIM was used, instead of the more popular SPICE circuit simulator. BSIM simulation was performed to carry out the functionality check and extract the timing parameters of the I/O buffers. As the design was refined, the BSIM simulations were made more detailed, eventually reflecting in most cases the actual circuit implementation to the layout level.

The Magic layout system was used to generate the I/O buffer cell layout. An interactive Design Rule Checker (DRC) was used to check design rule violations. The feature size of Magic is based on a lambda unit. The minimum feature size is represented by two lambda units. In our case, the minimum feature size is 1.2um, therefore one lambda equals to 0.6um. As process technology advances, the minimum feature size and the lambda representation will get smaller. The geometry in magic is represented in lambda units and the geometry preserves its relative position and size with process scaling. Therefore, except for bonding pad area, the physical geometry is scalable over a range of values for lambda. Using Magic, switch-level simulation files used to verify functionality were extracted from the layout for RSIM.

3. Design

In this section, I discuss the I/O buffer design in a top-down structure starting from functionality. Following this discussion I describe several issues involving circuit protection and power and ground requirements. Appendix B and C include a library of I/O buffers for ASP and characterization and physical layout of the buffers.

It is common to design I/O buffers with constant height and width, i.e. pitch matching. The width of the buffers is determined by the minimum distance which two bonding wires can be placed next to each other. This distance is called the pitch, and is 175um in this design. In the HP 1.2um technology, the width of an I/O buffer is calculated as follow:

$$width = \frac{pitch}{minimum\_feature\_size}$$

$$width = \frac{pitch}{(\lambda/2)}$$

If the pitch or the minimum feature size changes, one can always calculate the width of an I/O buffer according to the above equations. There are fixed positions for Vdd and ground rails. Two power rails and two ground rails are fed through each cell horizontally.

The I/O buffer library consists of output pads, input pads, a power pad, a ground pad, a corner pad and a space pad. In the functionality description, I discuss the usage of each pad. Another critical factor in designing I/O buffer is circuit protection. In this section, I discuss various circuit protection techniques used to guard against electro-static discharge (ESD) and over-voltage on the chip pins. Inductance of a bonding wire causes power and ground bounce, which is very undesirable in circuit operation. A section is dedicated to the discussion of issues relating to power and ground bounce.

3.1. Functionality

The basic function of an I/O buffer is to interface the chip to the outside world. This section contains descriptions of output buffers (direct output buffers, tri-state output buffers and bi-directional output buffers), input buffers (a direct input buffer and a clock driver) and other pads, such as the power pad, the ground pad, the corner pad and the space pad. I will concentrate the discussion on buffers to drive TTL loads.

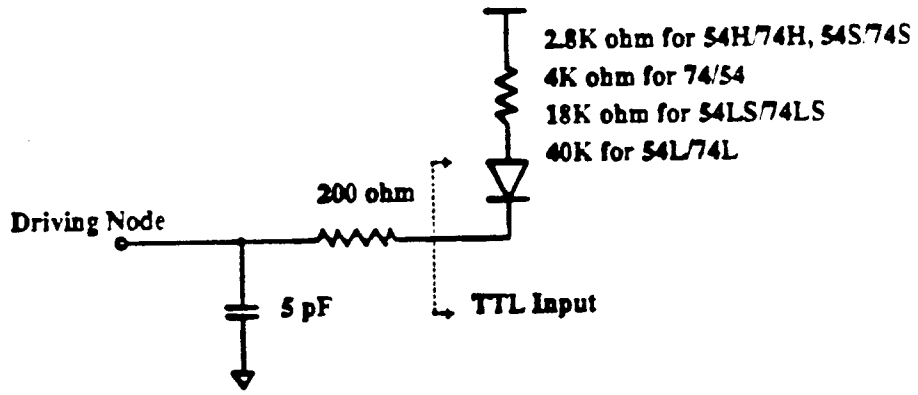

Figure 3.1.a: Schematic for typical TTL loads for an output buffer

Among different TTL loads as shown in Figure 3.1.a, the 54H/74H and 54S/74S present the smallest load resistance. According to Ohm's law:

$$V = I * R$$

V = buffer output voltage;

I = buffer sinking current;

R = TTL-load resistance;

the smallest resistive load requires the largest amount of current from an output buffer.

Therefore, the 54H/74H and 54S/74S load resistance is used in this design to represent the worst case TTL load. Any buffer which is capable of driving the worst case TTL load can be used to drive a load with higher load resistance.

3.1.1. Output Buffers

It is important for an output buffer to have sufficient driving capability to achieve specific rise and fall times for a given capacitive load. Given a load capacitance, target rise and fall time, and power and ground bounce requirements, the output transistors of an output buffer are sized using SPICE simulation. Generally two or more stages of buffering are needed to present a lower capacitive load to internal circuitry. Also, an even number of stages is used to result in a non-inverting output stage.

To meet performance specification, large transistors are used for output buffers; therefore, output currents are large and latch-up is likely to occur. Latch-up occurs when transients rise above Vdd or sink below ground by a sufficient amount (about 0.7 Volts). Refer to the sections on ESD Protection and Latch-up for further details. Guard rings are used to reduce the possibility of latch-up.

In order to drive TTL loads with CMOS gates, different switching thresholds were considered. In the low state, V_{IL} of a TTL gate is 0.4 Volts while V_{OL} of a CMOS gate is 0 Volt. In our design, the V_{OL} was targeted at 0.2 Volts. V_{IH} for a TTL gate is 2.4 Volts whereas the V_{OH} of a CMOS gate is 5 Volts. Therefore, there is plenty of voltage margin at the *HIGH* state. In this design, the output buffers were sized to drive an output *HIGH* of 3.4 Volts within 5-10ns.

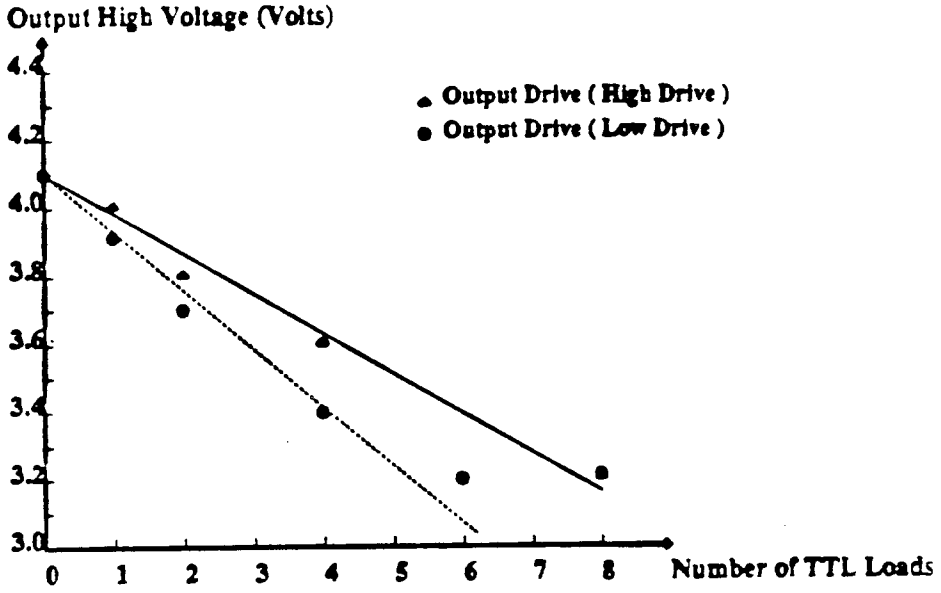

Figure 3.1.1.a: Output buffer output high voltage for multiple loads

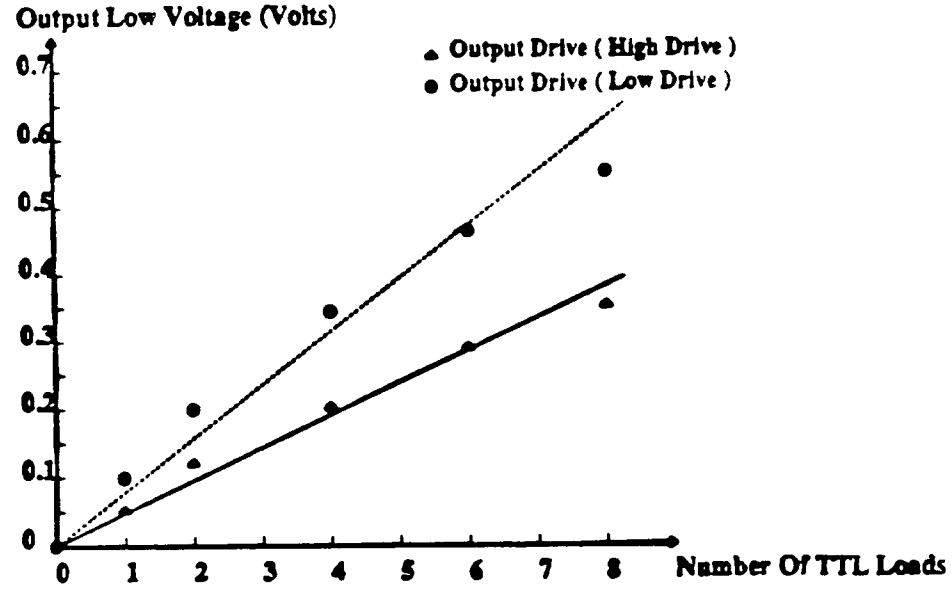

Figure 3.1.1.b: Output buffer output low voltage for multiple loads

The I/O buffers in this design can be used for an output *HIGH* voltage greater than 3.4 Volts and an output *LOW* voltage less than 0.4 Volts. The drawback in this case is the larger the voltage swing at the output, the smaller the number of TTL loads an output buffer can drive. For example, if one wants to achieve output voltages of 0.1 and 3.9 Volts, one must limit the number of TTL load to one only (compare to output voltages of 0.2 and 3.4 Volts with 4 TTL loads). Refer to Figure 3.1.1.a and Figure 3.1.1.b for relationship between output levels and the number of TTL loads.

A tri-state buffer has its output valid only when its output is enabled. A bi-directional buffer is formed by merging an input buffer and a tri-state output buffer. Because of the complex function of the bi-directional buffer, the buffer requires the largest layout area of the standard set of pads. Usually, the layout of the bi-directional buffer is completed first so as to set an upper limit of area used for all other I/O buffers.

3.1.2. Input Buffers

An input buffer is built by cascading an even number of inverter stages to pass an outside signal to internal circuitry. To interface TTL logic to CMOS logic, it is common practice to place the switching point of the input inverter in the middle of the TTL switching range. In this design, for TTL V_{OL} of 0.2 Volts and V_{OH} of 3.4 Volts, the switching point for input buffers was set to be 1.8 Volts. The inverter transistors were ratioed by performing SPICE simulations.

Current of a transistor is directly proportional to the mobility of the charge carriers and W/L ratio.

$$I \alpha u^{*} \frac{W}{L}$$

I = current;

u = mobility;

W/L = transistor size;

For n-well process, the mobility of a p-channel transistor is approximately half of that of

a n-channel transistor. In order to have equal driving capability of the p-channel and the n-channel transistor, the W/L of the p-transistor is doubled of that of the n-transistor. By symmetry, the switching point for such an input buffer is 2.5 Volts. However, if a lower switching point is desired, such as 1.8 Volts in this design, a stronger n-transistor is used as a strong pull-down device against the weak p-channel pull-up transistor. In this design, the W/L ratio of the n-transistor is 19/1.2 whereas the W/L ratio of the p-transistor is 30/1.2. By the same token, if a switching point higher than 2.5 Volts is desired, the W/L ratio of the p-transistor should be larger than two times that of the n-transistor.

An important cell in the I/O buffer library is the input clock driver. The clock driver must be able to drive a huge load compared to what a normal input buffer would drive. It is also desirable to have as little delay as possible because the speed of the clock driver has great impact on the performance of the chip. As a result, the switching current of the clock driver is very large.

$$I = C * \frac{\Delta V}{\Delta t}$$

I = current;

C = capacitance;

ΔV = voltage swing;

Δt = delay time;

Loading of the clock line is 5 pF in our design, speed of the clock driver is 2 ns and the voltage swing of a CMOS driver is 5 Volts. Using the above equation, there is 12.5 mA of switching current. Usually, one pair of power and ground supply pads is assigned to the clock driver.

3.1.3. Power and Ground Buffers

Power and ground buffers consist of metal pads connected to the appropriate rails. There are two sets of power and ground rings in this design. Multiple sets of power and ground rings are used to resolve some of the power and ground bounce issues (refer to the section on Power and Ground Issue for further details). Each power/ground buffer is connected to two power/ground rings of appropriate polarity. A large number of vias were used in the power/ground connection to ensure better conductivity.

3.1.4. Other Buffers

Often a VLSI design is pad limited, i.e. the size an an VLSI chip is determined by the packing density of the I/O pads along their sides. One would like to pack as many pins as possible in a fixed size I/O frame. One way to achieve this is by utilizing corner space of the I/O frame as well. One set of power and ground pads was built into the corner pad. By doing so, four sets of power and ground pads were acquired without consuming any I/O slot.

A space pad consists of two segments of the power rings and two segments of the ground rings only. There is no bonding pad in the layout. The space pad is used to expand the I/O frame when the VLSI design is not pad limited. See Figure 3.1.a for a sample layout of the I/O frame.

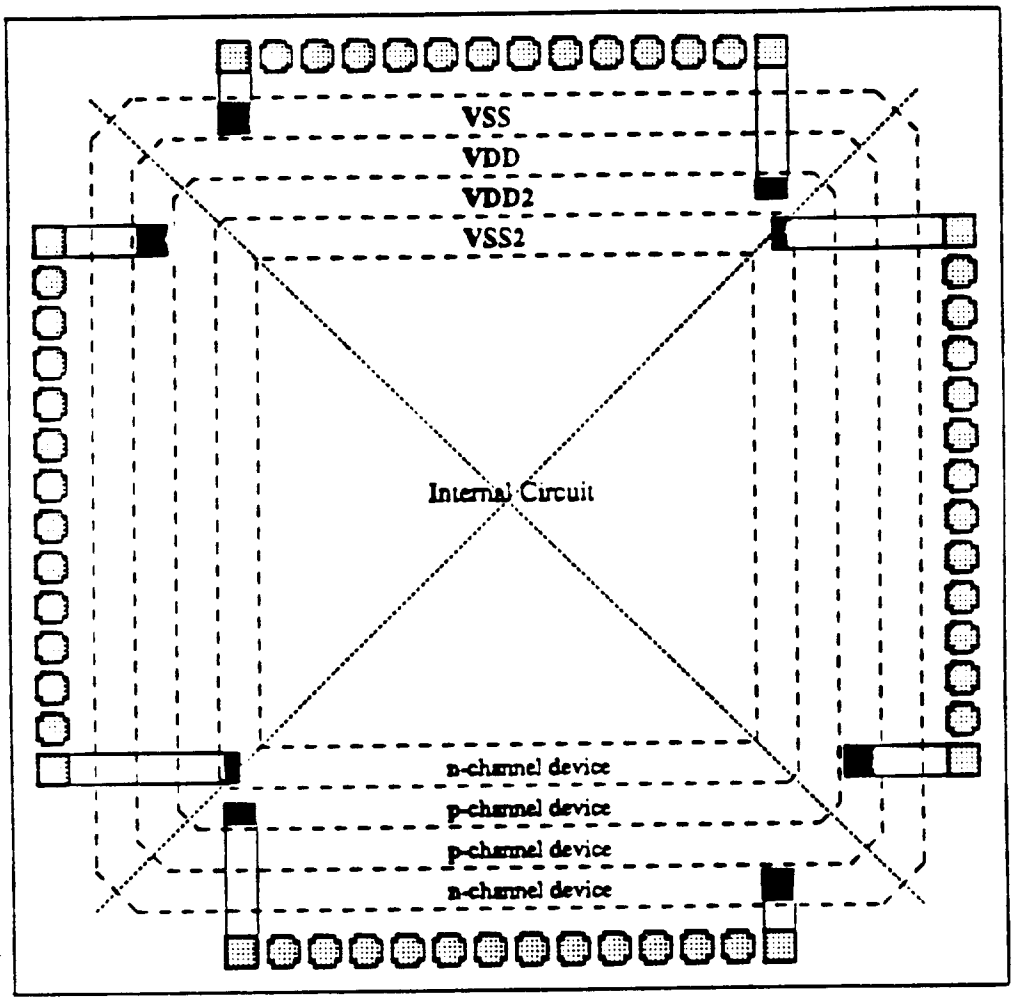

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Figure 3.1.a: Layout of the I/O frame

3.2. Electro-static Discharge Protection

In a VLSI chip, pad drivers and input buffers are the most important part of the design. Special care must be taken to protect the chip against ESD. ESD is a particular concern for input pads because an outside electric signal connected to an input pin may be well above 5 Volts, e.g. static charge from human fingers [12]. A resistor and two clamp diodes are used to reduce this voltage; hence, protect the circuit from ESD. See Figure 3.2.1.a for a typical input protection structure.

If the voltage at the input node A rises sufficiently above Vdd or below ground, the clamp diodes are then turned on to provide a current path to drain off the excess charge brought in by the high input voltage. The resistor is used to limit the peak current that flows in the clamp diodes in the event of an unusual voltage excursion; therefore, protecting the clamp diodes. However, this resistor contributes delay to an input circuit combines with the input capacitance to form an RC time constant. Value of the resistor can not be too big as it will lead to a large RC time constant and effect the timing in high speed circuit operation. Typical values of the resistors used range from 200 Ω to 3K Ω. In this design, a 500 Ω resistor is used. A polysilicon resistor is preferable to a diffusion resistor as the polysilicon, being the topmost layer of resistive material in a CMOS process, dissipates heat more efficiently.

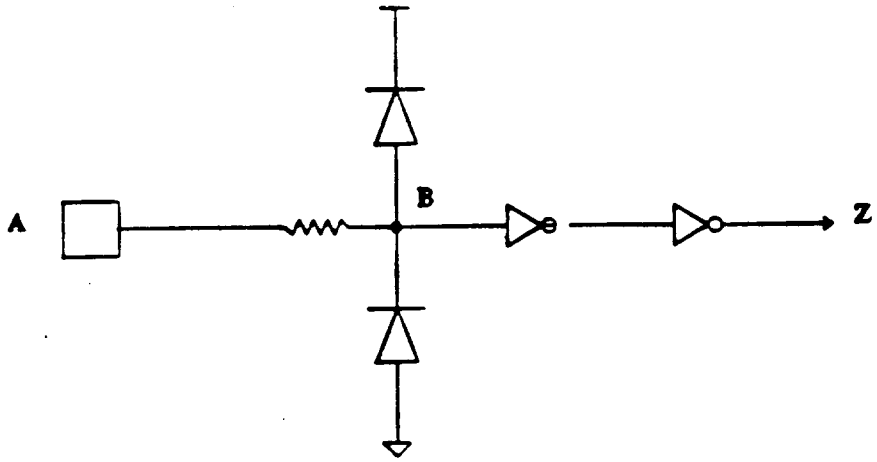


Figure 3.2.1.a: Input Protection Structure

There is an advantage by laying out the clamp diode connecting to Vdd as shown in Figure 3.2.1.b. The base of the pnp transistor is able to sink a current of I_b. At node B, the pnp transistor is able to sink a current of $\beta * I_b$, where β is the current gain of the transistor.

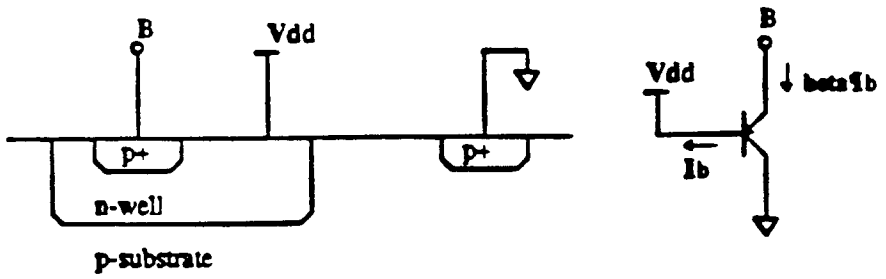


Figure 3.2.1.b: Actual circuit representation of the clamp diode connecting to Vdd

A similar transistor structure replaces the diode connected to ground using a npn transistor may be used, but was not in our design.

In addition to the structure shown in Figure 3.2.1.a, two diode connected transistors (one PMOS transistor connected to Vdd and one NMOS transistor connected to ground) may be added to the input protection circuit. The diode connected transistors can also be used as substitution for the clamp diodes. This technique is a very common practice in a NMOS process where both types of diodes are not readily available.

For an output buffer, the output drivers act as oversized protection diodes which protect the buffer against ESD damage. Therefore, the clamp diodes may not exist in the output buffer.

3.3. Latch-up

In CMOS design, there is an undesirable parasitic circuit effect called "latch-up." Latch-up results in shorting of power and ground supply lines; thus, causing chip self-destruction or system failure [2]. The most likely place for latch-up to occur is in I/O buffers where large current flows, large parasitics may be present and abnormal circuit voltages may be encountered. Figure 3.3.a and Figure 3.3.b show a cross section of a n-well process CMOS inverter and the latch-up circuit representation.

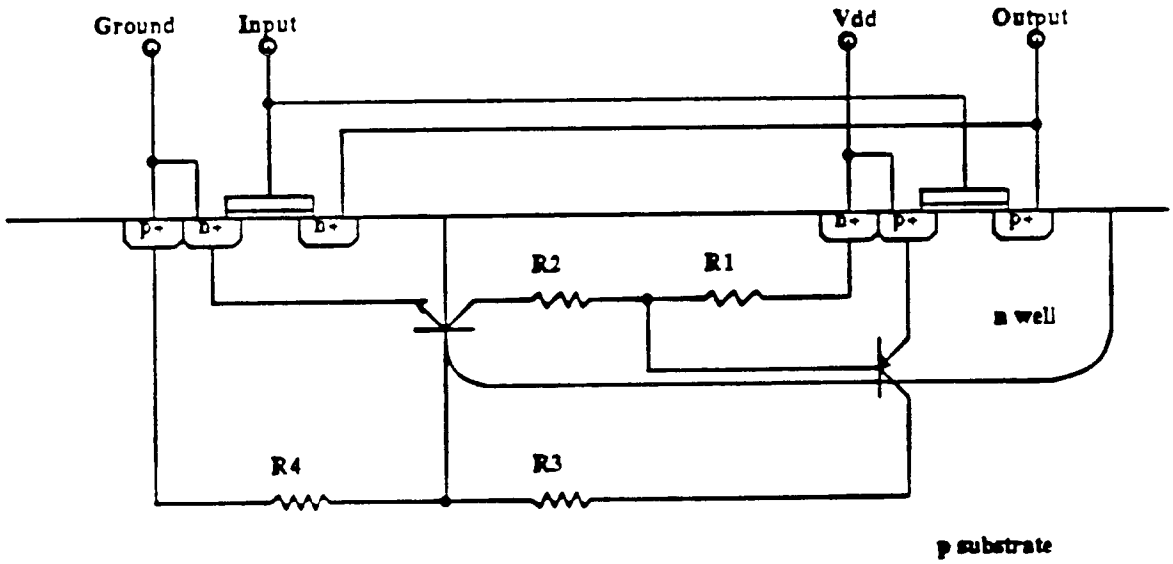


Figure 3.2.a: Cross Section of a n-well CMOS Inverter

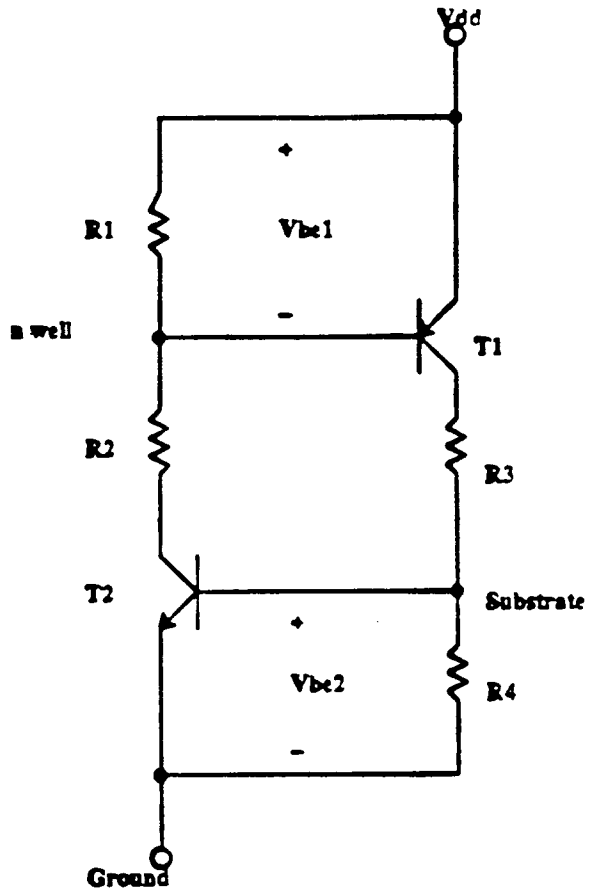


Figure 3.2.b: The latch-up circuit representation

A variety of mechanisms may cause latch-up, includes ESD, power or ground bounce and α-particles [11]. Under normal circuit operation, currents in the substrate and n-well are very small. The voltages across R1 and R4 will be less than those required to turn on the bipolar transistors T1 and T2. With both T1 and T2 are off, latch-up is not a concern. However, if V_{be1} is 0.7 Volts (the turn on voltage of a p-n junction) or higher, T2 will be turned on. A current starts to flow in R1 and R2; therefore, lowering the voltage of the n-well and causes T1 to be turned on. Both bipolar transistors begin to conduct and the current rises sharply from a leakage level (under 1 uA) to a value limited by resistors R2 and R3, often many milliamperes. Values of R1 and R2 depend heavily on the fabrication process, they are in the range of 0.005 to 40 Ω-cm [8]. A positive

feedback path is then created, circuits are often permanently damaged by the resulting high currents. This phenomenon is known as *latch-up*. It can occur at normal operating voltages if the voltages applied to input or output pins cause forward-biasing of *pn* junctions within the chip. The unwanted current can only be shut off by disconnecting the chip from the power supply.

Guard rings and layout design rules are used to reduce the possibility for latch-up to occur. Latch-up occurs when the p+ source and n-well is forward biased. Electrons are being injected into the substrate. With the presence of guard ring, these electrons are removed from the substrate and break the feedback loop for latch-up to occur. In the n-well, a strip of n+ diffusion is used to surround the PMOS circuit within the well. Similarly, a strip of p+ diffusion is used to surround the NMOS circuit in the p-substrate. Due to the layout area limitation, the guard ring is usually drawn close to the minimum width defined by the layout design rule.

In this design, a n-channel transistor, instead of a p-channel transistor, is used as pull-up device in the output driver. By eliminating the PMOS and the n-well, the latch-up circuit is broken.

In order to reduce the possibility of internal latch-up, the following layout rules are observed [1]:

1. Every well must have at least one substrate contact of the appropriate type. The substrate contact is best located near the power or ground supply line.
2. Every substrate contact is connected by metal directly to a supply pad.
3. Substrate contacts are placed as close as possible to the source connection of transistors connected to the supply rails, i.e., Vss to n-devices and Vdd to p-devices. This rule reduces the value of R1 and R4 in Figure 3.2.b. A very conservative rule would place one substrate contact for every supply connection.
4. At least one substrate contact are placed per 5-10 logic transistors.

5. N- and p-transistors were drawn with packing of n-devices towards Vss and packing of p-devices towards Vdd. Interwining n- and p-devices in checkerboard patterns is not recommended.
6. P+ guard rings are included around n-transistors connected to Vss.
7. N+ guard rings are included around p-transistors connected to Vdd.

3.4. Power and Ground Issues

In a typical VLSI design, inductance of the bonding wires is a very critical issue. Value of the inductance varies between different packaging techniques. The traditional end-pin package has an inductance of about 15 nH on the lead. The center-pin package has an inductance of about 4 nH [5]. In this design, a bonding wire inductance of 5 nH is taken into consideration. As technology advances, the speed of the VLSI chip improves. This implies that the chip needs to switch current more rapidly. The transient current introduces voltage drops across an inductor by the relationship:

$$V = L \cdot \frac{di}{dt} \tag{1}$$

V = voltage drop across the parasitic inductor;

L = inductance of the bonding wire;

i = switching current;

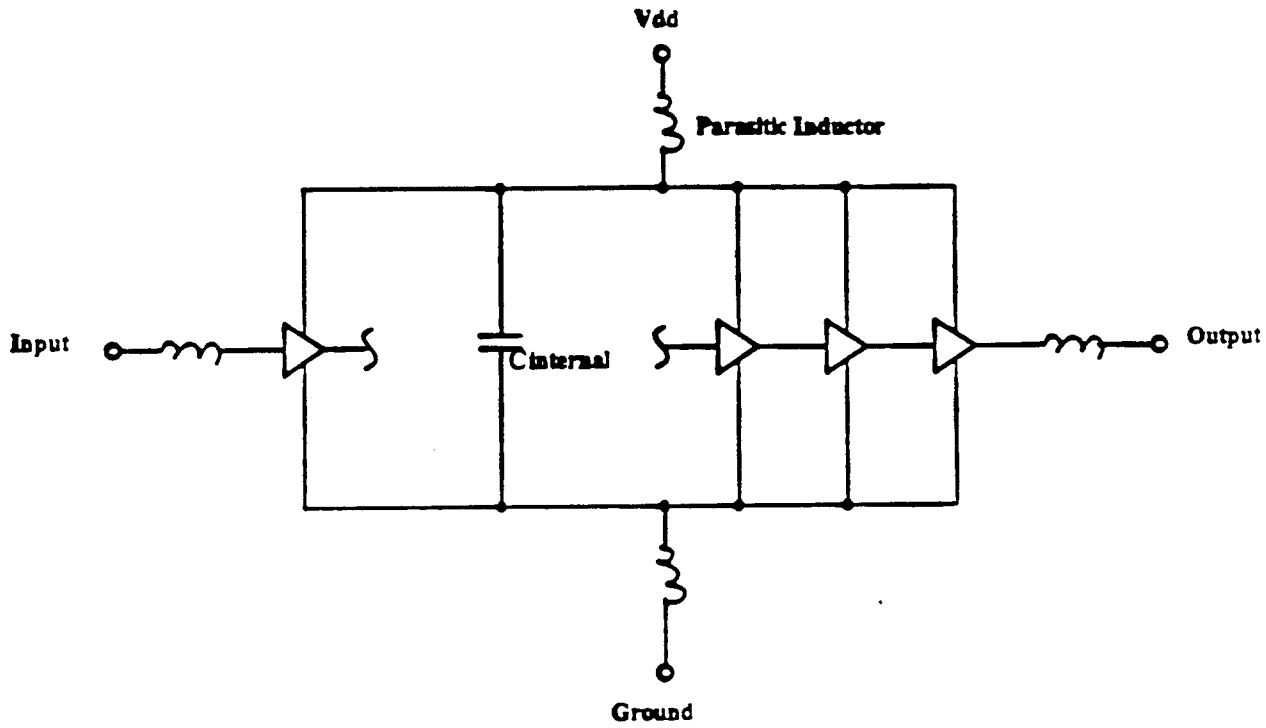


Figure 3.4.a: Parasitic Inductance on a VLSI Chip

All CMOS logic chips have an inherent noise problem. For high speed chips, the rise and fall times of the outputs are very fast and thus requires a large amount of current to switch between power or ground and an output node. This large changing current, $\frac{di}{dt}$, causes the chip's power and ground to *bounce* (also called *simultaneous switching noise).*

The following calculation shows how to determine the I/O buffer size taking the power and ground bounce into consideration. First, we will model the transistor by a resistor:

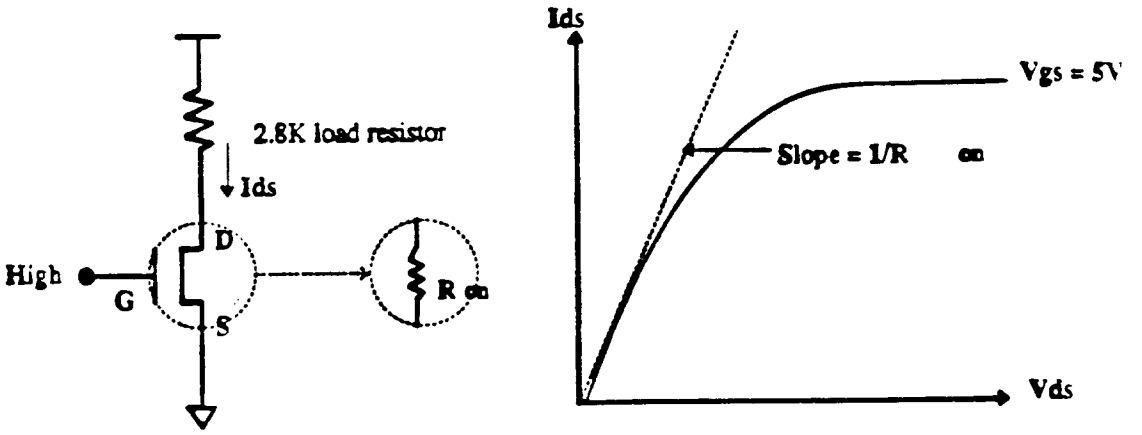


Figure 3.4.b: Transistor Model

For transistor operating as shown above, its electrical characteristic can be modeled by a resistor as follows:

$$I_{ds} = \frac{1}{2} * u * Cox * \frac{W}{L} * [2(Vgs - Vt)Vds - Vds^2]$$

Ids = Drain to Source Current;

u = mobility;

Cox = oxide capacitance;

W = width of transistor;

L = length of transistor;

Vgs = gate to source voltage;

Vds = drain to source voltage;

Vt = threshold voltage

Taking derivative of Ids with respect to Vds:

$$\frac{dI_{ds}}{dV_{ds}} = \frac{1}{2} * u * Cox * \frac{W}{L} * [2(Vgs - Vt) - 2Vds]$$

Evaluate above equation at Vds = 0 Volt gives R_{on}:

$$\frac{dI_{ds}}{dV_{ds}} = u * Cox * \frac{W}{L} * (Vgs - Vt)$$

$$\frac{1}{R_{on}} = u * Cox * \frac{W}{L} * (Vgs - Vt)$$

From process parameters given by MOSIS, u = 1000 sq.cm/V-s, Cox = 0.06 fF/sq.um, Vt = 0.7 Volts, we have R_{on} = 4000 Ω/(W/L).

To obtain an estimate W/L ratio for the I/O buffers, we target at a rise or fall time of 5ns.

$$5RC = t_{rise\ fall}$$

where R is the R_{on} of a transistor and C is the load capacitance. For 5ns rise or fall time, RC = 1ns. There are four standard loads for the high drive output buffer, which amounts to 20pF.

$$RC = R_{on} * C$$

$$RC = 4000\Omega * \frac{20pF}{W/L}$$

With $t_{rise\ fall}$ targeted at 5ns, W/L is 80.

The following calculation shows how to obtain a value for the power/ground bounce.

$$V = L * \frac{di}{dt}$$

$L * \frac{di}{dt}$ is approximated as follow:

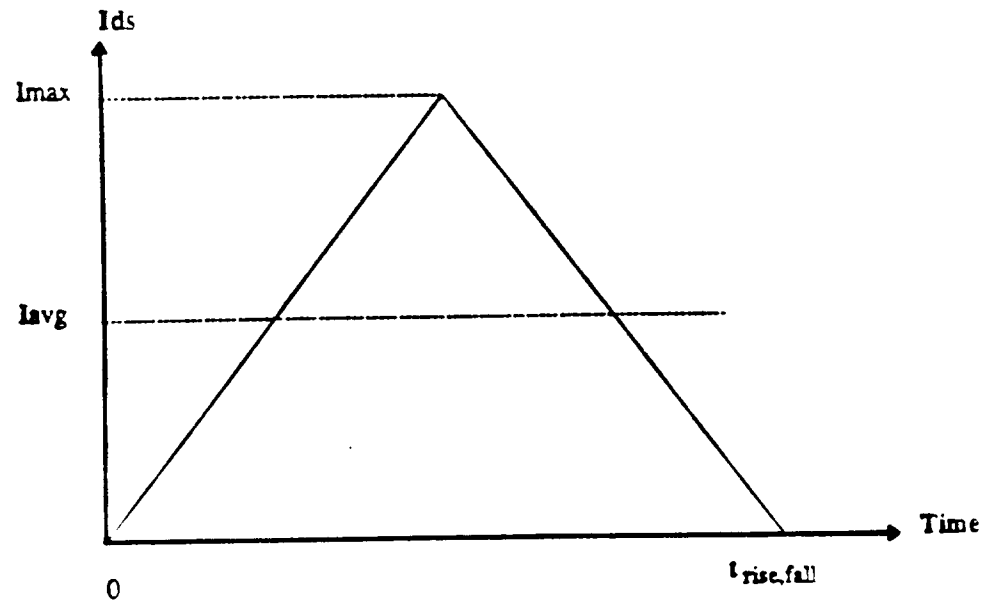


Figure 3.4.c: Transition Current Model

$$I_{avg} = C_{load} * \frac{\Delta V}{\Delta t}$$

Cload = 5pF * number of loads;

$\Delta v = 5$ V;

Δt = trise,fall;

From Figure 3.4.c, we have:

$$\frac{dI}{dt} = \frac{2 * I_{avg}}{t_{rise\ fall}/2}$$

$$\frac{dI}{dt} = \frac{4 * I_{avg}}{t_{rise\ fall}}$$

$$\frac{dI}{dt} = \frac{100pF - V * number\ of\ loads}{t^2_{rise\ fall}}$$

Therefore, power/ground bounce equals:

$$dV = L * \frac{dI}{dt} = 5nH * \frac{100pF - V * number - of - loads}{t_{rise,fall}^2} \quad (3)$$

The result is summarized in Table 3.3.a:

Table 3.3.a: A summary of W/L sizing and power/ground bounce

Driver Type	low drive	high drive
Number of Loads	2	4
trise,fall	5ns	5ns
W/L calculated	40	80
W/L from BSIM	50	100
power/ground bounce	0.04 Volts	0.08 Volts
#drivers/power pad calculated	10	5
#drivers/power pad from BSIM	12	4

The above calculation can be repeated for each fabrication process in order to obtain the W/L ratio and power/ground bounce for the I/O drivers. With changes in technology, one can use the appropriate mobility, oxide capacitance and threshold voltage of the transistor to obtain R_{on} and continue the calculation from there.

Power and ground bounce can cause a number of problems. One particular concern for the CMOS design is the excitation of latch-up. Refer to Figure 3.2.b for the schematic of a latch-up circuit. If the substrate that is connected to ground rises to a voltage high enough (around 0.7 Volts) to turn on the p-n junction of T2, base and emitter of T2 may become forward biased. T1 will then be turned on; thus, latch-up occurs. On the other hand, if the n-well that is connected to the power bounce such that the collector is 0.7 Volts above the base, the collector and base of T1 may become forward biased. T2 will then be turned on; therefore, exciting the latch-up mechanism.

To minimize power and ground bounce, the I/O buffers are designed to have large rise and fall times that are 5-10ns in this design. In other words, the buffers have sizes just big enough to drive the designated load. By doing so, the term $\frac{di}{dt}$ is small, and the voltage drop across the inductor of power and ground bonding wires is reduced. The trade-off for this approach is speed of the I/O buffers, which in turn affects the speed of the chip. The smaller the switching current is, the longer it takes the load to be charged or discharged.

The most obvious problem resulting from power and ground bounce occurs when the ground bounce causes an unswitched output to exceed the threshold of the loading device [5]. Thus, the loading device detects a logic transition which does exist. If the unswitched output is driving an edge-triggered input, the input may falsely clock the device. To make the problem even worse, because power and ground bounce are dynamic, it is almost impossible to track down this false input.

Ground bounce also causes input level shift. As the ground bounce below 0 Volts, an input may exceed the device's threshold. For example, if the ground bounce to -2 Volts and the input is at 0.5 Volts, the input is actually 2.5 Volts above ground. At this point, the input can register a high logic level. The input level shift can cause a latch to lose stored data. If a latch's clock input exceeds its threshold, the latch will store whatever is on its data input. As a result, the original data will be lost. Such an event is disastrous for RAMs, PLDs, etc.

In a traditional packaging technique, power and ground pins are placed at the end of the package. By moving the power and ground pins to the center of a package, as in a center-pin package, the inductance between a chip and the ground is reduced. Since power/ground bounce equal to L*dI/dt, any reduction in L would reduce the noise that the chip created.

Another common practice in a VLSI design is to put in multiple power and ground rings [7]. Refer to Figure 3.1.a for a possible layout scheme and Appendix C for the implementation for two sets of power/ground rings. Multiple power (Vdd) and ground (Vss) rings are designed to reduce Vdd and Vss path inductance and resistance. In order to ensure proper power and ground signals transmission, the power and ground rings were made very wide (20-30um) to resolve the issues of IR drops and metal migration [11], [12]. The largest current transient is observed at the I/O drivers, which leads to the largest power/ground bounce. Therefore, a wider power/ground ring is connected to the I/O driver. A narrower power/ground ring is used by the I/O logic to save layout area.

4. Simulation

The BSIM circuit simulator (based on Berkeley Short-channel IGFET Model), instead of the more popular SPICE program, was used for circuit simulation in this design. The BSIM simulator uses process parameters in the BSIM format. There are three reasons for using BSIM. First, the process parameters provided by MOSIS were extracted from wafers by using the BSIM parameter extraction program. Rather than translating the BSIM parameters into SPICE parameters, therefore adding inaccuracy to the parameters, the BSIM simulator was called upon. The BSIM parameters were stored in a process file which would then be accessed in every BSIM simulation run. Refer to Appendix A for the HP 1.2um process parameters.

The second reason to use BSIM is model accuracy. The process employed in this design is the HP 1.2um process, the smallest geometry in MOSIS process to date. As device dimension decreases, a true physical device model is difficult to derive because of the three dimensional nature of small geometry effects. Even if the physical model was feasible, the complicated equations involved would prohibit its use for circuit simulation purposes. Furthermore, a true device physics oriented modeling approach usually makes parameter extraction very difficult. In BSIM, empirical parameters were added to existing physical parameters to achieve a more accurate modeling [6] and to alleviate the job of parameter extraction. The semi-empirical model replaces sophisticated equations by empirical equations to represent small-geometry effects and process variation. The semi-empirical model is simplier and more efficient in circuit simulation.

The third reason to use BSIM is its performance. Experimental results show that the BSIM model reduces simulation time as compared to the popular SPICE level 2 MOSFET model. A comparison of selected SPICE2 simulation execution time from [6] is listed in Table 4.a.

Table 4.a: A comparison of selected SPICE2 simulation execution time

Circuit Description	BSIM (sec)	SPICE(sec)
Ratioless Dynamic Logic	24.50	29.75
Five Stages Inverter Chain	18.30	44.25
MOS Amplifier (DC and AC)	40.02	52.70
MOS Amplifier (transient)	75.08	137.50
One Stage Op-Amp	15.83	70.77
Binary-to-Octal Decoder	262.37	586.28
Telecommunication Circuit	1784.83	2717.32

5. Results

In this design, the I/O buffers were implemented according to the following specification. The output buffers must be able to drive a V_{OL} of 0.2 Volts and a V_{OH} of 3.4 Volts with less than 0.4 Volts of power or ground bounce. There are two standard loads on a low-drive output buffer and four standard loads on a high-drive output buffer. See Figure 5.a for the schematic for one standard load.

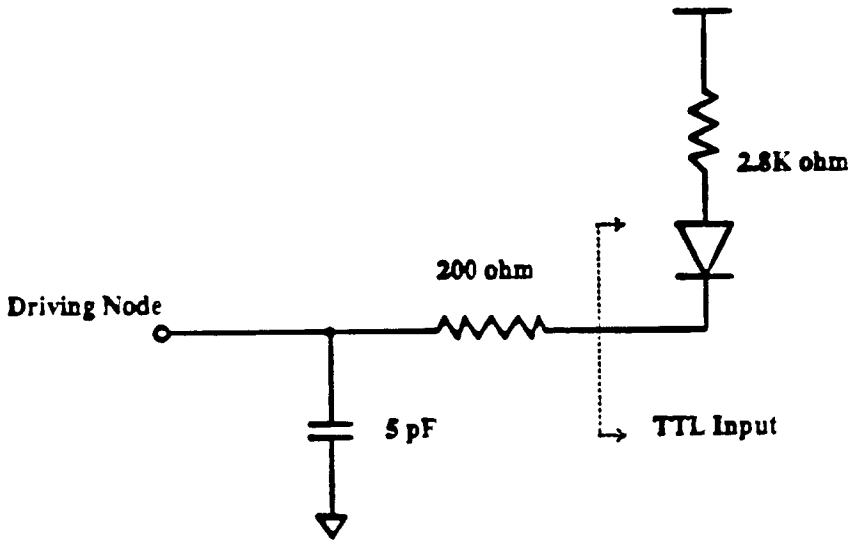


Figure 5.a: Schematic for a standard load for an output buffer

The input driver was designed to drive a 2pF capacitive load. On the other hand, the input clock driver was designed to drive the clock line, a huge load which amounts to a 5pF capacitor. Table 5.a gives a summary of the performance of the I/O buffers based on simulations of the layouts.

Table 5.a: Summary of the performance of I/O buffers

Cell Name	Description	Loading	Delay(BSIM)	Delay(calculated)
BOL	Direct Output Buffer	2 std loads	3.5ns	5ns
BO	Direct Output Buffer	4 std loads	5.0ns	5ns
BTL	Tri-state Output Buffer	2 std loads	5.4ns	5ns
BT	Tri-state Output Buffer	4 std loads	7.4ns	5ns
BIL	Bidirectional Output	2 std loads	5.5ns	5ns
BI	Bidirectional Output	4 std loads	7.4ns	5ns
BIN	Input Buffer	2 pF	2.0ns	2ns
BINP	Clock Driver	5 pF	2.5ns	2ns

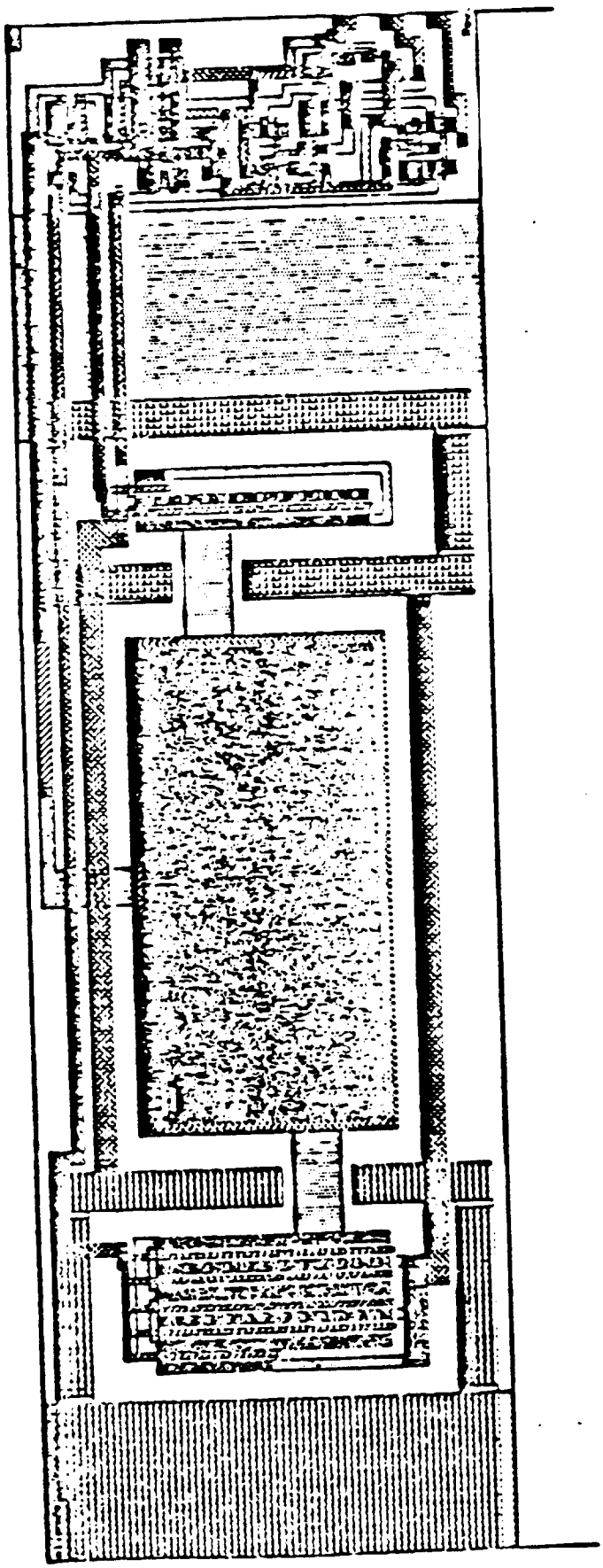
The delay from BSIM was taken at the 50% switching point and it was the average of the rise time and the fall time of the buffer.

6. Discussion

In VLSI design, CMOS is the dominant process. As speed of the VLSI design becomes faster, larger current is required for the I/O buffers to switch logic levels more quickly. In order to obtain more accurate results one must not only rely on hand calculated values as shown in section 3, but also must perform circuit simulations.

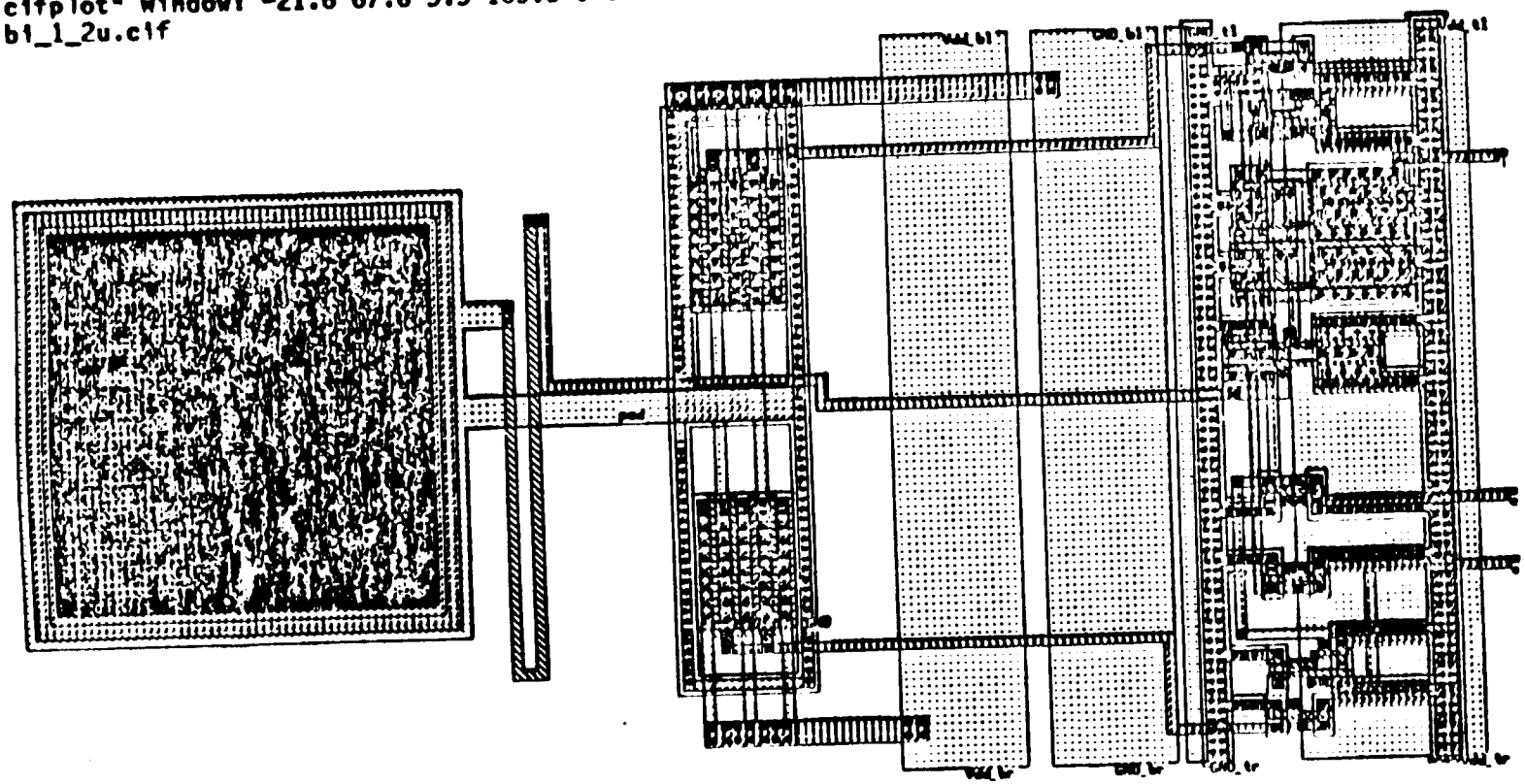
BiCMOS has been used by other designers to help cope with the problems created by large current requirements. Because of the greater current driving capability, bipolar transistors are frequently used for driving larger off-chip capacitances. Also, they have proven to have a speed advantage over a conventional CMOS buffer with the same area [3], [4]. We were interested in using only standard CMOS available through MOSIS. In the future, it may be important to redesign these pads using BiCMOS, when it becomes more available.

There is more than one way of laying out an I/O buffer. The following page contains a bi-directional output pad from the Berkeley SPUR pad cell library for comparison with our bi-directional output buffer for design and layout style.



Job: stdin
Date: Wed Mar 8 17:22:31 1989

cifplot* Window: -21.6 67.8 9.9 189.3 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
bi_1_2u.cif



ASP Pad Layout

The most obvious difference between the SPUR pad design and the ASP pad design is the number of power and ground rings. To save layout area, there is only one pair of power and ground busses in the SPUR pad design. To isolate power and ground bounce, two separate power and ground busses have been designed into the ASP pads. One pair of power and ground busses is used for the pad logic while the other pair is used for internal circuitry.

In the SPUR design, a p-transistor is used as a pull-up device for the output driver. By doing so, the driver has a larger logic swing compared to the n-channel pull-up design in the ASP pads. In our design, the n-channel pull up device is able to drive a V_{OH} of 3.4 Volts. Substituting a large p-channel output transistor with a large n-channel device has an advantage of reducing the possibility for latch-up to occur.

Random logic of the I/O buffers in the ASP design is nicely packed in the form of standard cell, i.e. each logic cell has the same height. This not only enables a user to trace the logic very easily, but also makes debugging the pads an easier task.

7. Conclusion

This report describes my design and implementation of I/O buffers for ASP. I studied the SPUR pad library and appropriate changes were made to develop pads for ASP. Preliminary transistor sizes were calculated according to equations given in section 3.3. These sizes were refined by doing BSIM circuit simulations. Layout was done in Magic (refer to Appendix C for the I/O buffer cell layout). Appendix A contains a BSIM process parameter file given by MOSIS and used in the circuit simulations for the pad design. A summary of the I/O buffer characteristics is listed in Appendix B.

I/O buffer design is one of the most important aspects of a VLSI design. Careful circuit simulation and special layout techniques were used in this design. The following areas deserve special attention in I/O buffer design: ESD protection, latch-up protection, and power and ground issues. Also, there are many trade-offs a circuit designer has to make. For example, the number of power and ground rings, using a n-channel (instead of a p-channel) for pull-up device, etc. These issues were discussed in previous sections. Therefore, it is very important for the designer to have a strong circuit background and be able to make trade-offs in flavor of a particular VLSI design.

8. References

[1] Weste and Eshraghian, CMOS VLSI Design, 1st ed. Addison-Wesley, Oct 1985.

[2] Hodges and Jackson, Analysis and Design of Digital Integrated Circuits, 1st ed. McGraw-Hill, Inc., 1983.

[3] Masaharu Kubo et al., "Prospective on BiCMOS VLSI's," IEEE Journal Solid-state Circuits, Feb 88, pp.5-11.

[4] Rosseel et al., "Influence of Device Parameters on the Switching Speed of BiCMOS Buffers," IEEE Journal Solid-state Circuits, Feb 89, pp.90-99.

[5] David Shear, "EDN's advanced CMOS logic ground-bounce tests," EDN, March 2, 1989, pp. 88-112.

[6] M. C. Jeng et al., "Theory, Algorithm, And User's Guide For BSIM And Scalp," University of California, Berkeley, 28 May 1987.

[7] LSI Logic Data Book 1.5-Micron Compacted Array Technology, 1st ed. Milpitas: LSI Logic Corporation, July 1987.

[8] S. M. Sze, VLSI Technology 1st ed. McGraw-Hill, Inc., 1983.

[9] W. Scott et al., "Changes to Magic in Version 4," University of California, Berkeley, 30 November 1985.

[10] W. Bush et al., "A Prototype Silicon Compiler in Prolog," University of California, Berkeley, Report No. UCB/CSD 88/476, December 1988.

[11] C. Mead et al., Introduction To VLSI Systems 1st ed. Addison-Wesley, Inc., 1980.

[12] L. Glasser et al., The Design and Analysis of VLSI Circuits 1st ed. Addison-Wesley, Inc., 1985.

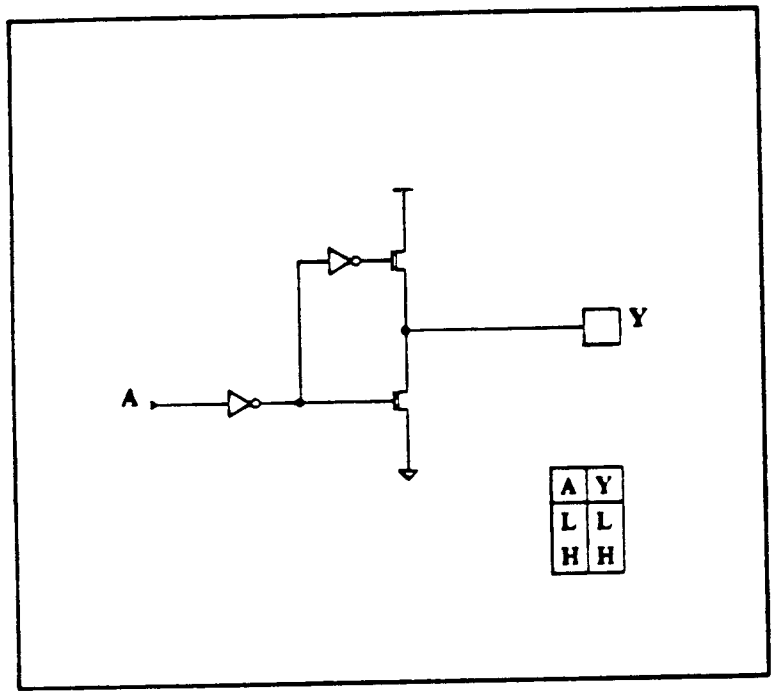
APPENDIX A: HP 1.2um Process Parameters

```
NM1 PM1 DU1 DU2 ML1 ML2 PY1
*
*PROCESS=HP
*RUN=M84O
*WAFER=3
*Gate-oxide thickness= 209.0 angstroms
*Geometries (W-drawn/L-drawn, units are um/um) of transistors measured were:
* 1.8/1.2, 3.6/1.2, 10.8/1.2, 3.6/3.6, 3.6/10.8
*Bias range to perform the extraction (Vdd)=5 volts
*DATE=8-16-88
*
*NMOS PARAMETERS
*
-9.3224E-001,-6.6008E-002,2.75809E-002
8.06697E-001,0.00000E+000,0.00000E+000
1.03393E+000,3.93570E-002,-5.9727E-002
1.34895E-001,5.81587E-002,-8.1833E-002
-1.1204E-002,1.46856E-002,1.98907E-002
5.40978E+002,4.97351E-001,3.70931E-001
5.51003E-002,1.18030E-001,2.76067E-003
9.07433E-002,1.11534E-001,-9.8848E-002
2.34076E+000,-3.5191E+000,3.34191E+001
-1.3553E-003,-5.6379E-003,1.20539E-003
2.40859E-003,-1.4277E-003,-7.0492E-003
-2.7901E-003,-1.6434E-003,1.92960E-002
-9.7102E-003,9.55623E-003,8.68224E-003
6.52812E+002,9.83057E+001,-1.8275E+002
-9.6332E+000,1.21415E+001,4.83453E+001
1.32105E+001,1.60438E+001,-3.1120E+001
1.84390E-002,5.10249E-003,-2.3331E-002
2.09000E-002,2.70000E+001,5.00000E+000
4.10850E-010,4.10850E-010,6.12835E-010
1.00000E+000,0.00000E+000,0.00000E+000
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
* Gate Oxide Thickness is 209 Angstroms
*
*
*PMOS PARAMETERS
*
-1.4869E-001,-2.1441E-002,3.54787E-003
7.22944E-001,0.00000E+000,0.00000E+000
4.08978E-001,4.69138E-003,6.81592E-002
-2.9728E-002,3.71040E-002,-4.4978E-003
-8.3243E-003,2.07175E-002,6.03684E-003
1.83660E+002,2.05851E-001,6.91218E-001
1.53564E-001,5.58641E-002,-7.1815E-002
-6.9671E-003,1.30250E-001,-2.5383E-003
```

```
8.93617E+000,-3.4801E-001,2.26803E+000
-3.6836E-004,-5.1259E-004,-2.7662E-003
1.11807E-003,-1.4041E-004,-3.6621E-003
8.50662E-003,2.05772E-003,-1.1552E-004
-2.2970E-003,1.84288E-003,1.06009E-002
1.93175E+002,6.94033E+001,-2.7880E+001
6.63966E+000,4.31665E+000,7.29263E+000
2.58409E-001,2.33255E+000,-6.0300E-001
-8.0194E-003,-5.1670E-003,3.14919E-003
2.09000E-002,2.70000E+001,5.00000E+000
1.70049E-010,1.70049E-010,1.14200E-009
1.00000E+000,0.00000E+000,0.00000E+000
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
*N+ diffusion::
*
82.4,  3.107000e-04,  4.296000e-10,  1.000000e-08,  0.72
0.66,  0.8628,  0.133,  0,  0
*
*P+ diffusion::
*
126.6,  4.920000e-04,  1.302000e-10,  1.000000e-08,  0.74
0.86,  0.4716,  0.111,  0,  0
*
*METAL LAYER -- 1
*
6.100000e-02,  2.600000e-05,  0,  0,  0
0,  0,  0,  0,  0
*
*METAL LAYER -- 2
*
3.800000e-02,  1.300000e-05,  0,  0,  0
0,  0,  0,  0,  0
*
*POLY LAYER -- 1
*
24.8,  5.900000e-05,  0,  0,  0
0,  0,  0,  0,  0
```

APPENDIX B: I/O Buffer Cell Library

UNIDIRECT OUTPUT BUFFER



DESCRIPTION

BOL and **BO** are non-inverting output pad drivers which are compatible with TTL signal levels. For every 12 instances of **BOL**, one pair of power and ground pads is required. For every eight instances of **BO**, one pair of power and ground pads is required.

BOL (STANDARD DRIVE)

Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	5	10	20	40	60	80	100
tPLH	4.0	4.3	4.6	4.9	5.4	5.6	5.7	5.8
tPHL	2.1	2.4	2.5	2.8	3.1	3.5	3.7	3.9

Standard Load	0	1	2	4	6	8	10	12
tPLH	4.0	4.3	4.5	4.9	5.5	5.8	5.9	6.2
tPHL	2.1	2.4	2.5	2.7	3.1	3.6	4.0	4.2
VOL	0.0	0.1	0.20	0.34	0.46	0.55	0.63	0.70

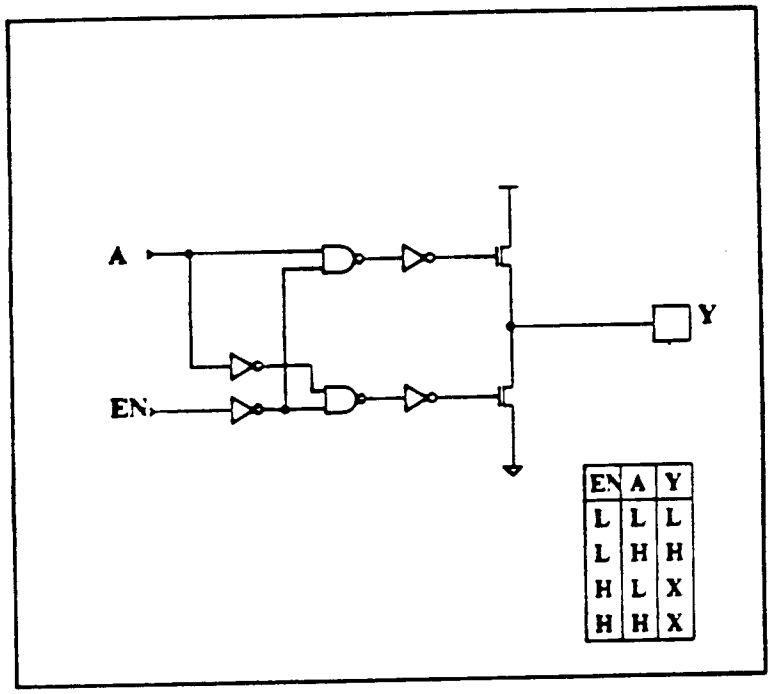
BO (HIGH DRIVE)

Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	5	10	20	40	60	80	100
tPLH	5.8	6.0	6.4	6.7	7.1	7.8	8.3	8.9
tPHL	2.7	3.0	3.1	3.3	3.8	4.2	4.6	5.0

Standard Load	0	1	2	4	6	8	10	12
tPLH	5.8	6.0	6.5	6.8	7.2	7.5	7.9	8.0
tPHL	2.7	3.0	3.1	3.2	3.4	3.6	3.9	4.2
VOL	0.0	0.1	0.12	0.20	0.29	0.35	0.40	0.44

TRI-STATE OUTPUT BUFFER



EN	A	Y
L	L	L
L	H	H
H	L	X
H	H	X

DESCRIPTION

BTL and BT are non-inverting tri-state output pad drivers which are compatible with TTL signal levels. For every 12 instances of BTL, one pair of power and ground pads is required. For every eight instances of BT, one pair of power and ground pads is required.

BTL (STANDARD DRIVE)

Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	5	10	20	40	60	80	100
tPLH	4.3	4.5	4.7	4.9	5.1	5.2	5.3	5.4
tPHL	4.6	5.7	6.0	6.2	6.4	6.8	7.1	7.5

Standard Load	0	1	2	4	6	8	10	12
tPLH	4.3	4.5	4.5	4.7	5.0	5.1	5.3	5.5
tPHL	4.6	5.7	6.2	6.6	6.8	7.0	7.2	7.3
VOL	0.0	0.10	0.19	0.34	0.46	0.55	0.63	0.70

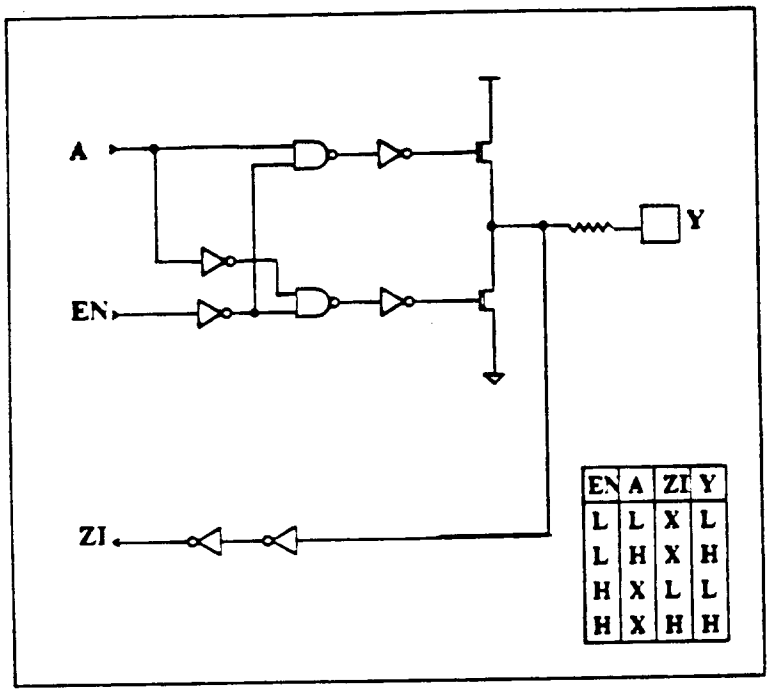
BT (HIGH DRIVE)

Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	5	10	20	40	60	80	100
tPLH	6.4	6.5	6.7	6.8	6.9	7.0	7.2	7.3
tPHL	5.9	6.9	7.3	7.5	7.6	7.7	7.8	7.9

Standard Load	0	1	2	4	6	8	10	12
tPLH	6.4	6.5	6.5	6.7	7.0	7.1	7.3	7.4
tPHL	5.9	6.9	7.5	8.0	8.2	8.4	8.5	8.6
VOL	0.0	0.10	0.12	0.20	0.29	0.35	0.40	0.44

BIDIRECT OUTPUT BUFFER



EN	A	ZI	Y
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

DESCRIPTION

BIL and BI are tri-state output pad drivers *(EN* is high) or input buffers *(EN* is low). The output driver is compatible with TTL signal levels. For every 12 instances of BIL, one pair of power and ground pads is required. For every eight instances of BI, one pair of power and ground pads is required.

BIL (STANDARD DRIVE)

Output Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	5	10	20	40	60	80	100
tPLH	4.4	4.6	4.6	5.0	5.2	5.3	5.4	5.5
tPHL	4.8	5.8	6.1	6.2	6.6	6.8	7.1	7.3

Standard Load	0	1	2	4	6	8	10	12
tPLH	4.4	4.6	4.6	4.7	4.9	5.2	5.4	5.6
tPHL	4.8	5.8	6.3	6.7	7.0	7.1	7.2	7.3
VOL	0.0	0.10	0.19	0.34	0.46	0.53	0.63	0.70

Input Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	2	4	6	8	10	15	20
tPLH	1.6	2.2	2.7	3.3	3.9	4.5	5.9	7.4
tPHL	1.3	1.8	2.3	2.8	3.3	3.9	5.1	6.1

BI (HIGH DRIVE)

Output Delays are Nominal [25° C, 5V Performance (ns)]

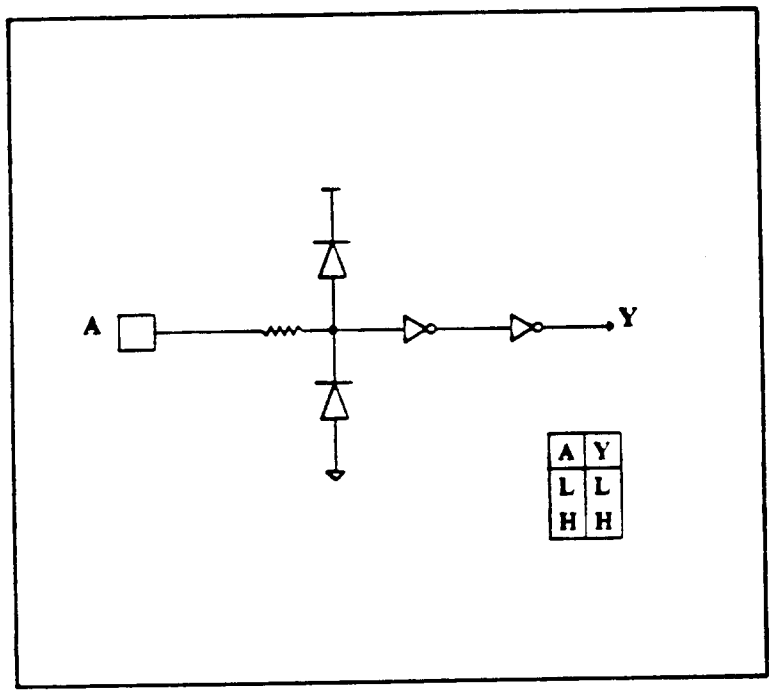
LOAD(pF)	0	5	10	20	40	60	80	100
tPLH	6.5	6.6	6.7	6.8	6.9	7.0	7.1	7.1
tPHL	6.0	7.1	7.4	7.5	7.6	7.7	7.8	7.9

Standard Load	0	1	2	4	6	8	10	12
tPLH	6.5	6.6	6.7	6.7	6.9	7.1	7.3	7.5
tPHL	6.0	7.1	7.5	8.0	8.2	8.3	8.3	8.5
VOL	0.0	0.06	0.12	0.20	0.28	0.34	0.39	0.43

Input Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	2	4	6	8	10	15	20
tPLH	1.6	2.2	2.7	3.3	3.9	4.5	5.9	7.4
tPHL	1.3	1.8	2.3	2.8	3.3	3.9	5.1	6.1

INPUT BUFFER



DESCRIPTION

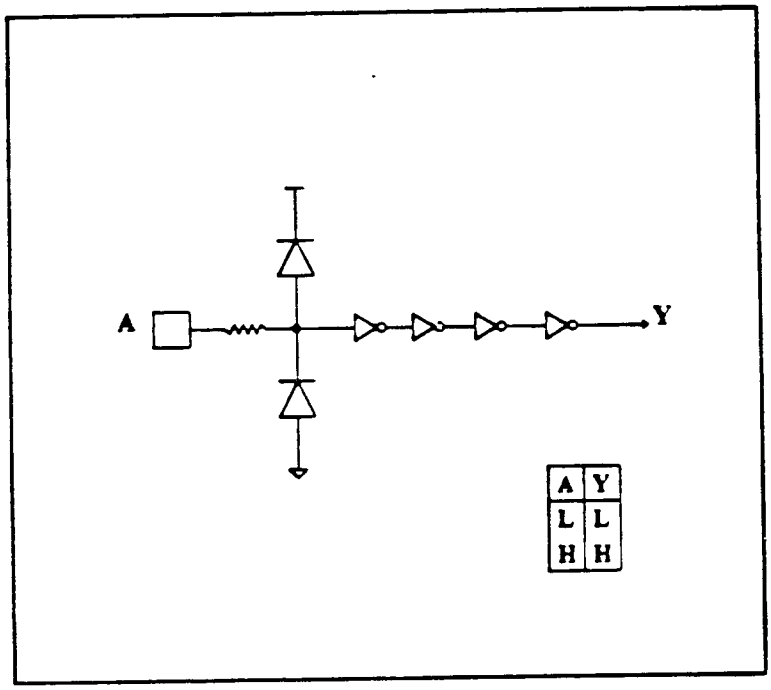
BIN is a non-inverting input buffer which is compatible with TTL signal levels. For every 12 instances of BIN, one pair of power and ground pads is required.

BIN

Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	2	4	6	8	10	15	20
tPLH	1.6	2.2	2.7	3.3	3.9	4.5	5.9	7.4
tPHL	1.3	1.8	2.3	2.8	3.3	3.9	5.1	6.1

INPUT CLOCK DRIVER



DESCRIPTION

BINP is a non-inverting input clock driver which is compatible with TTL signal levels. For every one instance of BINP, one pair of power and ground pads is required.

BINP

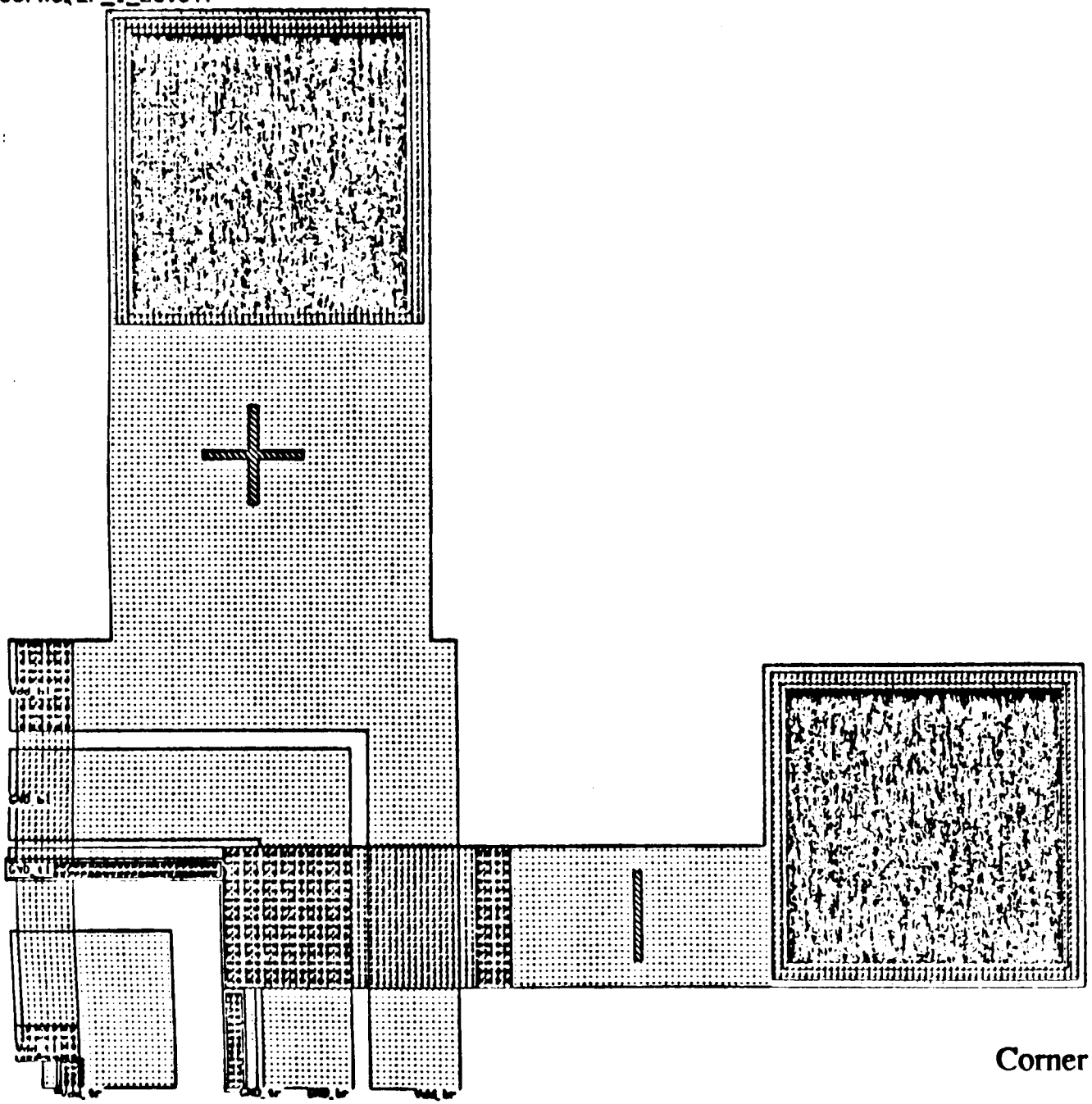
Delays are Nominal [25° C, 5V Performance (ns)]

LOAD(pF)	0	5	10	15	20	25	30	35	40
tPLH	1.7	2.3	2.9	3.4	4.0	4.7	5.3	5.9	6.5
tPHL	1.8	2.6	2.6	3.0	3.4	3.7	4.0	4.3	4.5

APPENDIX C: I/O Buffer Cell Layout

Job: stdin
Date: Wed Mar 8 18:23..: 1989

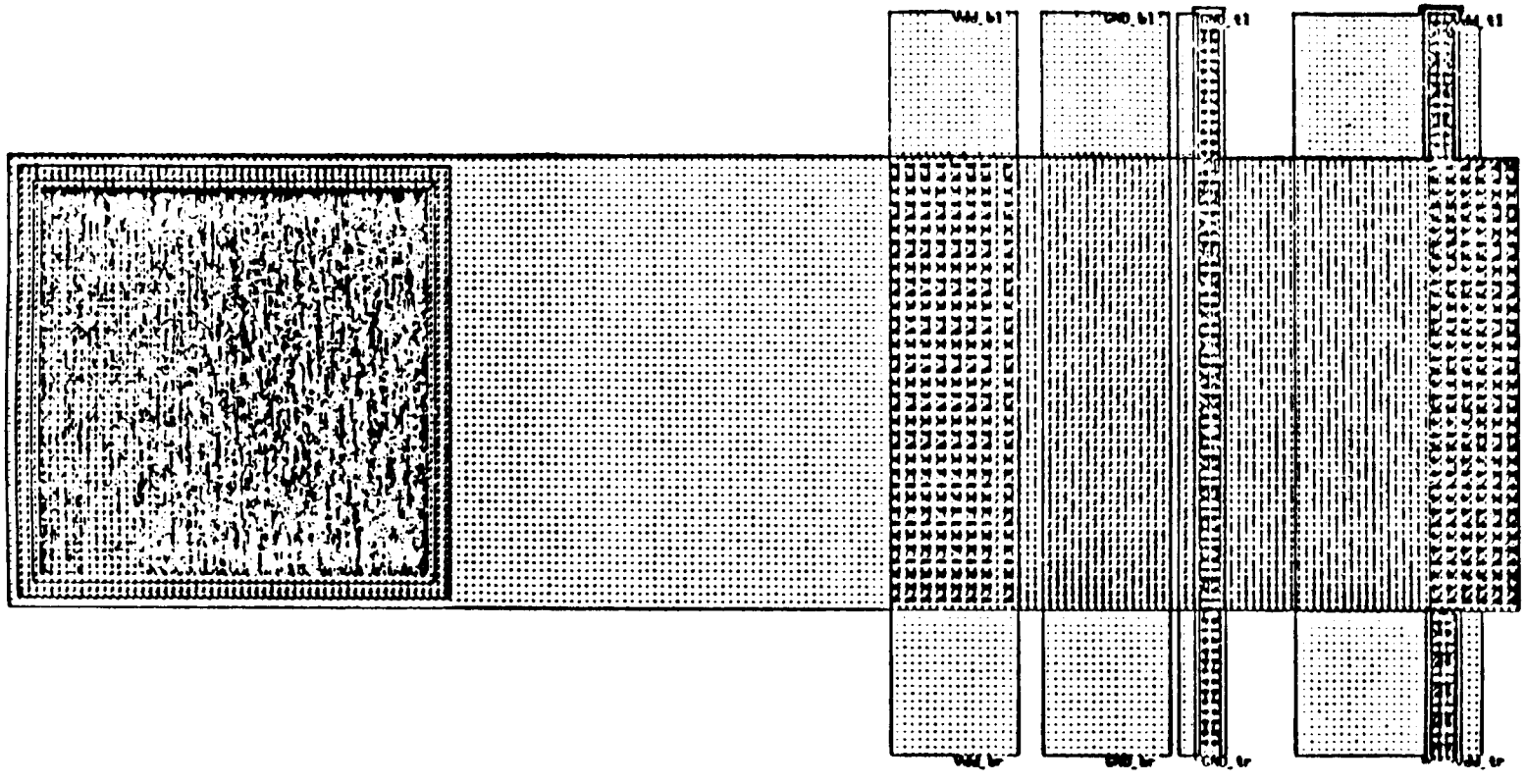
cifplot* Window: 49.8 230.1 -21 159 0 u=200 --- Scale: 1 micron is 0.019 inches (483x)
corner2P_1_2u.cif



Corner Pad

Job: stdin
Date: Wed Mar 8 17:58:03 1989

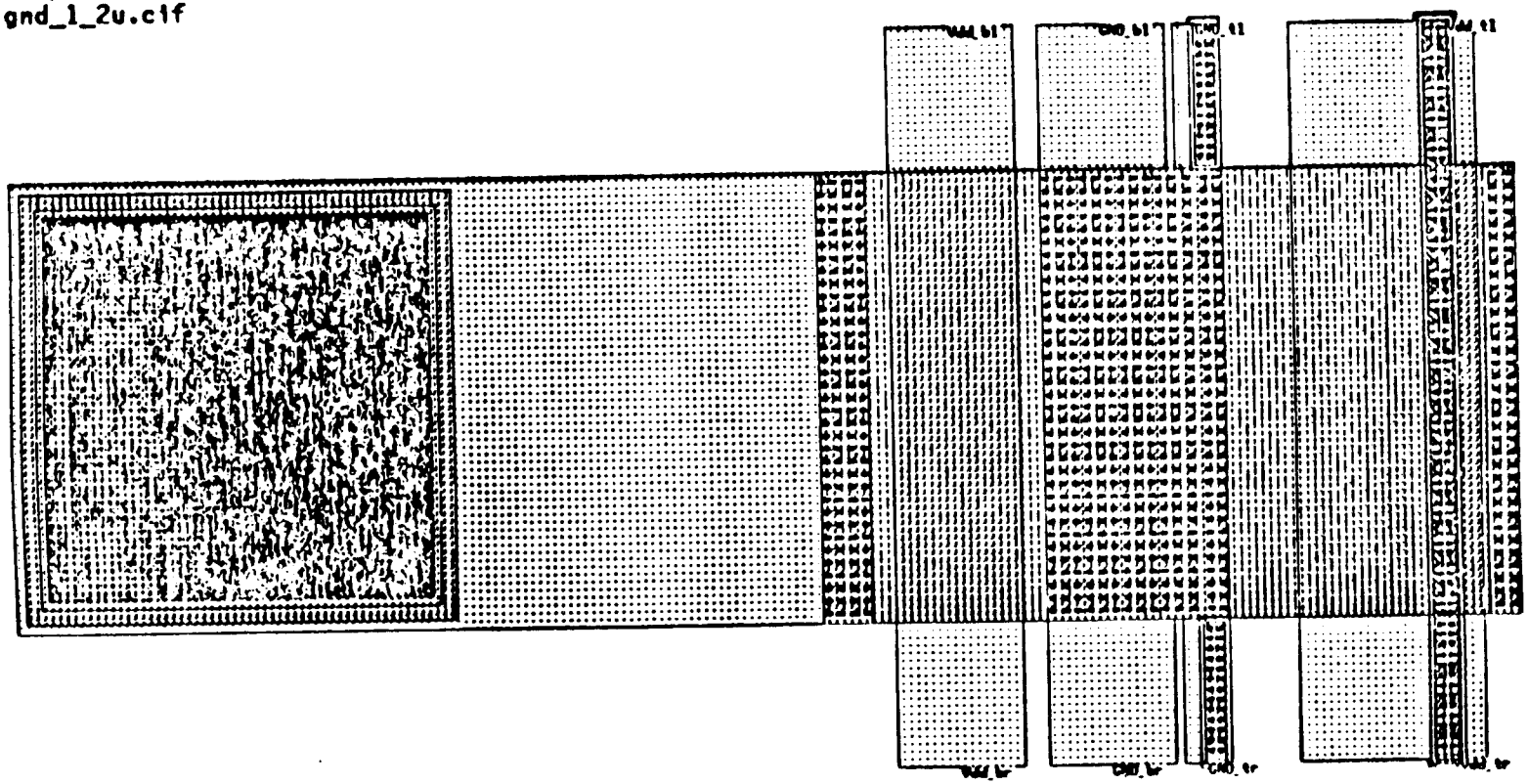
cifplot* Window: -27.6 61.8 15.6 196 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
vdd_1_2u.cif



Vdd Pad

Job: stdin
Date: Wed Mar 8 17:56:24 1989

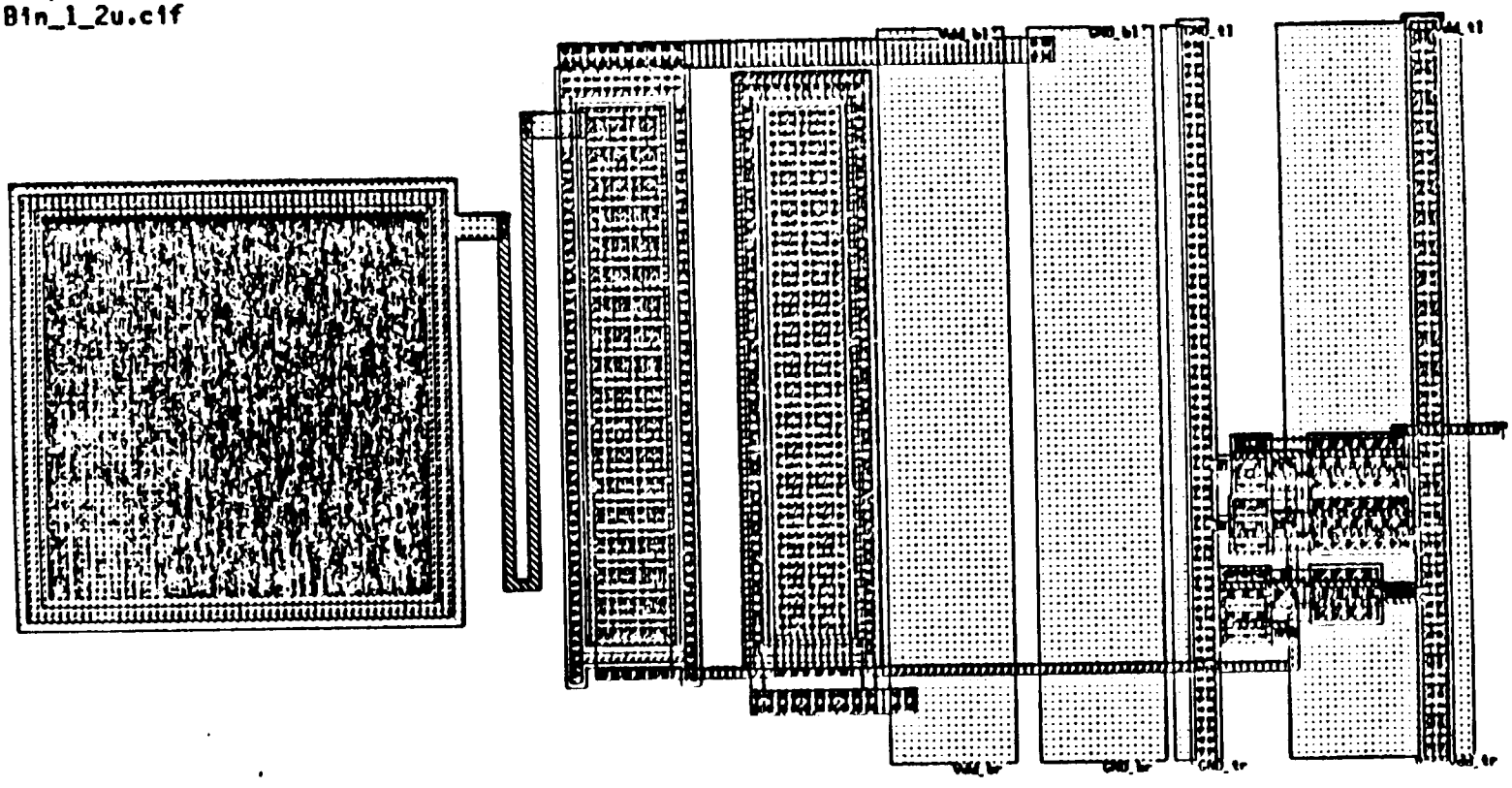
cifplot* Window: -27.6 61.8 15.6 196 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
gnd_1_2u.cif



Ground Pad

Job: stdin
Date: Wed Mar 8 17:14:23 1989

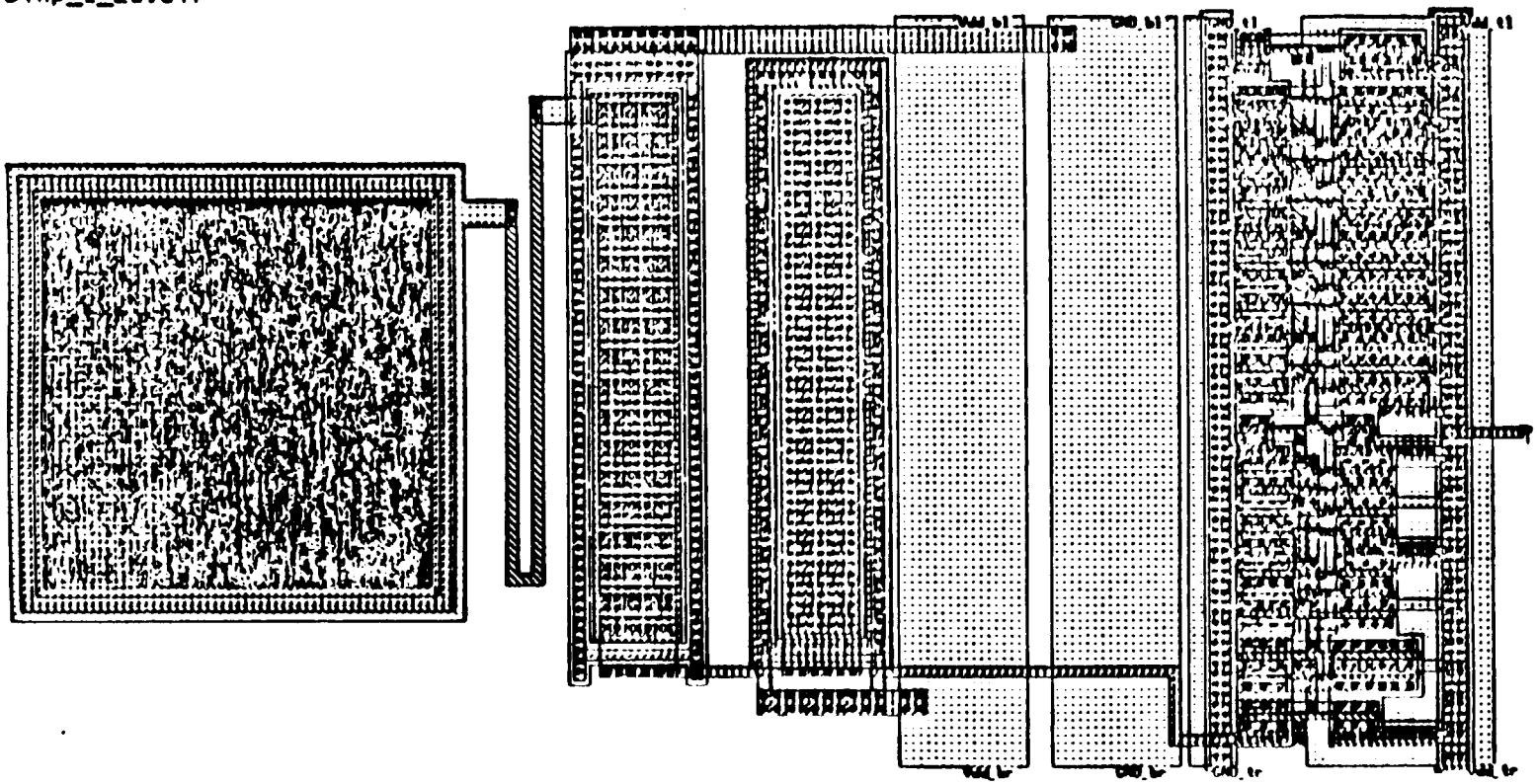
cifplot* Window: -8.1 81.3 -2.4 177 @ u=200 --- Scale: 1 micron is 0.0223 inches (566x)
Bin_1_2u.cif



BIN: Input Buffer

Job: stdin
Date: Wed Mar 8 17:20:35 1989

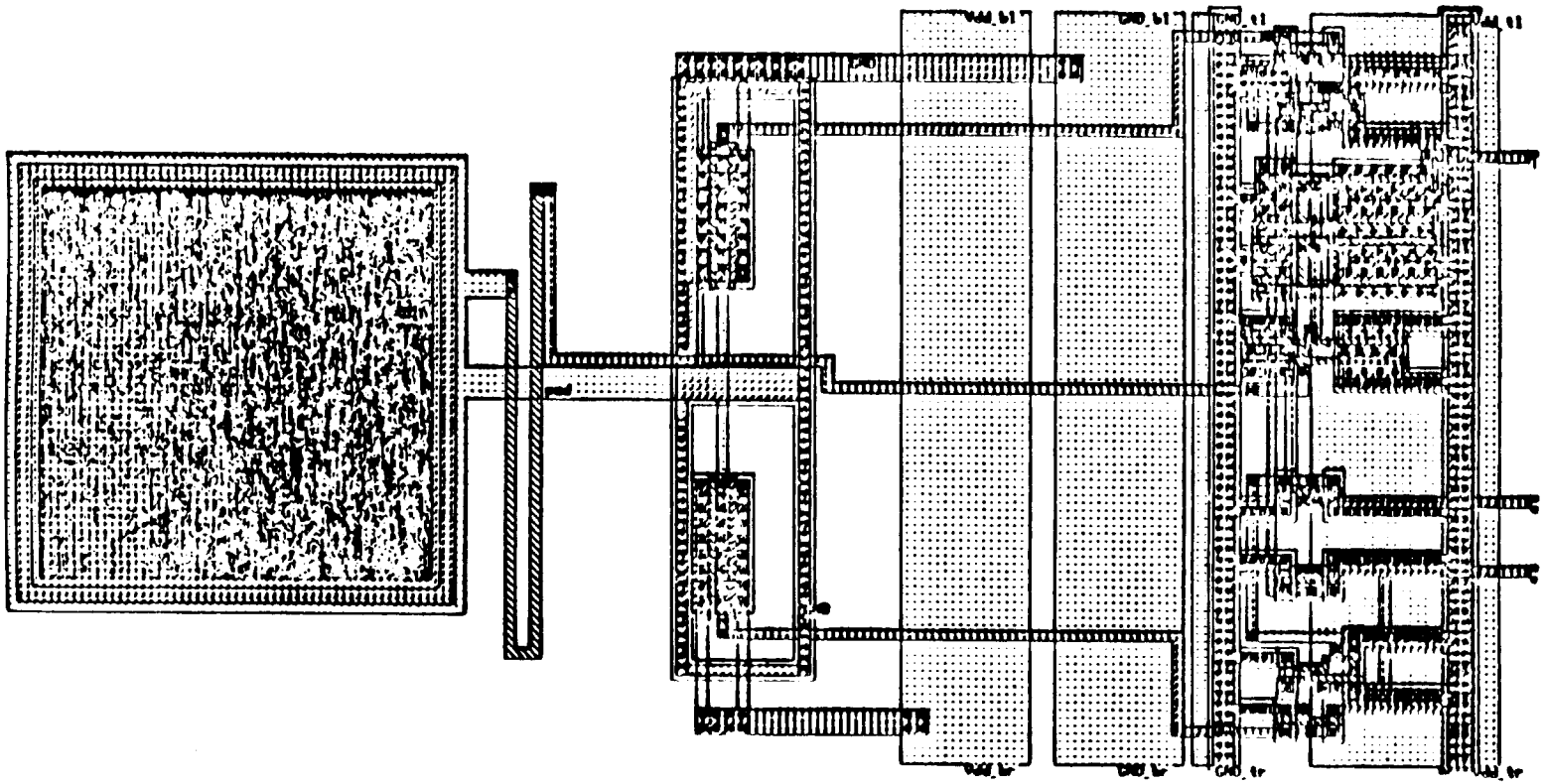
cifplot* Window: -8.1 81.3 6.6 186 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
Binp_1_2u.cif



BINP: Input Clock Buffer

Job: stdin
Date: Wed Mar 8 17:24:39 1989

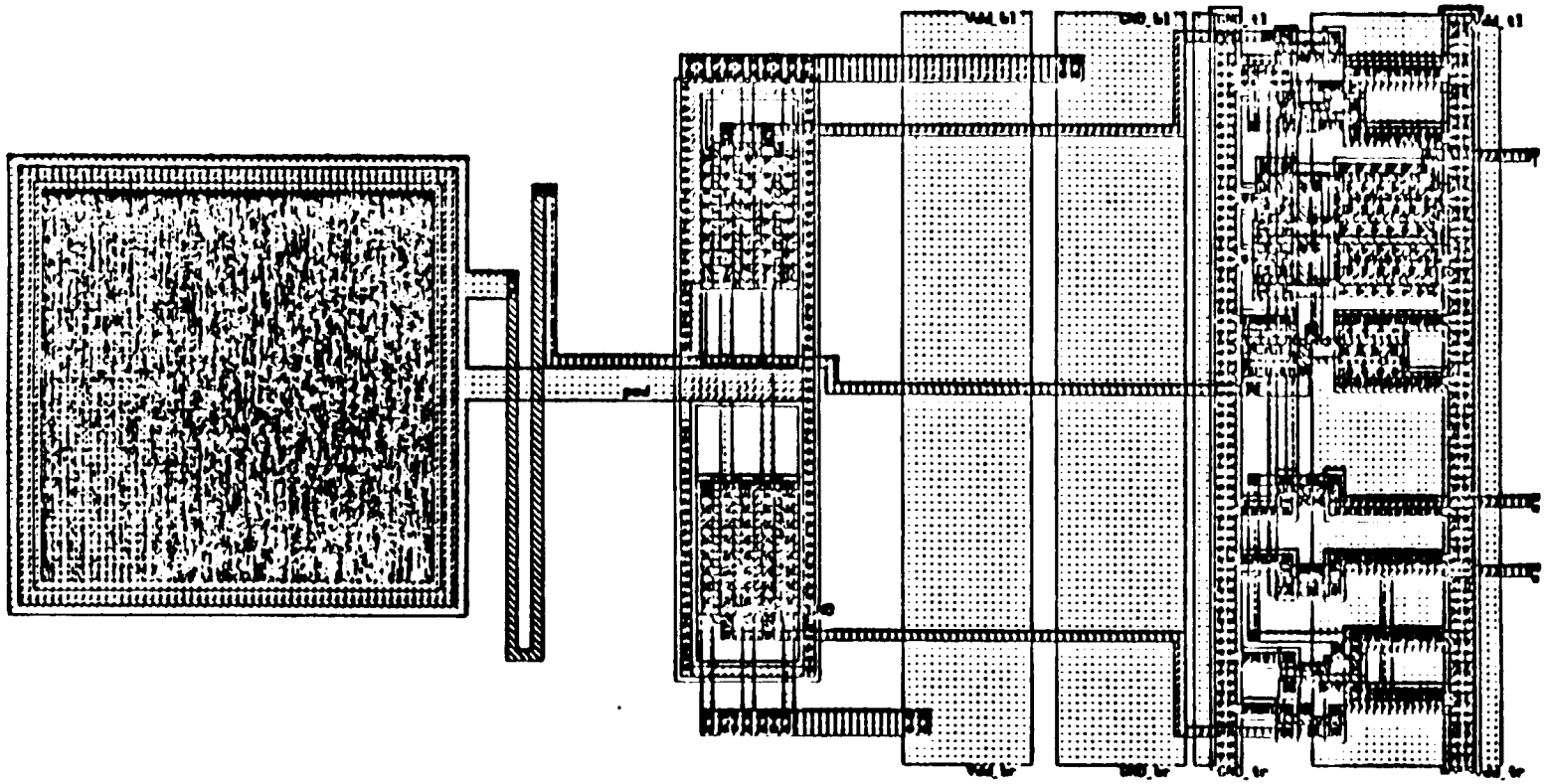
cifplot* Window: -21.6 67.8 9.9 189.3 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
bil_1_2u.cif



BIL: Standard Bidirect Output Buffer

Job: stdin
Date: Wed Mar 8 17:22:31 1989

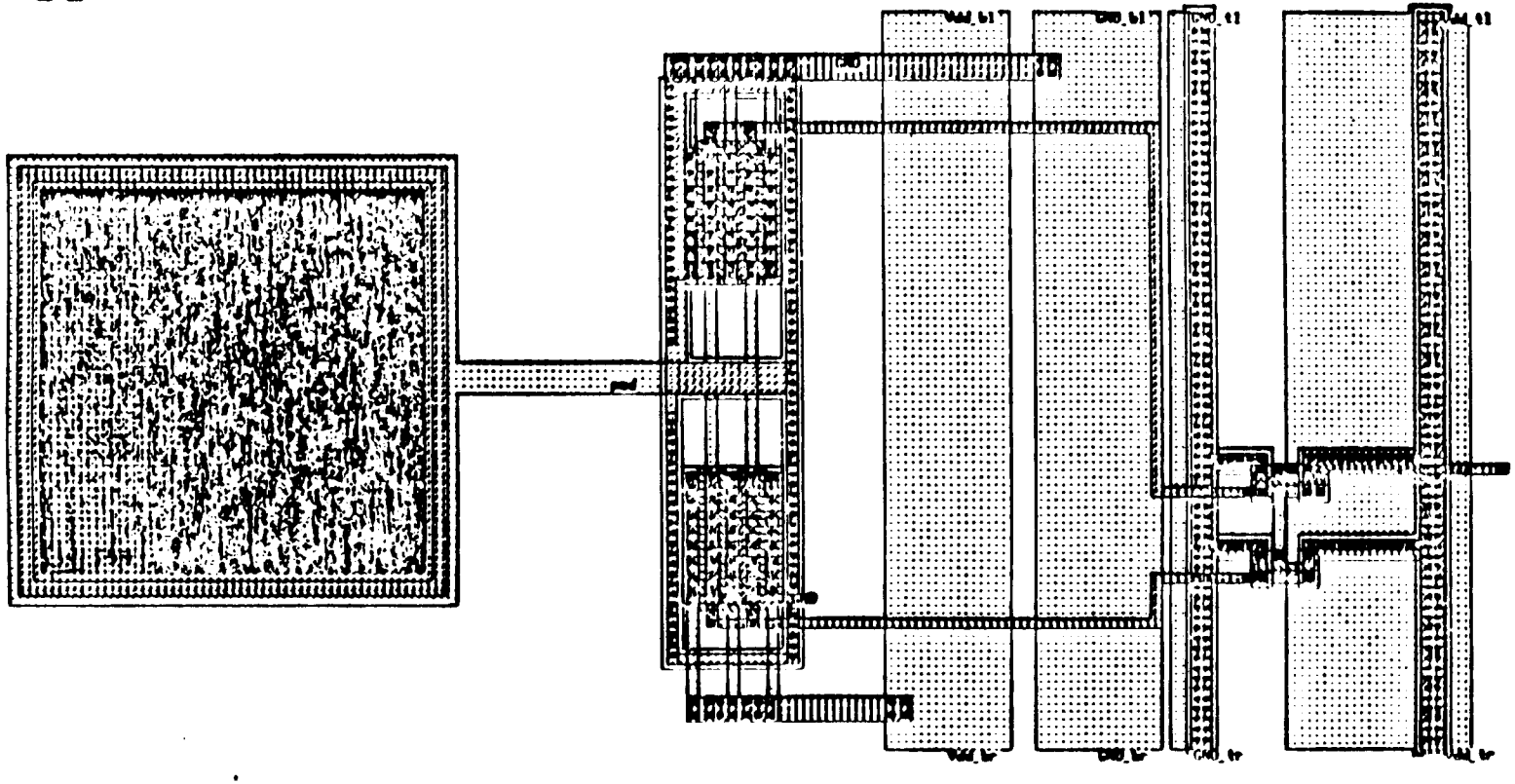
cifplot* Window: -21.6 67.8 9.9 189.3 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
bi_1_2u.cif



BI: High Drive Bidirect Output Buffer

Job: stdin
Date: Wed Mar 8 17:36:15 1989

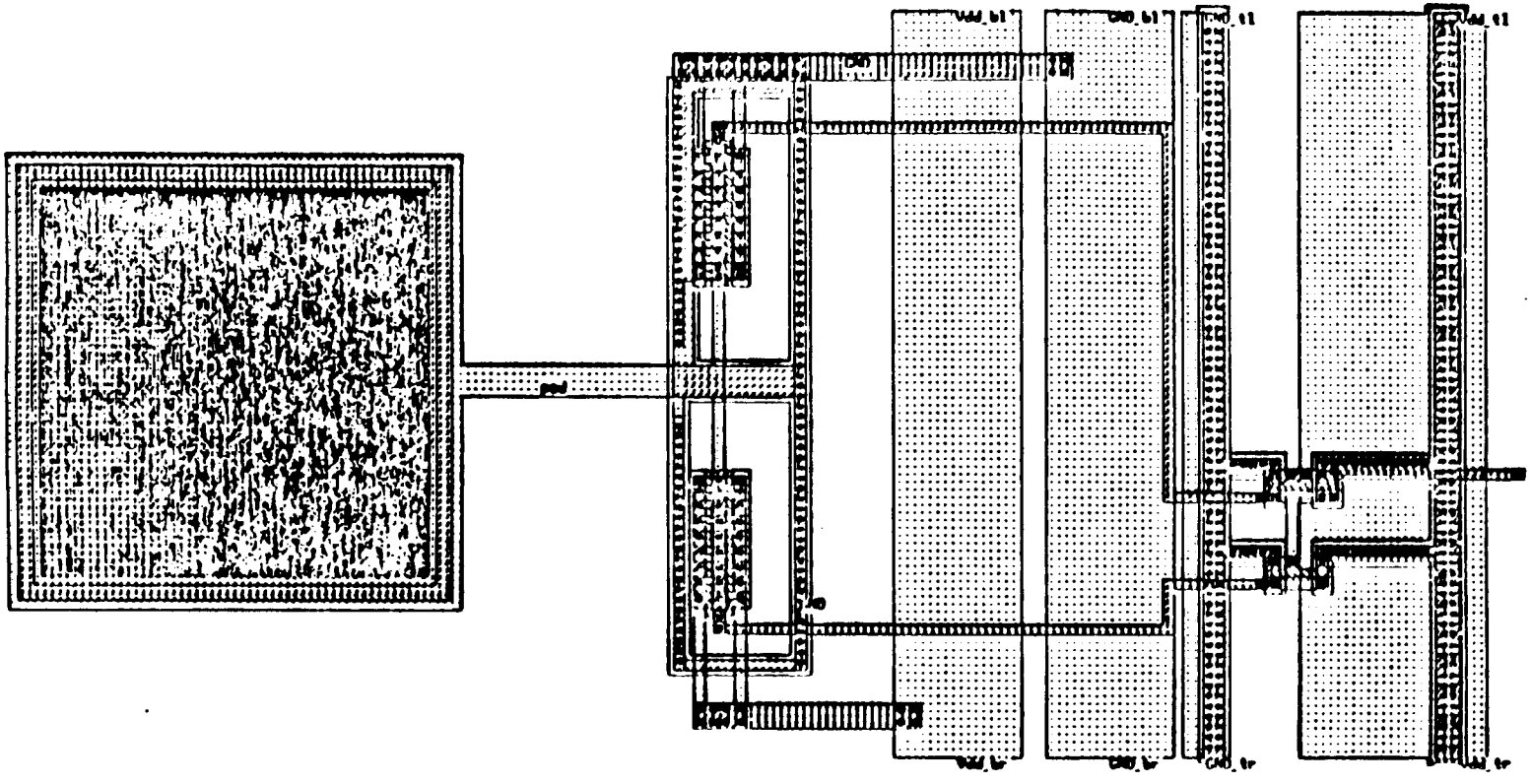
cifplot* Window: -21.6 67.8 9.6 189 @ u=200 --- Scale: 1 micron is 0.0223 inches (566x)
bo_1_2u.cif



BO: High Drive Output Buffer

Job: stdin
Date: Wed Mar 8 17:40:12 1989

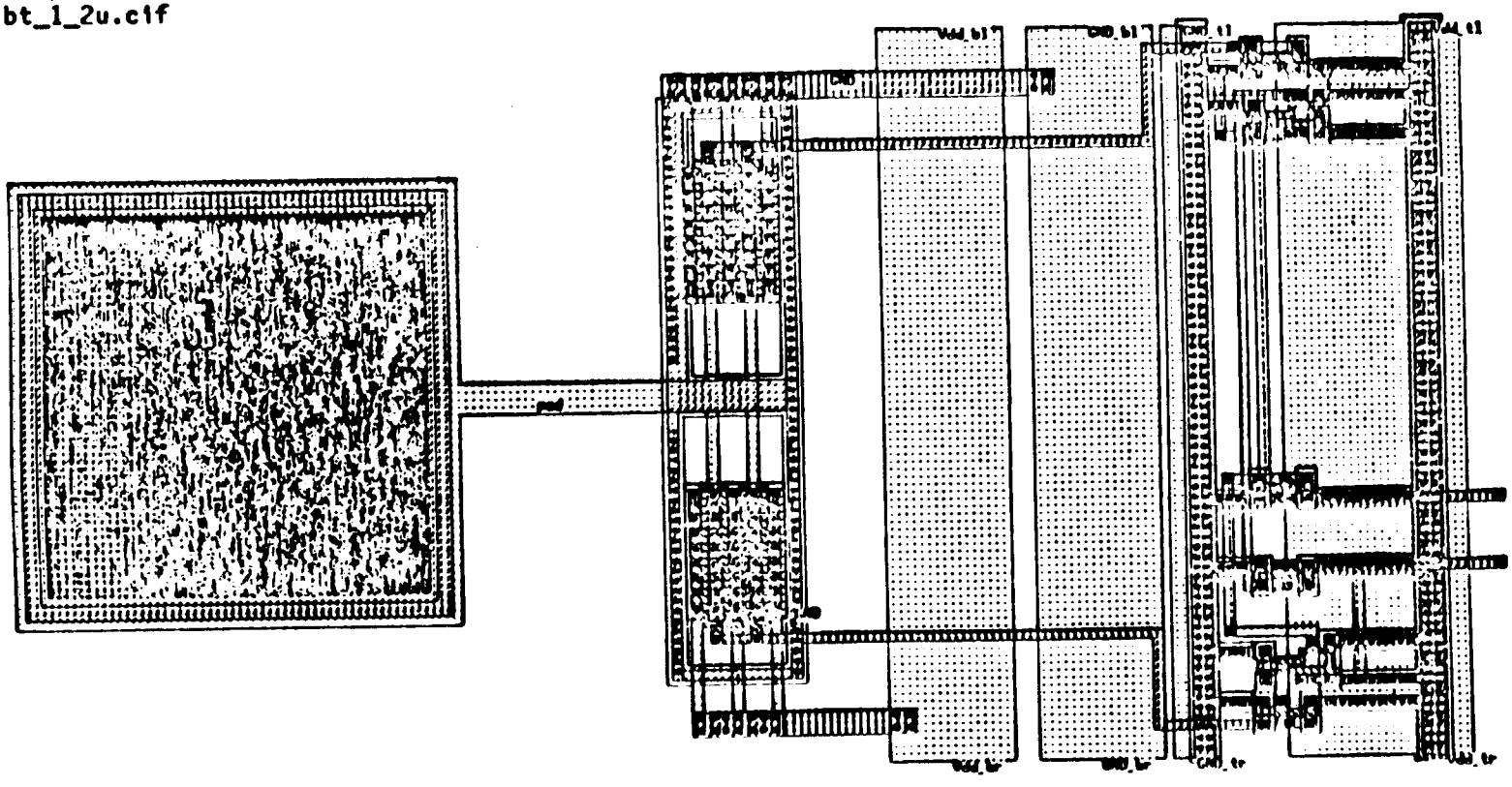
cifplot* Window: -21.6 67.8 9.9 189.3 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
bol_1_2u.cif



BOL: Standard Output Buffer

Job: stdin
Date: Wed Mar 8 17:42:22 1989

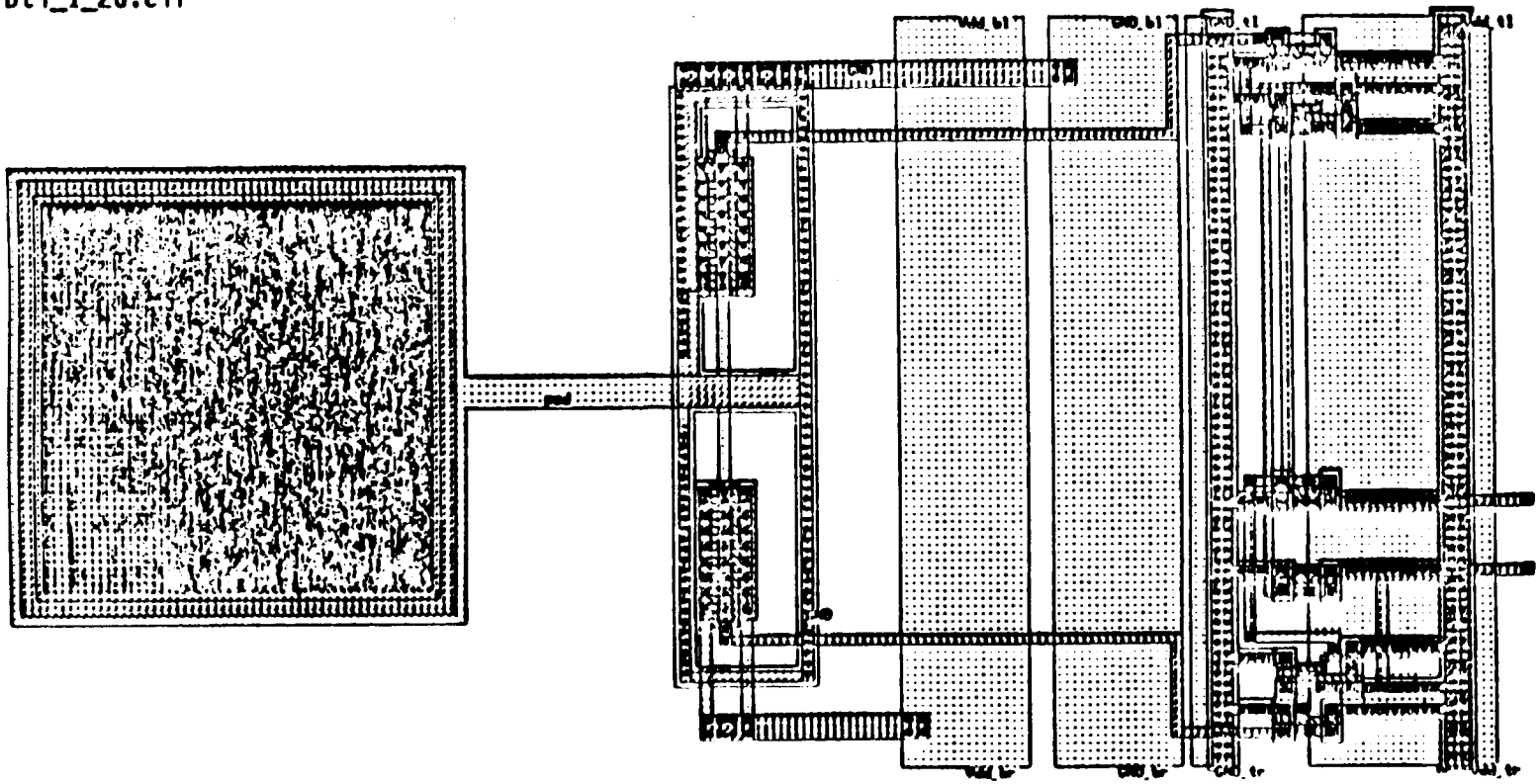
cifplot* Window: -21.6 67.8 9.9 189.3 @ u=200 --- Scale: 1 micron is 0.0223 inches (566x)
bt_1_2u.cif



BT: High Drive Tri-state Output Buffer

Job: stdin
Date: Wed Mar 8 17:51:07 1989

cifplot* Window: -21.6 67.8 9.9 109.3 @ u=200 --- Scale: 1 micron is 0.0223 inches (666x)
btl_1_2u.cif



BTL: Standard Tri-state Output Buffer

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ERRATA: The pages of this technical report have been misnumbered. Page #43 is missing.